ALPHA & OMEGA SEMICONDUCTOR

AO3422
N-Channel Enhancement Mode Field Effect Transistor

General Description

The AO3422 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. It offers operation over a wide gate drive range from 2.5V to 12V. This device is suitable for use as a load switch.

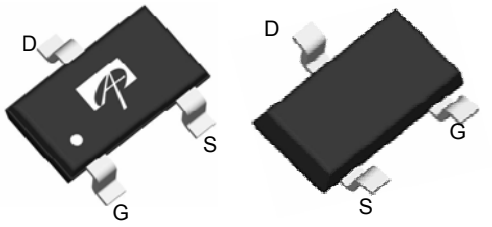
Features

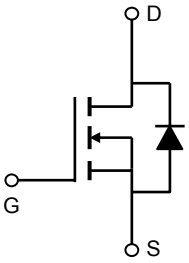
V_{DS} (V) = 55V
I_D = 2.1A (V_{GS} = 4.5V)
$R_{DS(ON)}$ < 160mΩ (V_{GS} = 4.5V)
$R_{DS(ON)}$ < 200mΩ (V_{GS} = 2.5V)

Green Product

SOT23

Top View **Bottom View**





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	55	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current [A]	T_A=25°C	I_D	2.1	A
	T_A=70°C		1.7	
Pulsed Drain Current [B]		I_{DM}	10	
Power Dissipation	T_A=25°C	P_D	1.25	W
	T_A=70°C		0.8	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	75	100	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		115	150	°C/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	48	60	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=10mA, V_{GS}=0V	55			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=44V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Source leakage current	V_{DS}=0V, V_{GS}=±12V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	0.6	1.3	2	V
$I_{D(ON)}$	On state drain current	V_{GS}=4.5V, V_{DS}=5V	10			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=4.5V, I_D=2.1A		125	160	mΩ
		T_J=125°C		175	210	
		V_{GS}=2.5V, I_D=1.5A		157	200	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=2.1A		11		S
V_{SD}	Diode Forward Voltage	I_S=1A		0.78	1	V
I_S	Maximum Body-Diode Continuous Current				1	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=25V, f=1MHz		214	300	pF
C_{oss}	Output Capacitance			31		pF
C_{rss}	Reverse Transfer Capacitance			12.6		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		1.3	3	Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{GS}=4.5V, V_{DS}=27.5V, I_D=2.1A		2.6	3.3	nC
Q_{gs}	Gate Source Charge			0.6		nC
Q_{gd}	Gate Drain Charge			0.8		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=27.5V, R_L=12Ω, R_{GEN}=3Ω		2.3		ns
t_r	Turn-On Rise Time			2.4		ns
$t_{D(off)}$	Turn-Off DelayTime			16.5		ns
t_f	Turn-Off Fall Time			2		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=2.1A, dI/dt=100A/µs		20	30	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=2.1A, dI/dt=100A/µs		17		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in ^{2} FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.
B: Repetitive rating, pulse width limited by junction temperature.
C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.
D. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.
E. These tests are performed with the device mounted on 1 in ^{2} FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.
Rev2: Sep 2010

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

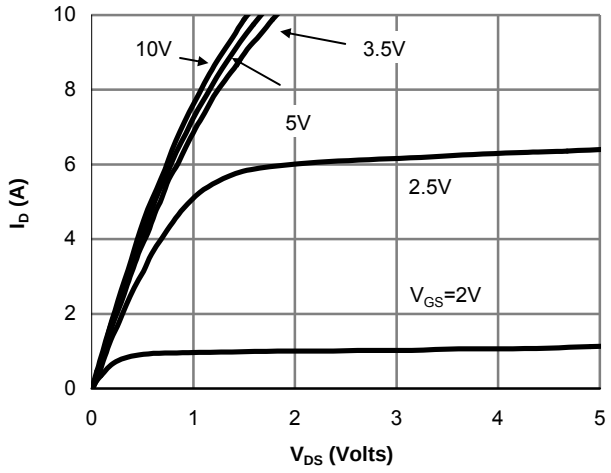


Fig 1: On-Region characteristics

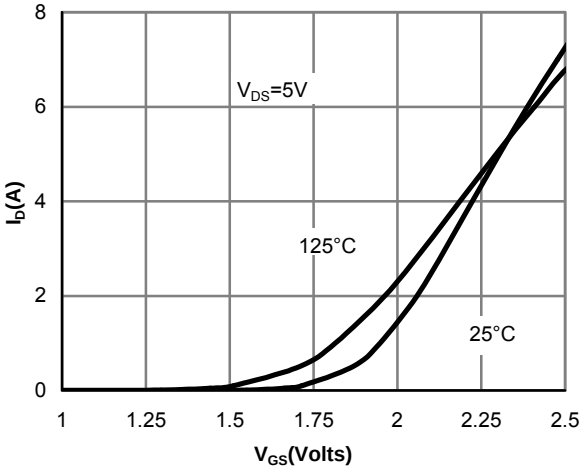


Figure 2: Transfer Characteristics

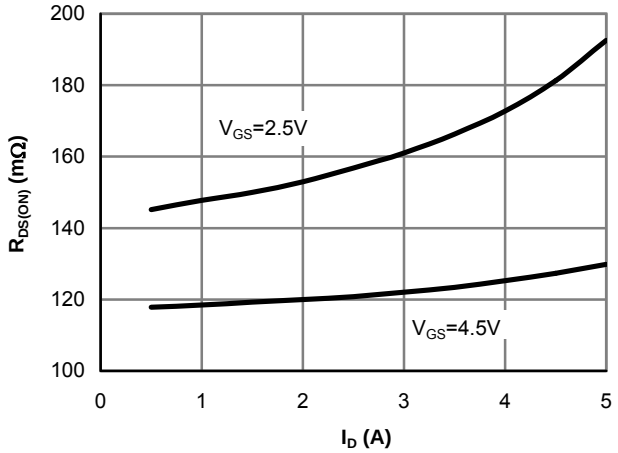


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

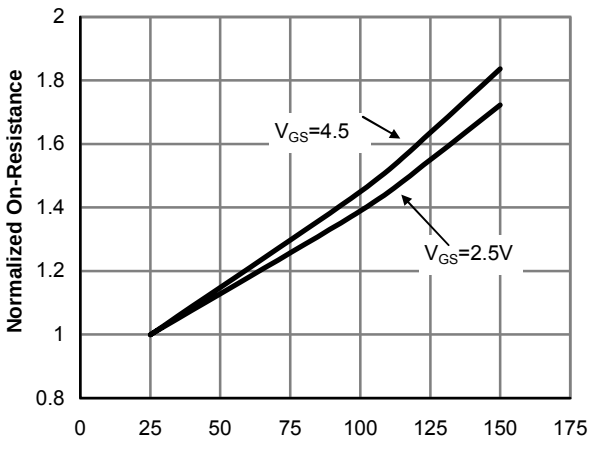


Figure 4: On-Resistance vs. Junction Temperature

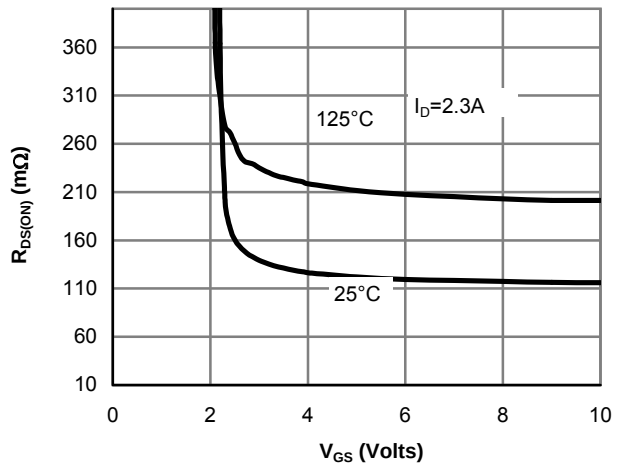


Figure 5: On-Resistance vs. Gate-Source Voltage

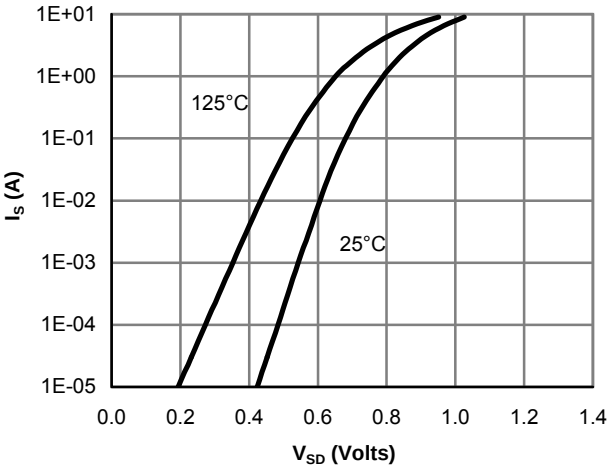


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

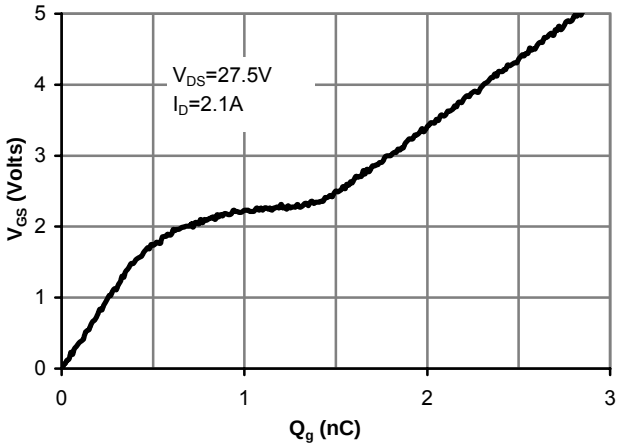


Figure 7: Gate-Charge Characteristics

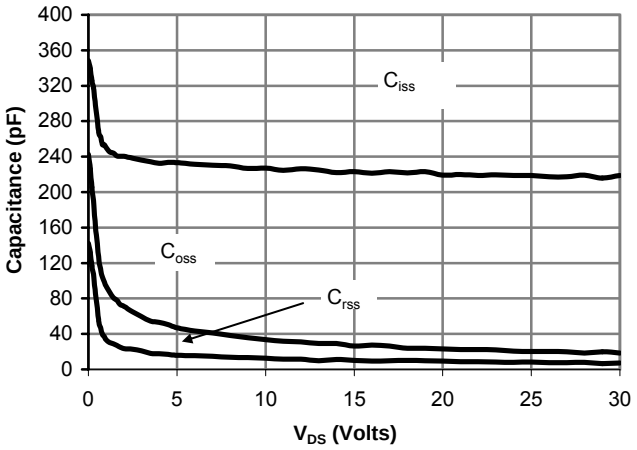


Figure 8: Capacitance Characteristics

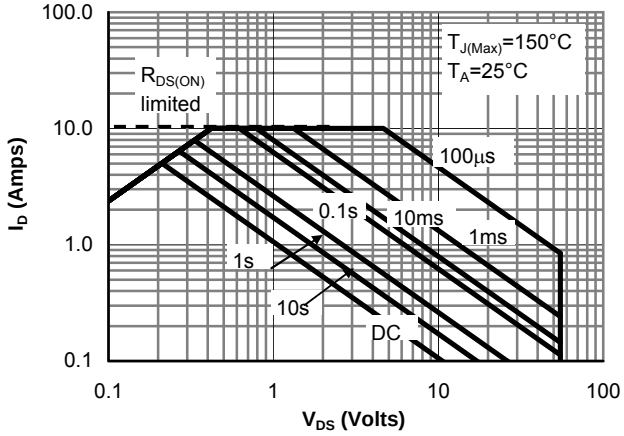


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

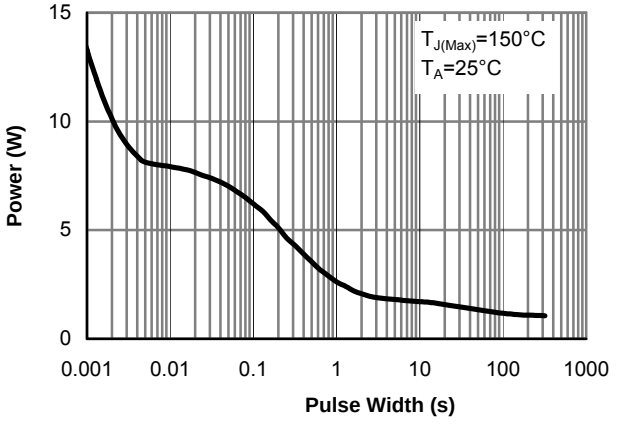


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

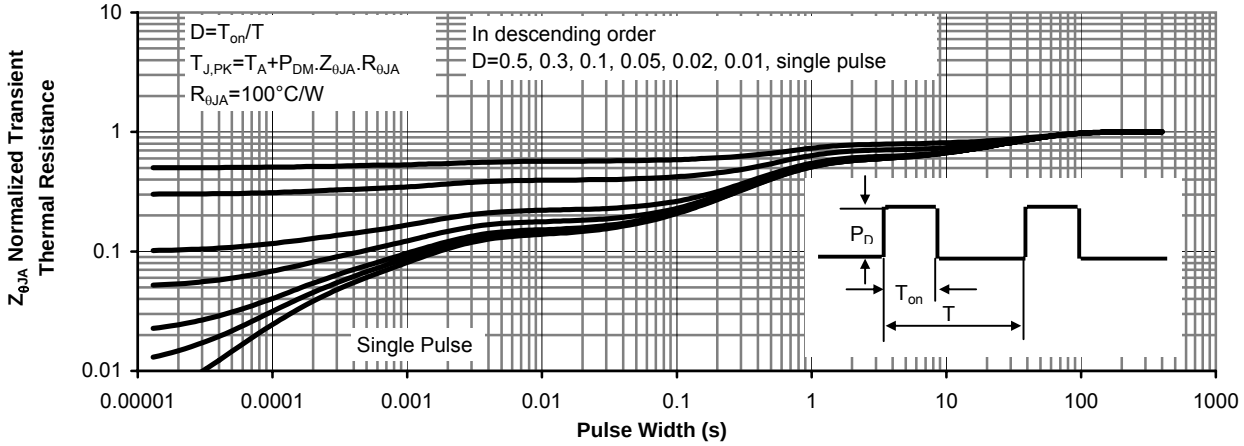
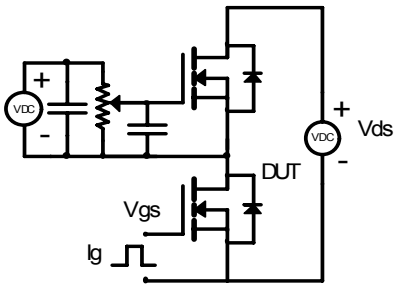
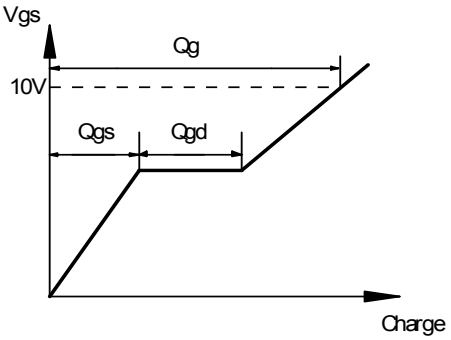


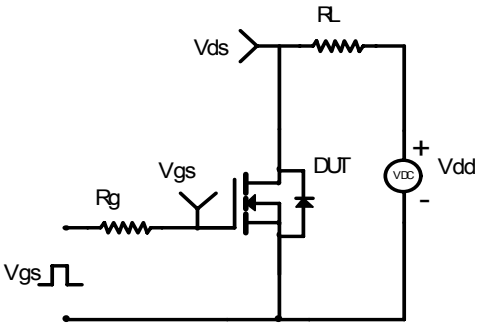
Figure 11: Normalized Maximum Transient Thermal Impedance

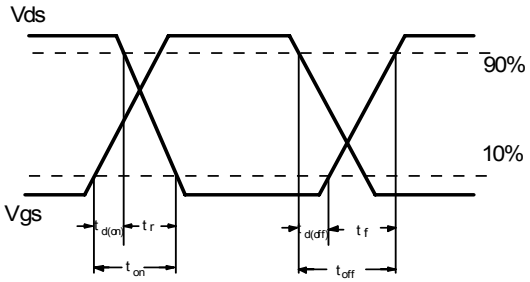
Gate Charge Test Circuit & Waveform



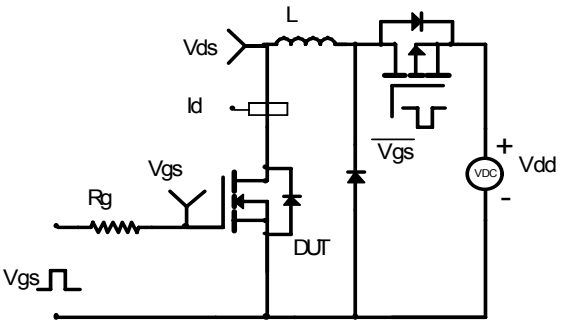


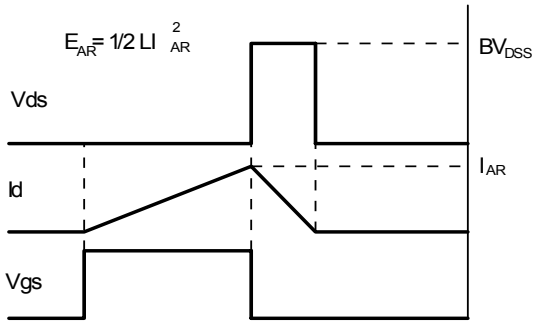
Resistive Switching Test Circuit & Waveforms





Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





Diode Recovery Test Circuit & Waveforms