

High-Speed CMOS Logic 8-Stage Synchronous Down Counters

Features

- Synchronous or Asynchronous Preset
- Cascadable in Synchronous or Ripple Mode
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL} , V_{OH}

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC40103F3A	-55 to 125	16 Ld CERDIP
CD74HC40103E	-55 to 125	16 Ld PDIP
CD74HC40103M	-55 to 125	16 Ld SOIC
CD74HC40103MT	-55 to 125	16 Ld SOIC
CD74HC40103M96	-55 to 125	16 Ld SOIC
CD74HCT40103E	-55 to 125	16 Ld PDIP
CD74HCT40103M	-55 to 125	16 Ld SOIC
CD74HCT40103MT	-55 to 125	16 Ld SOIC
CD74HCT40103M96	-55 to 125	16 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

Description

The 'HC40103 and CD74HCT40103 are manufactured with high speed silicon gate technology and consist of an 8-stage synchronous down counter with a single output which is active when the internal count is zero. The 40103 contains a single 8-bit binary counter. Each has control inputs for enabling or disabling the clock, for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the \overline{TC} output are active-low logic.

In normal operation, the counter is decremented by one count on each positive transition of the CLOCK (CP). Counting is inhibited when the \overline{TE} input is high. The \overline{TC} output goes low when the count reaches zero if the \overline{TE} input is low, and remains low for one full clock period.

When the \overline{PE} input is low, data at the P0-P7 inputs are clocked into the counter on the next positive clock transition regardless of the state of the \overline{TE} input. When the \overline{PL} input is low, data at the P0-P7 inputs are asynchronously forced into the counter regardless of the state of the \overline{PE} , \overline{TE} , or CLOCK inputs. Input P0-P7 represent a single 8-bit binary word for the 40103. When the MR input is low, the counter is asynchronously cleared to its maximum count of 255_{10} , regardless of the state of any other input. The precedence relationship between control inputs is indicated in the truth table.

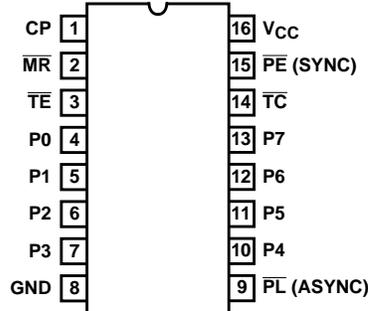
If all control inputs except \overline{TE} are high at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 100_{16} or 256_{10} clock pulses long.

The 40103 may be cascaded using the \overline{TE} input and the \overline{TC} output, in either a synchronous or ripple mode. These circuits possess the low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits and can drive up to 10 LSTTL loads.

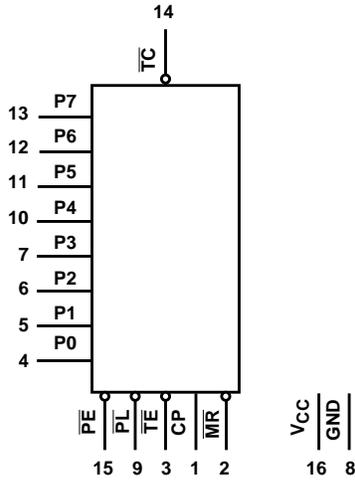
CD54HC40103, CD74HC40103, CD74HCT40103

Pinout

CD54HC40103
(CERDIP)
CD74HC40103, CD74HCT40103
(PDIP, SOIC)
TOP VIEW



Functional Diagram



TRUTH TABLE

CONTROL INPUTS				PRESET MODE	ACTION
MR	PL	PE	TE		
1	1	1	1	Synchronous	Inhibit Counter
1	1	1	0		Count Down
1	1	0	X		Preset On Next Positive Clock Transition
1	0	X	X	Asynchronously	Preset Asynchronously
0	X	X	X		Clear to Maximum Count

1 = High Level.

0 = Low Level.

X = Don't Care.

Clock connected to clock input.

Synchronous Operation: changes occur on negative-to-positive clock transitions.

Load Inputs: MSB = P7, LSB = P0.

CD54HC40103, CD74HC40103, CD74HCT40103

Absolute Maximum Ratings

DC Supply Voltage, V_{CC}	-0.5V to 7V
DC Input Diode Current, I_{IK}	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Diode Current, I_{OK}	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, I_O	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	$\pm 25mA$
DC V_{CC} or Ground Current, I_{CC}	$\pm 50mA$

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
E (PDIP) Package	67
M (SOIC) Package	73
Maximum Junction Temperature	150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C (SOIC - Lead Tips Only)

Operating Conditions

Temperature Range, T_A	-55°C to 125°C
Supply Voltage Range, V_{CC}	
HC Types2V to 6V
HCT Types4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O	0V to V_{CC}
Input Rise and Fall Time	
2V	1000ns (Max)
4.5V	500ns (Max)
6V	400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads	V_{OH}	V_{IH} or V_{IL}	-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	V_{OL}	V_{IH} or V_{IL}	-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	± 0.1	-	± 1	-	± 1	μA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	μA

CD54HC40103, CD74HC40103, CD74HCT40103

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HCT TYPES												
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I _I	V _{CC} and GND	0	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	5.5	-	-	8	-	80	-	160	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI _{CC} (Note 2)	V _{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

- For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS (NOTE)
P0-P7	0.20
TE, MR	0.40
CP	0.60
PE	0.80
PL	1.35

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360μA max at 25°C.

Prerequisite for Switching Specifications

PARAMETER	SYMBOL	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES										
CP Pulse Width	t _w	2	165	-	-	205	-	250	-	ns
		4.5	33	-	-	41	-	50	-	ns
		6	28	-	-	35	-	43	-	ns
PL Pulse Width	t _w	2	125	-	-	155	-	190	-	ns
		4.5	25	-	-	31	-	38	-	ns
		6	21	-	-	26	-	32	-	ns

CD54HC40103, CD74HC40103, CD74HCT40103

Prerequisite for Switching Specifications (Continued)

PARAMETER	SYMBOL	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
MR Pulse Width	t _W	2	125	-	-	135	-	190	-	ns
		4.5	25	-	-	31	-	38	-	ns
		6	21	-	-	26	-	32	-	ns
CP Max. Frequency (Note 3)	f _{CP(MAX)}	2	3	-	-	2	-	2	-	MHz
		4.5	15	-	-	12	-	10	-	MHz
		6	18	-	-	14	-	12	-	MHz
P to CP Set-up Time	t _{SU}	2	100	-	-	125	-	150	-	ns
		4.5	20	-	-	25	-	30	-	ns
		6	17	-	-	21	-	26	-	ns
PE to CP Set-up Time	t _{SU}	2	75	-	-	95	-	110	-	ns
		4.5	15	-	-	19	-	22	-	ns
		6	13	-	-	16	-	19	-	ns
TE to CP Set-up Time	t _{SU}	2	150	-	-	190	-	225	-	ns
		4.5	30	-	-	38	-	45	-	ns
		6	26	-	-	33	-	38	-	ns
P to CP Hold Time	t _H	2	5	-	-	5	-	5	-	ns
		4.5	5	-	-	5	-	5	-	ns
		6	5	-	-	5	-	5	-	ns
TE to CP Hold Time	t _H	2	0	-	-	0	-	0	-	ns
		4.5	0	-	-	0	-	0	-	ns
		6	0	-	-	0	-	0	-	ns
MR to CP Removal Time	t _{REM}	2	50	-	-	65	-	75	-	ns
		4.5	10	-	-	13	-	15	-	ns
		6	9	-	-	11	-	13	-	ns
PE to CP Hold Time	t _H	2	2	-	-	2	-	2	-	ns
		4.5	2	-	-	2	-	2	-	ns
		6	2	-	-	2	-	2	-	ns

HCT TYPES

CP Pulse Width	t _W	4.5	35	-	-	44	-	53	-	ns
PL Pulse Width	t _W	4.5	43	-	-	54	-	65	-	ns
MR Pulse Width	t _W	4.5	35	-	-	44	-	53	-	ns
CP Max. Frequency (Note 3)	f _{CP(MAX)}	4.5	14	-	-	11	-	9	-	MHz
P to CP Set-up Time	t _{SU}	4.5	24	-	-	30	-	36	-	ns
PE to CP Set-up Time	t _{SU}	4.5	20	-	-	25	-	30	-	ns
TE to CP Set-up Time	t _{SU}	4.5	40	-	-	50	-	60	-	ns
P to CP Hold Time	t _H	4.5	5	-	-	5	-	5	-	ns
TE to CP Hold Time	t _H	4.5	0	-	-	0	-	0	-	ns
MR to CP Removal Time	t _{REM}	4.5	10	-	-	13	-	15	-	ns
PE to CP Hold Time	t _H	4.5	2	-	-	2	-	2	-	ns

CD54HC40103, CD74HC40103, CD74HCT40103

Switching Specifications Input $t_r, t_f = 6\text{ns}$

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay CP to any \overline{TC} (Async Preset)	$t_{PLH},$ t_{PHL}	$C_L = 50\text{pF}$	2	-	-	300	-	375	-	450	ns
		$C_L = 50\text{pF}$	4.5	-	-	60	-	75	-	90	ns
		$C_L = 15\text{pF}$	5	-	25	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	51	-	64	-	77	ns
CP to \overline{TC} (Sync Preset)	$t_{PLH},$ t_{PHL}	$C_L = 50\text{pF}$	2	-	-	300	-	375	-	450	ns
		$C_L = 50\text{pF}$	4.5	-	-	60	-	75	-	90	ns
		$C_L = 15\text{pF}$	5	-	25	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	51	-	64	-	77	ns
\overline{TE} to \overline{TC}	$t_{PLH},$ t_{PHL}	$C_L = 50\text{pF}$	2	-	-	200	-	250	-	300	ns
		$C_L = 50\text{pF}$	4.5	-	-	40	-	50	-	60	ns
		$C_L = 15\text{pF}$	5	-	17	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	34	-	43	-	51	ns
\overline{PL} to \overline{TC}	$t_{PLH},$ t_{PHL}	$C_L = 50\text{pF}$	2	-	-	275	-	345	-	415	ns
		$C_L = 50\text{pF}$	4.5	-	-	55	-	69	-	83	ns
		$C_L = 15\text{pF}$	5	-	23	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	47	-	59	-	71	ns
\overline{MR} to \overline{TC}	$t_{PLH},$ t_{PHL}	$C_L = 50\text{pF}$	2	-	-	275	-	345	-	415	ns
		$C_L = 50\text{pF}$	4.5	-	-	55	-	69	-	83	ns
		$C_L = 15\text{pF}$	5	-	23	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	47	-	59	-	71	ns
Output Transition Time	t_{TLH}, t_{THL}	$C_L = 50\text{pF}$	2	-	-	75	-	95	-	110	ns
		$C_L = 50\text{pF}$	4.5	-	-	15	-	19	-	22	ns
		$C_L = 50\text{pF}$	6	-	-	13	-	16	-	19	ns
Input Capacitance	C_I	$C_L = 50\text{pF}$	-	-	-	10	-	10	-	10	pF
CP Maximum Frequency	f_{MAX}	$C_L = 15\text{pF}$	5	-	25	-	-	-	-	-	MHz
Power Dissipation Capacitance (Notes 4, 5)	C_{PD}	-	5	-	25	-	-	-	-	-	pF
HCT TYPES											
Propagation Delay CP to \overline{TC} (Async Preset)	$t_{PLH},$ t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	60	-	75	-	90	ns
		$C_L = 15\text{pF}$	5	-	25	-	-	-	-	-	ns
\overline{CE} to \overline{TC} (Sync Preset)	$t_{PLH},$ t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	63	-	79	-	95	ns
		$C_L = 15\text{pF}$	5	-	26	-	-	-	-	-	ns
\overline{TE} to \overline{TC}	$t_{PLH},$ t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	50	-	63	-	75	ns
		$C_L = 15\text{pF}$	5	-	21	-	-	-	-	-	ns
\overline{PL} to \overline{TC}	$t_{PLH},$ t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	68	-	85	-	102	ns
		$C_L = 15\text{pF}$	5	-	28	-	-	-	-	-	ns

CD54HC40103, CD74HC40103, CD74HCT40103

Switching Specifications Input t_r , $t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
\overline{MR} to \overline{TC}	t_{PLH} , t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	55	-	69	-	83	ns
		$C_L = 15\text{pF}$	5	-	23	-	-	-	-	-	ns
Output Transition Time	t_{THL} , t_{TLH}	$C_L = 50\text{pF}$	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	C_{IN}	$C_L = 50\text{pF}$	-	-	-	10	-	10	-	10	pF
CP Maximum Frequency	f_{MAX}	$C_L = 15\text{pF}$	5	-	25	-	-	-	-	-	MHz
Power Dissipation Capacitance (Notes 4, 5)	C_{PD}	-	5	-	27	-	-	-	-	-	pF

NOTES:

- Noncascaded operation only. With cascaded counters clock-to-terminal count propagation delays, count enables (\overline{PE} or \overline{TE})-to-clock SET UP TIMES, and count enables (\overline{PE} or \overline{TE})-to-clock HOLD TIMES determine maximum clock frequency. For example, with these HC devices:

$$C_P f_{MAX} = \frac{1}{\text{CP-to-}\overline{TC} \text{ prop delay} + \overline{TE}\text{-to-CP Setup Time} + \overline{TE}\text{-to-CP Hold Time}} = \frac{1}{60 + 30 + 0} \approx 11\text{MHz}$$

- C_{PD} is used to determine the dynamic power consumption, per package.
- $P_D = V_{CC}^2 f_i + C_L V_{CC}^2 f_o$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage, f_o = Output Frequency.

Timing Diagrams

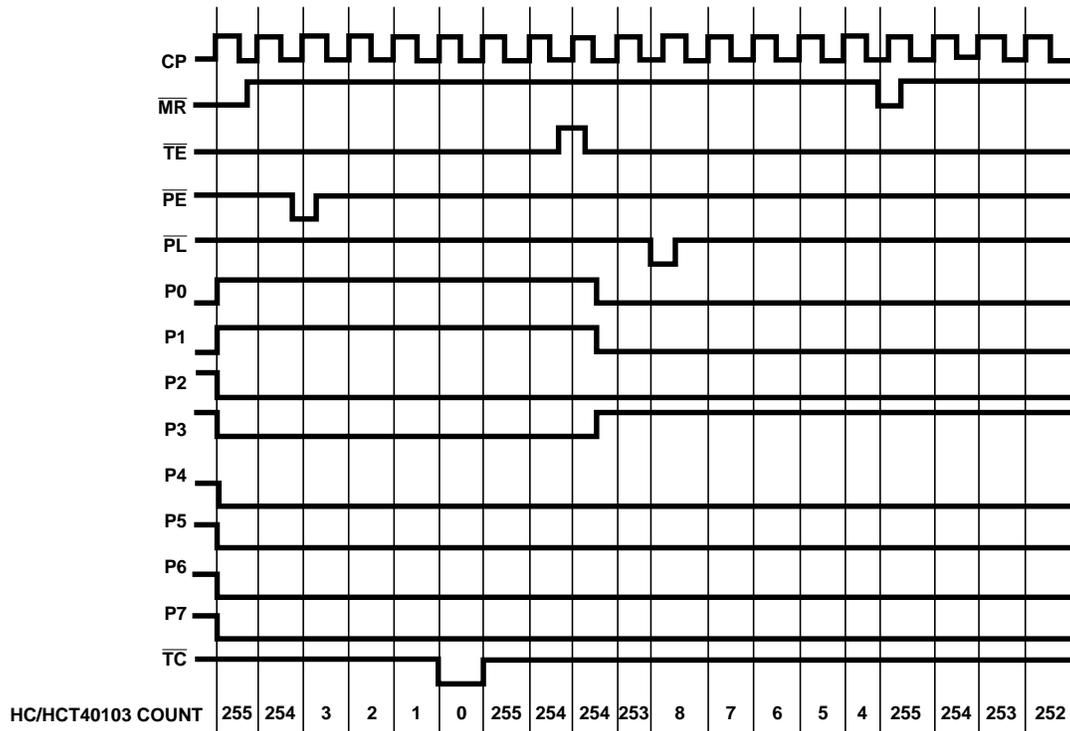


FIGURE 1.

Test Circuits and Waveforms

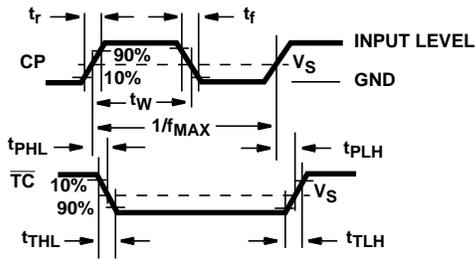


FIGURE 2.

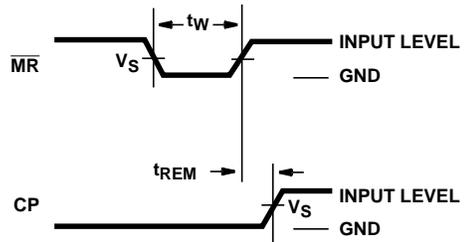


FIGURE 3.

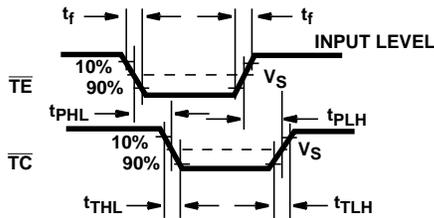


FIGURE 4.

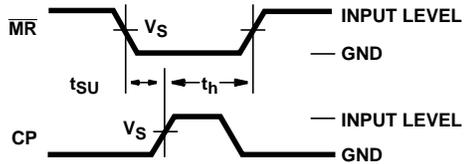


FIGURE 5.

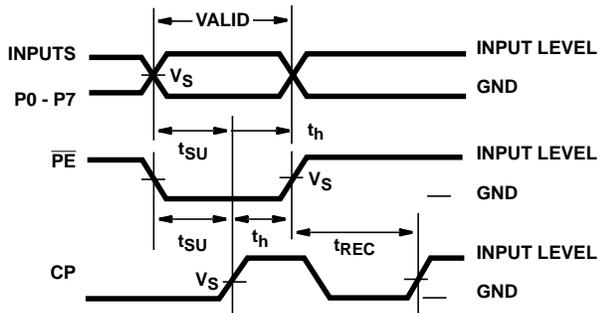


FIGURE 6.

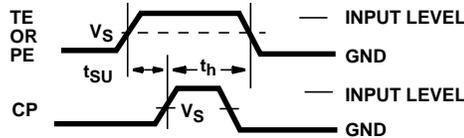
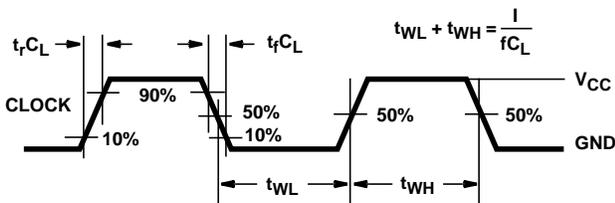
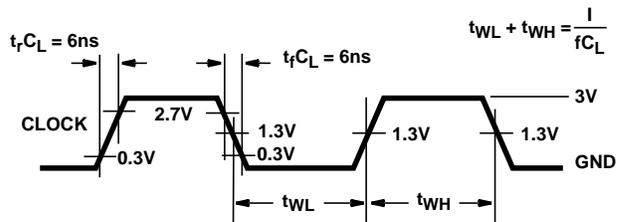


FIGURE 7.



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 8. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 9. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9055301EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9055301EA CD54HC40103F3A	Samples
CD54HC40103F	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54HC40103F	Samples
CD54HC40103F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9055301EA CD54HC40103F3A	Samples
CD74HC40103E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC40103E	Samples
CD74HC40103EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC40103E	Samples
CD74HC40103M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC40103M	Samples
CD74HC40103M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC40103M	Samples
CD74HC40103M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC40103M	Samples
CD74HC40103M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC40103M	Samples
CD74HC40103ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC40103M	Samples
CD74HC40103MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC40103M	Samples
CD74HC40103MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC40103M	Samples
CD74HCT40103E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT40103E	Samples
CD74HCT40103EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT40103E	Samples
CD74HCT40103M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT40103M	Samples
CD74HCT40103M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT40103M	Samples
CD74HCT40103M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT40103M	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HCT40103MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT40103M	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

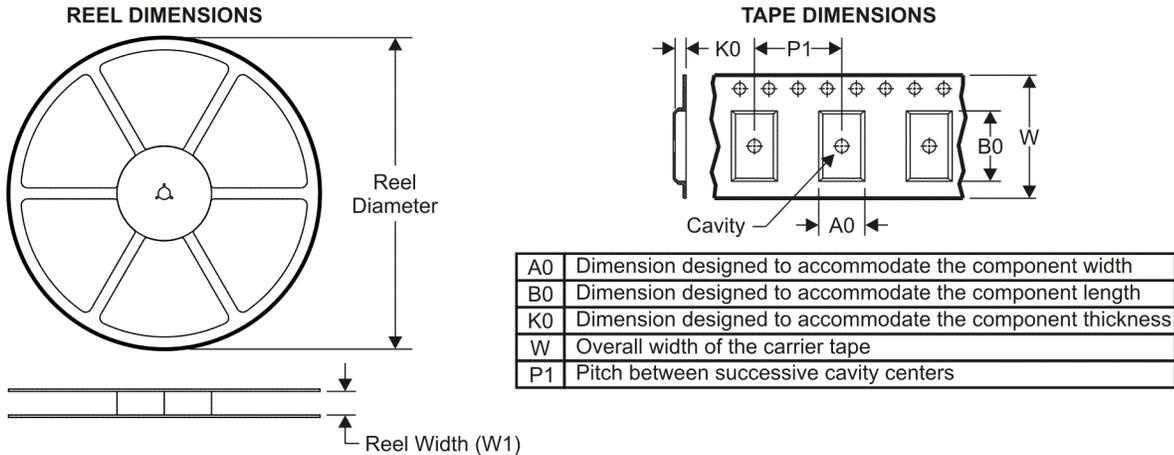
OTHER QUALIFIED VERSIONS OF CD54HC40103, CD74HC40103 :

- Catalog: [CD74HC40103](#)
- Enhanced Product: [CD74HC40103-EP](#), [CD74HC40103-EP](#)
- Military: [CD54HC40103](#)

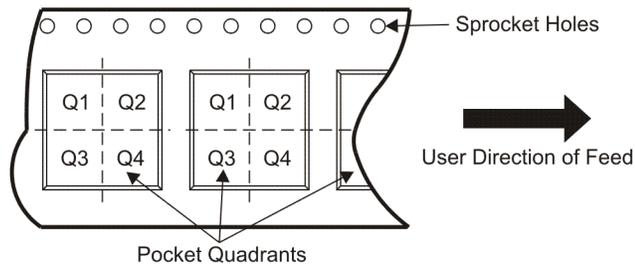
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



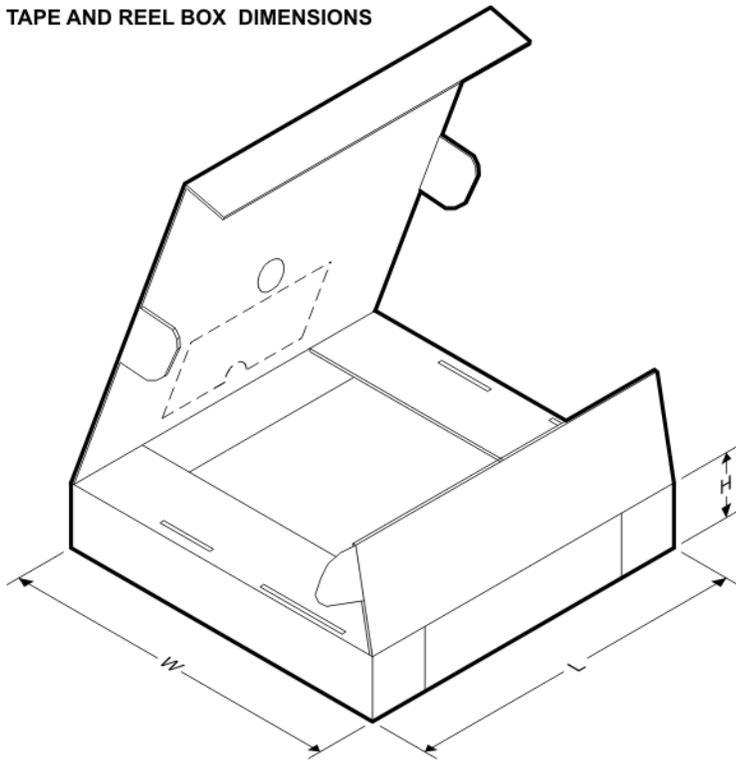
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC40103M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT40103M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

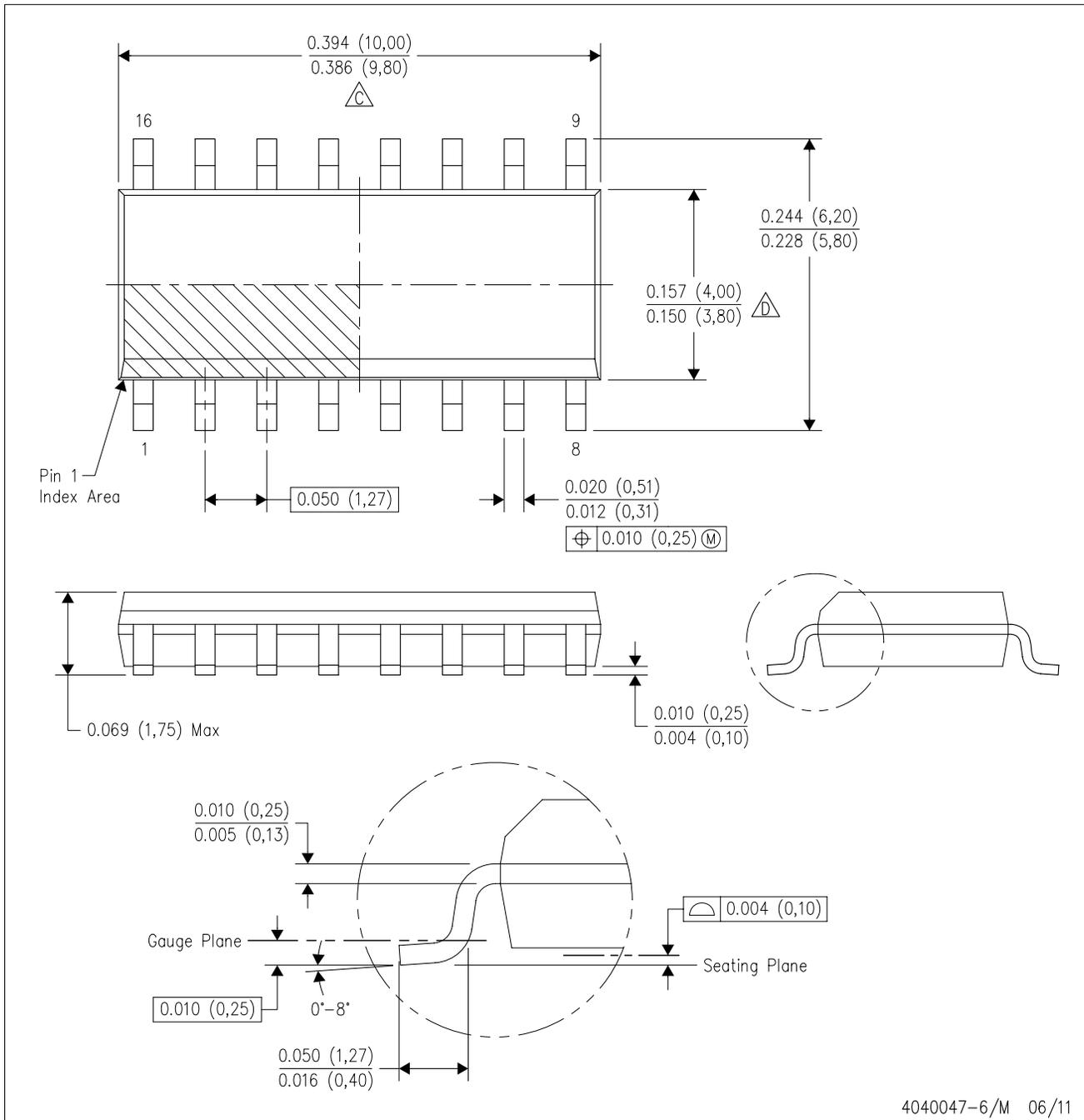


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC40103M96	SOIC	D	16	2500	333.2	345.9	28.6
CD74HCT40103M96	SOIC	D	16	2500	333.2	345.9	28.6

D (R-PDSO-G16)

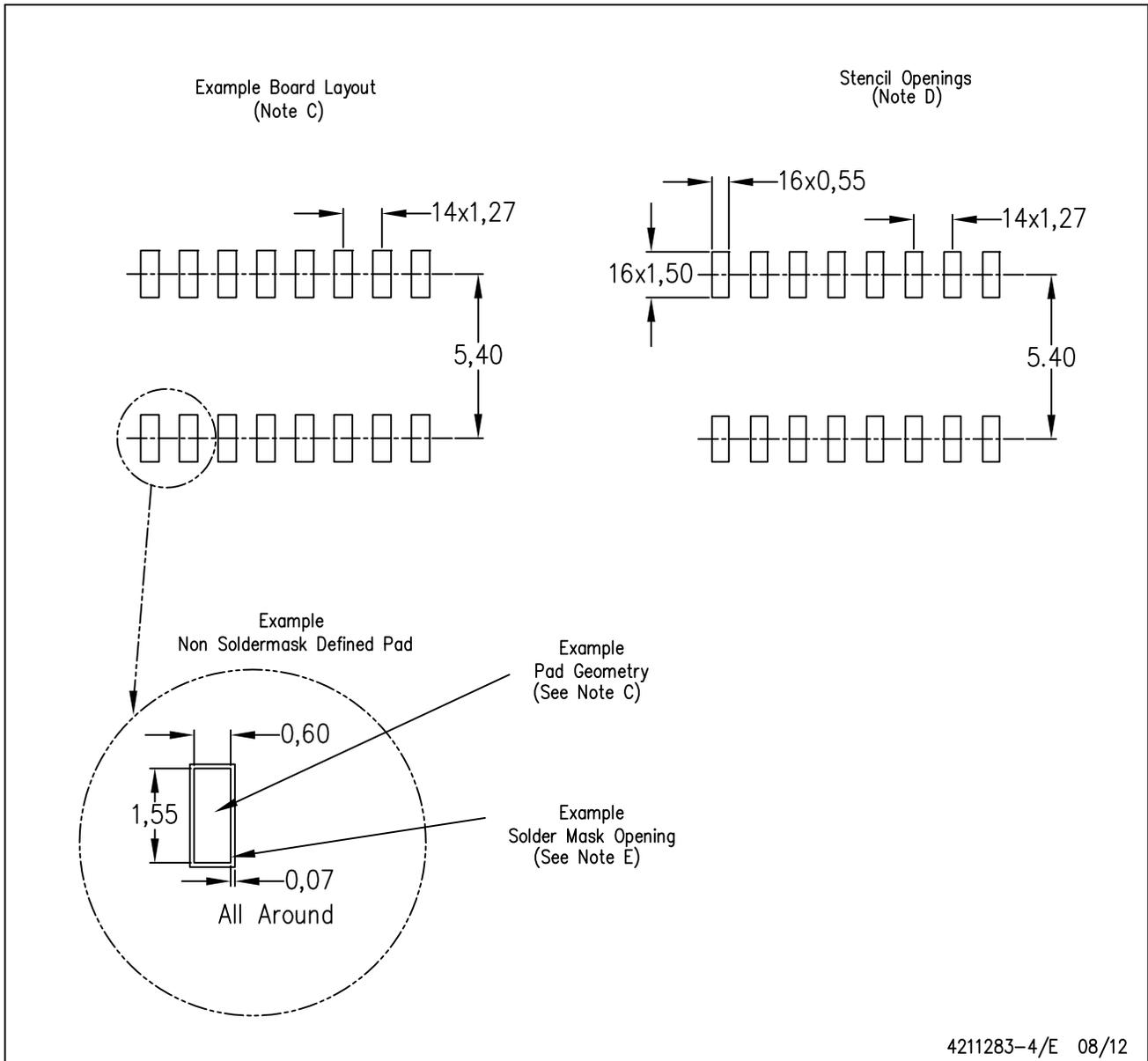
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

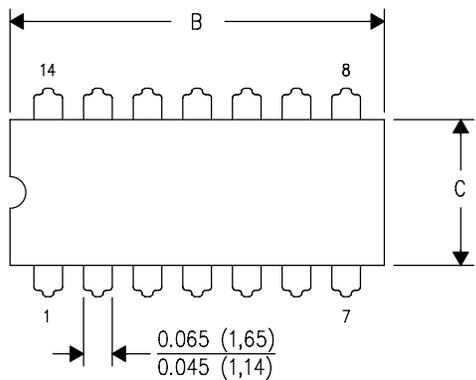


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

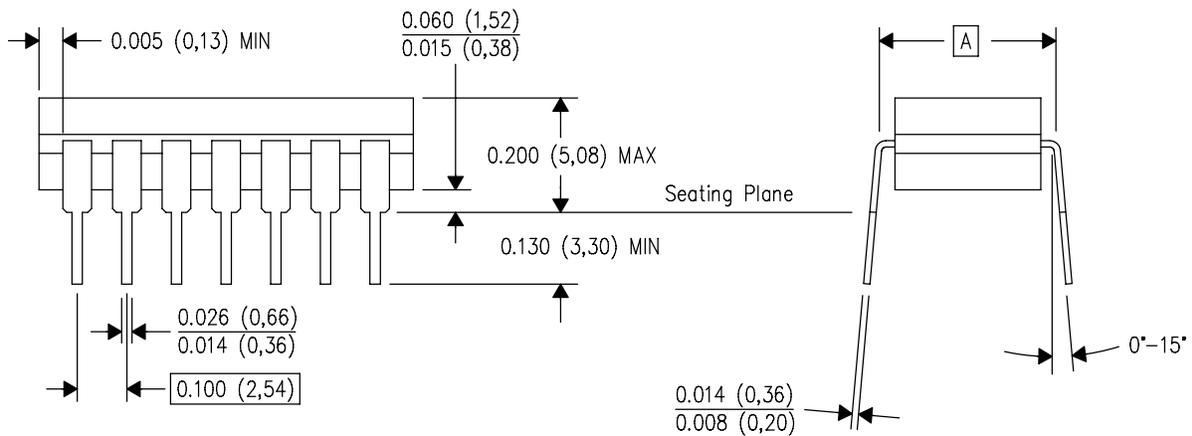
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.