

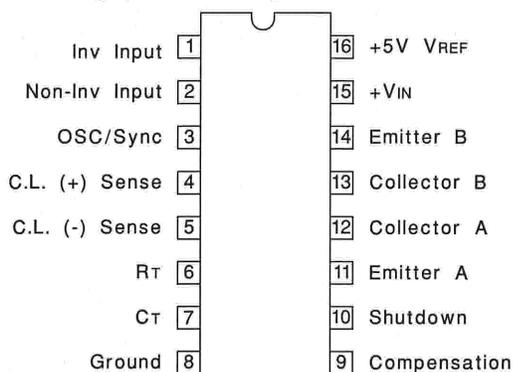


### ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V <sub>IN</sub> )	40V
Collector Supply Voltage (V <sub>C</sub> )	60V
Output Current (each Output)	200mA
Maximum Forced Voltage (Pin 9, 10)	-3 to +5V
Maximum Forced Current (Pin 9, 10)	±10mA
Reference Output Current	50mA
Oscillator Charging Current	5mA
Power Dissipation at T <sub>A</sub> = +25°C	1000mW
Power Dissipation at T <sub>C</sub> = +25°C	2000mW
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature, (Soldering, 10 seconds)	+300°C

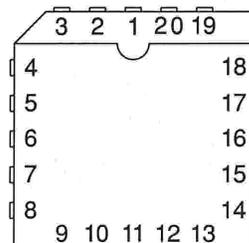
Note: Consult packaging section of Databook for thermal limitations and considerations of package.

### DIL-16, SOIC-16 (TOP VIEW) J or N Package, DW Package



### CONNECTION DIAGRAMS

#### PLCC-20, LCC-20 (TOP VIEW) Q or L Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Inv. Input	2
Non-Inv. Input	3
OSC/SYNC	4
C.L. (+) sense	5
N/C	6
C.L. (-) sense	7
R <sub>T</sub>	8
C <sub>T</sub>	9
Ground	10
N/C	11
Compensation	12
Shutdown	13
Emitter A	14
Collector A	15
N/C	16
Collector B	17
Emitter B	18
+V <sub>IN</sub>	19
+5V V <sub>REF</sub>	20

**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for T<sub>A</sub> = -55°C to +125°C for the UC1524A, -40° to +85°C for the UC2524A, and 0°C to +70°C for the UC3524A; V<sub>IN</sub> = V<sub>C</sub> = 20V, T<sub>A</sub> = T<sub>J</sub>.

PARAMETER	TEST CONDITIONS	UC1524A / UC2524A			UC3524A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>Turn-on Characteristics</b>								
Input Voltage	Operating Range after Turn-on	8		40	8		40	V
Turn-on Threshold		6.5	7.5	8.5	6.5	7.5	8.5	V
Turn-on Current	V <sub>IN</sub> = 6V		2.5	4		2.5	4	mA
Operating Current	V <sub>IN</sub> = 8 to 40V		5	10		5	10	mA
Turn-on Hysteresis*			0.5			0.5		V
<b>Reference Section</b>								
Output Voltage	T <sub>J</sub> = 25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
	Over Operating Range	4.9		5.1	4.85		5.15	V
Line Regulation	V <sub>IN</sub> = 10 to 40V		10	20		10	30	mV
Load Regulation	I <sub>L</sub> = 0 to 20 mA		20	25		20	35	mV
Temperature Stability*	Over Operating Range*		20	25		20	35	mV
Short Circuit Current	V <sub>REF</sub> = 0, 25°C ≤ T <sub>J</sub> ≤ 125°C		80	100		80	100	mA
Output Noise Voltage*	10Hz ≤ f ≤ 10kHz, T <sub>J</sub> = 25°C		40			40		μV <sub>rms</sub>
Long Term Stability*	T <sub>J</sub> = 125°C, 1000 Hrs.		20	50		20	50	mV

\* These parameters are ensured by design but not 100% tested in production.

**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for  $T_A = -55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  for the UC1524A,  $-40^{\circ}$  to  $+85^{\circ}\text{C}$  for the UC2524A, and  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$  for the UC3524A;  $V_{IN} = V_C = 20\text{V}$ ,  $T_A = T_J$ .

PARAMETER	TEST CONDITIONS	UC1524A / UC2524A			UC3524A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>Oscillator Section</b> (Unless otherwise specified, $R_T = 2700\Omega$ , $C_T = 0.01\text{ mfd}$ )								
Initial Accuracy	$T_J = 25^{\circ}\text{C}$	41	43	45	39	43	47	kHz
	Over Operating Range	40.2		45.9	38.2		47.9	kHz
Temperature Stability*	Over Operating Temperature Range		1	2		1	2	%
Minimum Frequency	$R_T = 150\text{k}\Omega$ , $C_T = 0.1\text{ mfd}$			140			120	Hz
Maximum Frequency	$R_T = 2.0\text{k}\Omega$ , $C_T = 470\text{pF}$	500			500			kHz
Output Amplitude*		3	3.5		3	3.5		V
Output Pulse Width*		0.29	0.5	1.0	0.3	0.5	1.0	$\mu\text{s}$
Ramp Peak		3.3	3.5	3.7	3.3	3.5	3.7	V
Ramp Valley	$T_J = 25^{\circ}\text{C}$	0.7	0.8	0.9	0.7	0.8	0.9	V
Ramp Valley T.C.			-1.0			-1.0		$\text{mV}/^{\circ}\text{C}$
<b>Error Amplifier Section</b> (Unless otherwise specified, $V_{CM} = 2.5\text{V}$ )								
Input Offset Voltage			0.5	5		2	10	mV
Input Bias Current			1	5		1	10	$\mu\text{A}$
Input Offset Current			.05	1		0.5	1	$\mu\text{A}$
Common Mode Rejection Ratio	$V_{CM} = 1.5$ to $5.5\text{V}$	70	80		70	80		dB
Power Supply Rejection Ratio	$V_{IN} = 10$ to $40\text{V}$	70	80		70	80		dB
Output Swing (Note 1)		5.0		0.5	5.0		0.5	V
Open Loop Voltage Gain	$\Delta V_O = 1$ to $4\text{V}$ , $R_L \geq 10\text{M}\Omega$	72	80		64	80		dB
Gain-Bandwidth*	$T_J = 25^{\circ}\text{C}$ , $A_V = 0\text{dB}$	1	3		1	3		MHz
DC Transconductance*§	$T_J = 25^{\circ}\text{C}$ , $30\text{k}\Omega \leq R_L \leq 1\text{M}\Omega$	1.7	2.3		1.7	2.3		mS
<b>P.W.M. Comparator</b> ( $R_T = 2\text{k}\Omega$ , $C_T = 0.01\text{ mfd}$ )								
Minimum Duty Cycle	$V_{COMP} = 0.5\text{V}$			0			0	%
Maximum Duty Cycle	$V_{COMP} = 3.8\text{V}$	45			45			%
<b>Current Limit Amplifier</b> (Unless otherwise specified, $\text{Pin } 5 = 0\text{V}$ )								
Input Offset Voltage	$T_J = 25^{\circ}\text{C}$ , E/A Set for Maximum Output	190	200	210	180	200	220	mV
	Over Operating Temperature Range	180		220	170		230	mV
Input Bias Current			-1	-10		-1	-10	$\mu\text{A}$
Common Mode Rejection Ratio	$V_{(\text{pin } 5)} = -0.3\text{V}$ to $+5.5\text{V}$	50	60		50	60		dB
Power Supply Rejection Ratio	$V_{IN} = 10$ to $40\text{V}$	50	60		50	60		dB
Output Swing (Note 1)	Minimum Total Range	5.0		0.5	5.0		0.5	V
Open-Loop Voltage Gain	$\Delta V_O = 1$ to $4\text{V}$ , $R_L \geq 10\text{M}\Omega$	70	80		70	80		dB
Delay Time*	$\text{Pin } 4$ to $\text{Pin } 9$ , $\Delta V_{IN} = 300\text{mV}$		300			300		ns
<b>Output Section</b> (Each Output)								
Collector Emitter Voltage	$I_C = 100\mu\text{A}$	60	80		60	80		V
Collector Leakage Current	$V_{CE} = 50\text{V}$		.1	20		.1	20	$\mu\text{A}$

\* These parameters are ensured by design but not 100% tested in production.

§ DC transconductance ( $gm$ ) relates to DC open-loop voltage gain according to the following equation:  $A_V = gmR_L$  where  $R_L$  is the resistance from pin 9 to the common mode voltage.

The minimum  $gm$  specification is used to calculate minimum  $A_V$  when the error amplifier output is loaded.

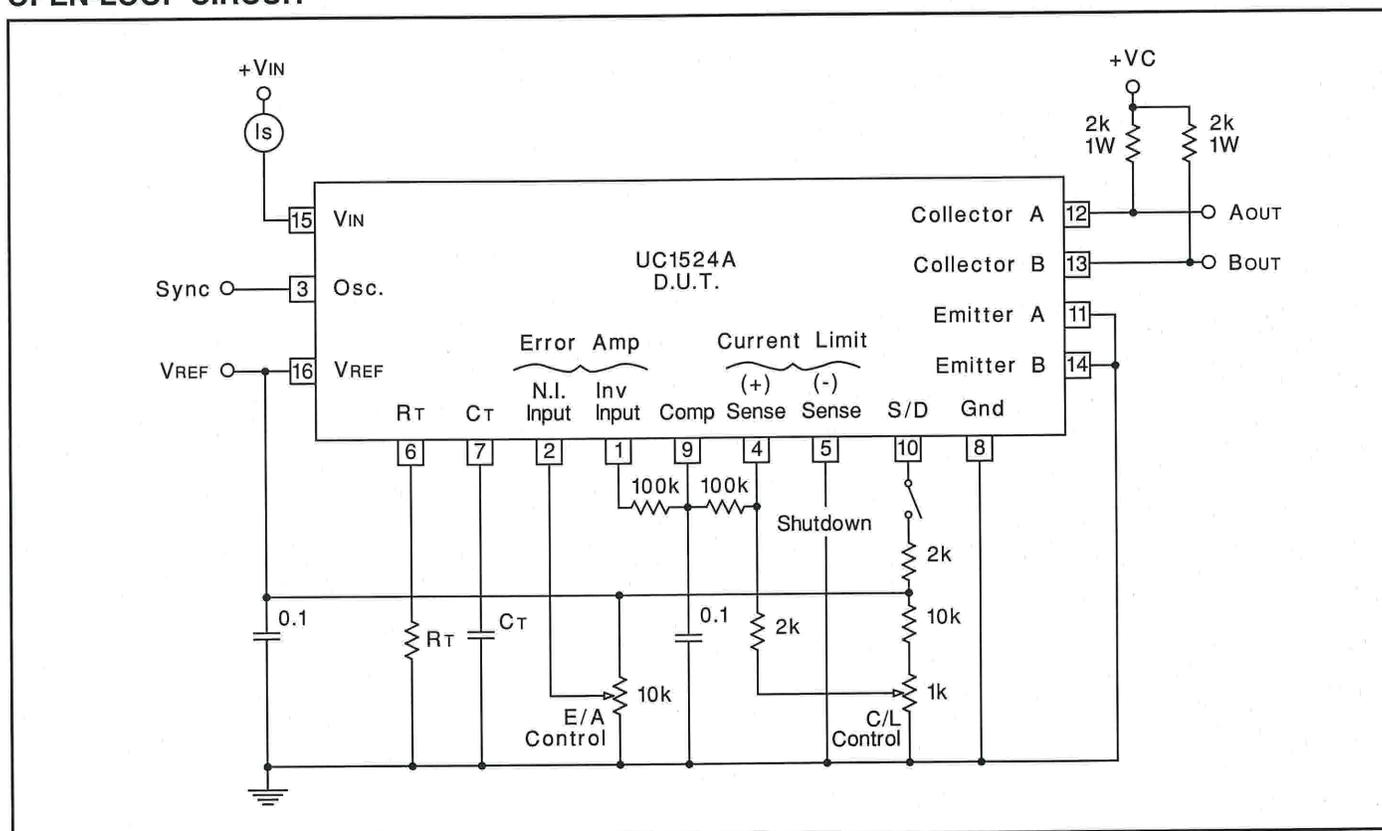
Note 1: Min Limit applies to output high level, max limit applies to output low level.

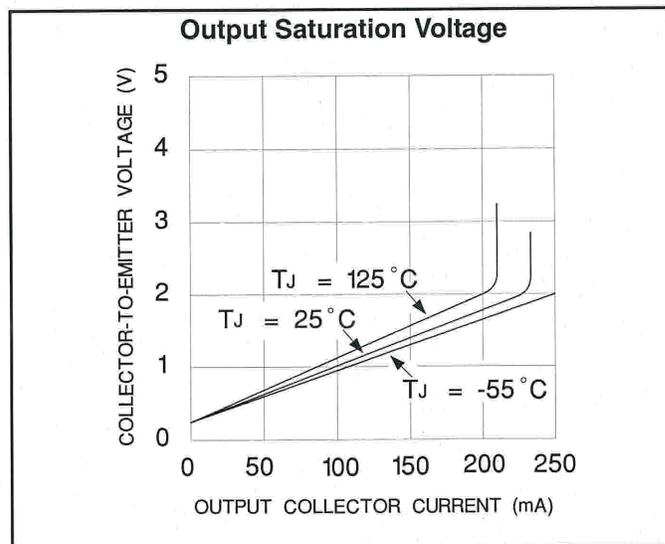
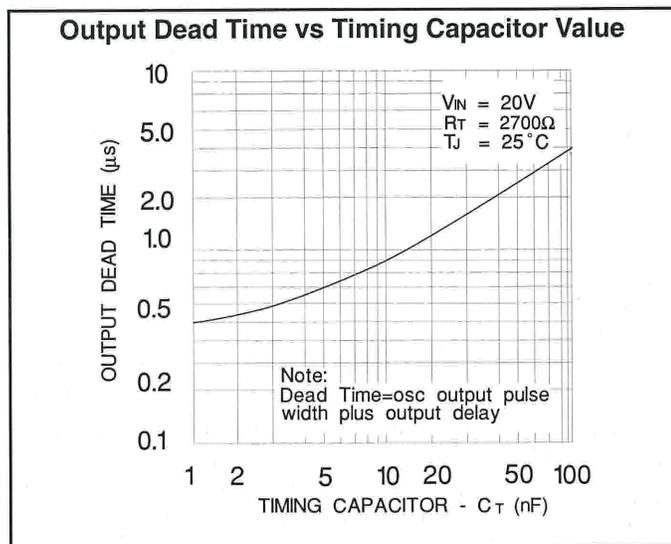
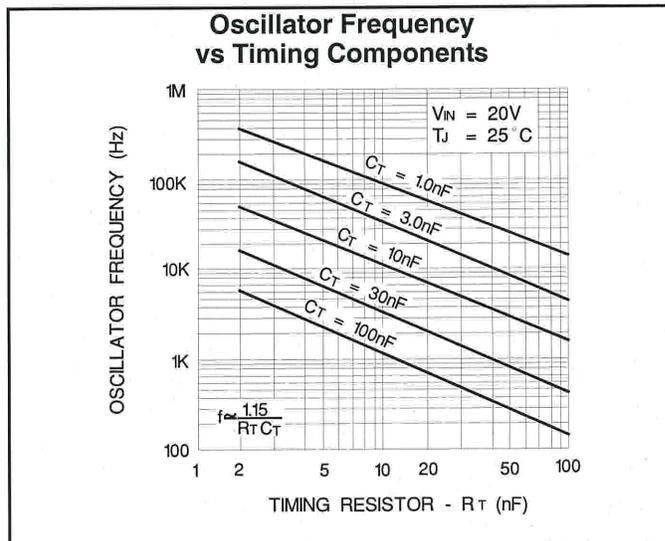
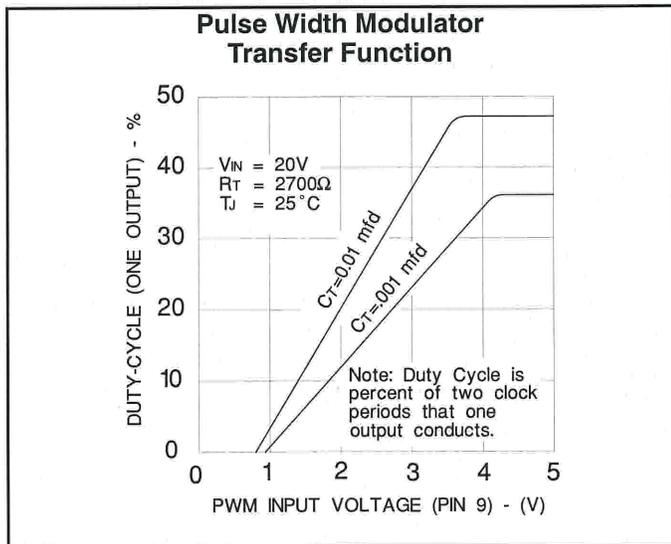
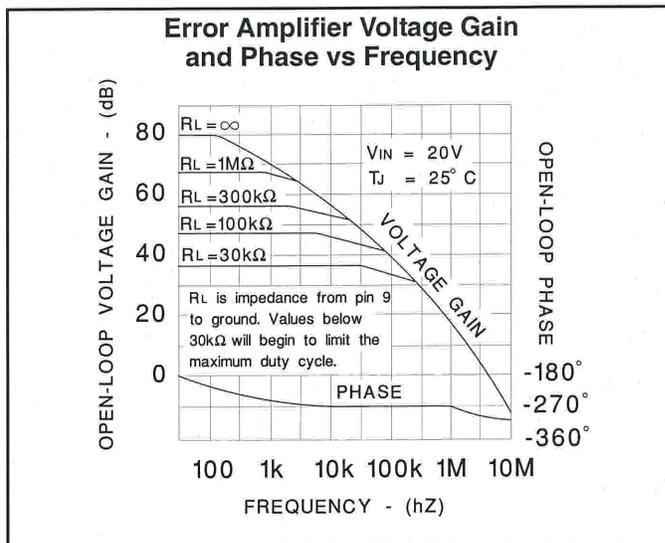
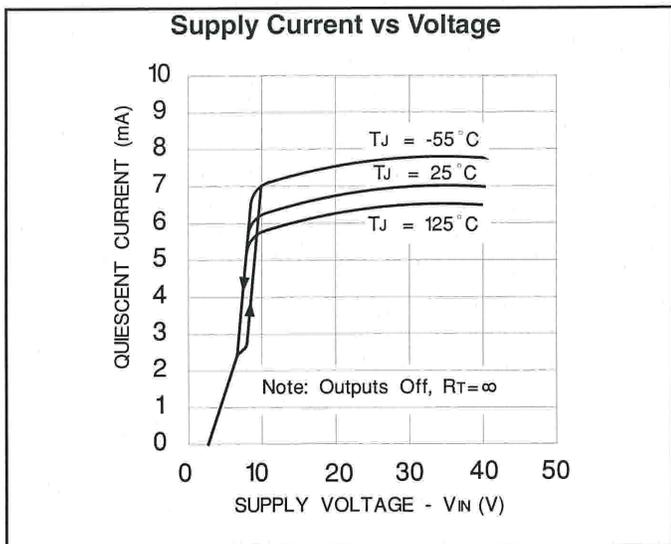
**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for  $T_A = -55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  for the UC1524A,  $-40^{\circ}$  to  $+85^{\circ}\text{C}$  for the UC2524A, and  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$  for the UC3524A;  $V_{IN} = V_C = 20\text{V}$ .  $T_A = T_J$ .

PARAMETER	TEST CONDITIONS	UC1524A / UC2524A			UC3524A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>Output Section ( cont.) (Each Output)</b>								
Saturation Voltage	$I_C = 20\text{mA}$ $I_C = 200\text{mA}$		.2 1	.4 2.2		.2 1	.4 2.2	V V
Emitter Output Voltage	$I_E = 50\text{mA}$	17	18		17	18		V
Rise Time*	$T_J = 25^{\circ}\text{C}$ , $R = 2\text{k}\Omega$		120	400		120	400	ns
Fall Time*	$T_J = 25^{\circ}\text{C}$ , $R = 2\text{k}\Omega$		25	200		25	200	ns
Comparator Delay*	$T_J = 25^{\circ}\text{C}$ , Pin 9 to output		300			300		ns
Shutdown Delay*	$T_J = 25^{\circ}\text{C}$ , Pin 10 to output		200			200		ns
Shutdown Threshold	$T_J = 25^{\circ}\text{C}$ , $R_C = 2\text{k}\Omega$	0.6	.7	1.0	0.6	.7	1.0	V
S/D Threshold Over Temp.	Over Operating Temperature Range	0.4		1.2	0.4		1.0	V
Thermal Shutdown*			165			165		$^{\circ}\text{C}$

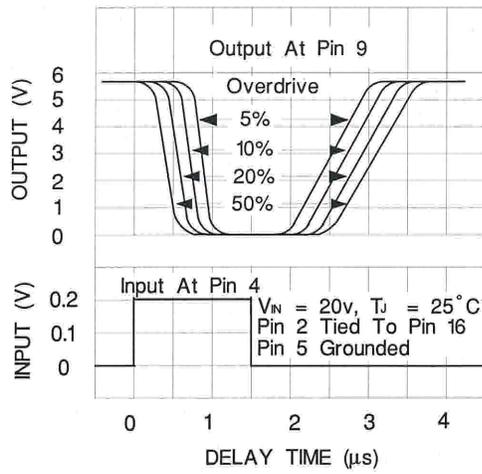
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### OPEN-LOOP CIRCUIT

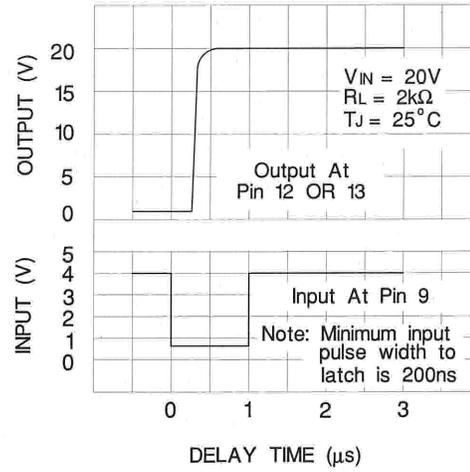




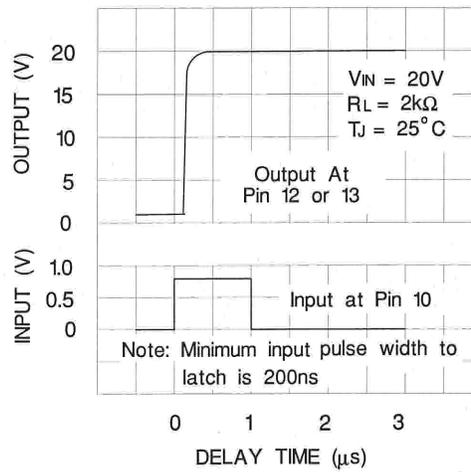
**Current Limit Amplifier Delay**



**Shutdown Delay From PWM Comparator - Pin 9**



**Turn-Off Delay From Shutdown - Pin 10**



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8764502EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8764502EA	<a href="#">Samples</a>
UC1524AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	UC1524AJ	<a href="#">Samples</a>
UC1524AJ883B	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	UC1524AJ/883B	<a href="#">Samples</a>
UC1524AL	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	UC1524AL	<a href="#">Samples</a>
UC1524AL883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	UC1524AL/ 883B	<a href="#">Samples</a>
UC2524ADW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2524ADW	<a href="#">Samples</a>
UC2524ADWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2524ADW	<a href="#">Samples</a>
UC2524ADWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2524ADW	<a href="#">Samples</a>
UC2524AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-40 to 85	UC2524AJ	<a href="#">Samples</a>
UC2524AN	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UC2524AN	<a href="#">Samples</a>
UC2524ANG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UC2524AN	<a href="#">Samples</a>
UC3524ADW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3524ADW	<a href="#">Samples</a>
UC3524ADWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3524ADW	<a href="#">Samples</a>
UC3524ADWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3524ADW	<a href="#">Samples</a>
UC3524ADWTRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3524ADW	<a href="#">Samples</a>
UC3524AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	0 to 70	UC3524AJ	<a href="#">Samples</a>
UC3524AN	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3524AN	<a href="#">Samples</a>
UC3524ANG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3524AN	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF UC1524A, UC2524A, UC2524AM, UC3524A, UC3524AM :**

● Catalog: [UC3524A](#), [UC2524A](#), [UC3524AM](#), [UC3524A](#)

● Military: [UC2524AM](#), [UC1524A](#), [UC1524A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2524ADWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
UC3524ADWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

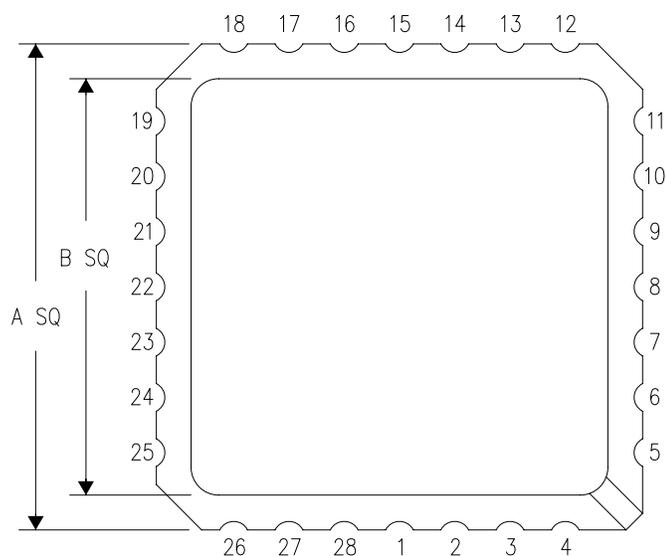

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2524ADWTR	SOIC	DW	16	2000	367.0	367.0	38.0
UC3524ADWTR	SOIC	DW	16	2000	367.0	367.0	38.0

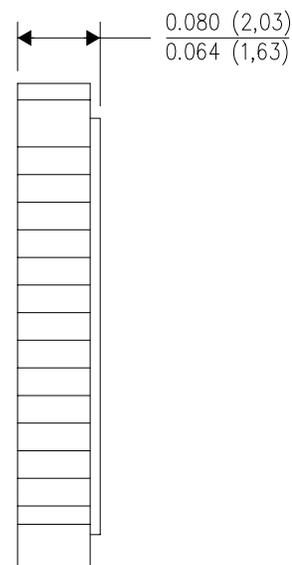
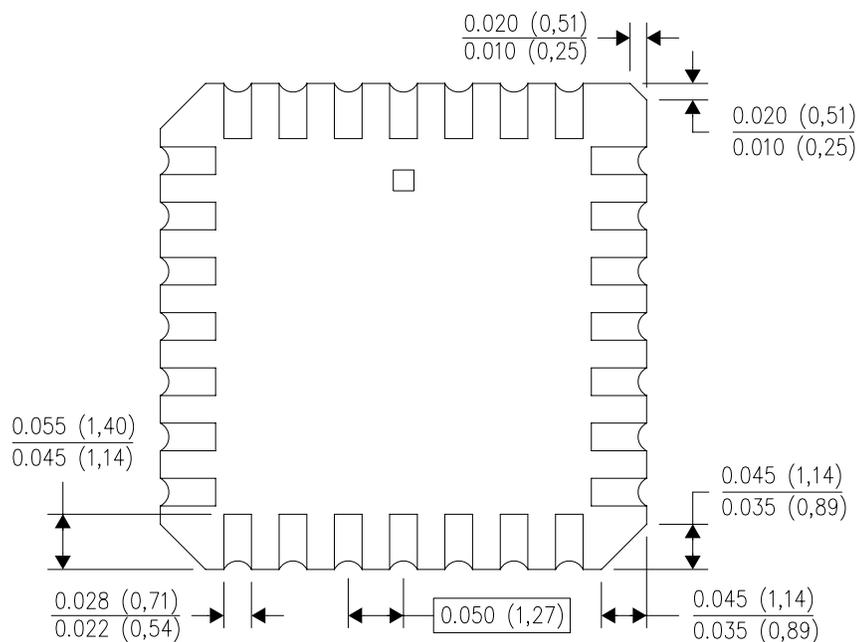
FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



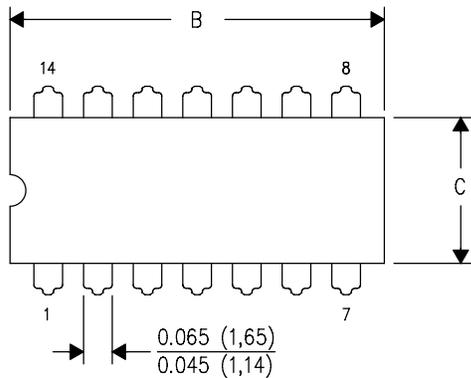
4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

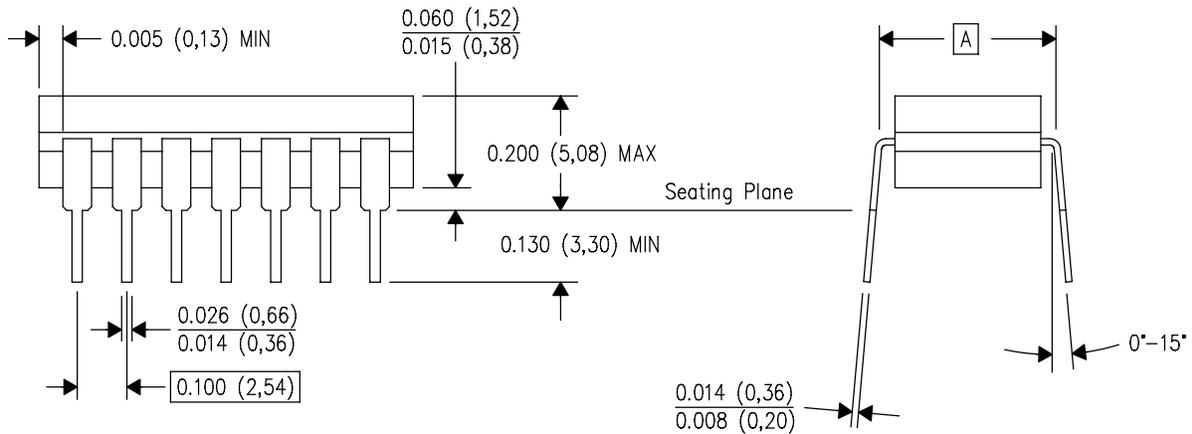
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



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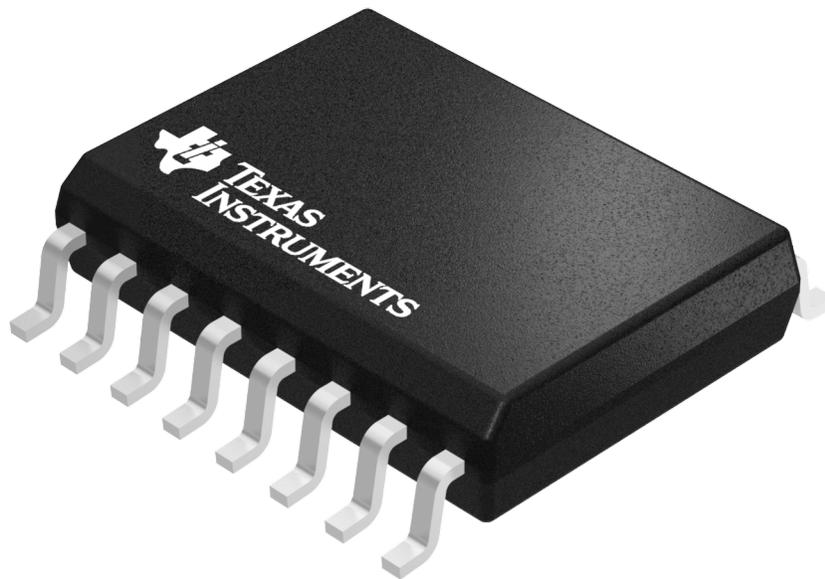
- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## GENERIC PACKAGE VIEW

DW 16

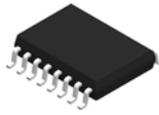
**SOIC - 2.65 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

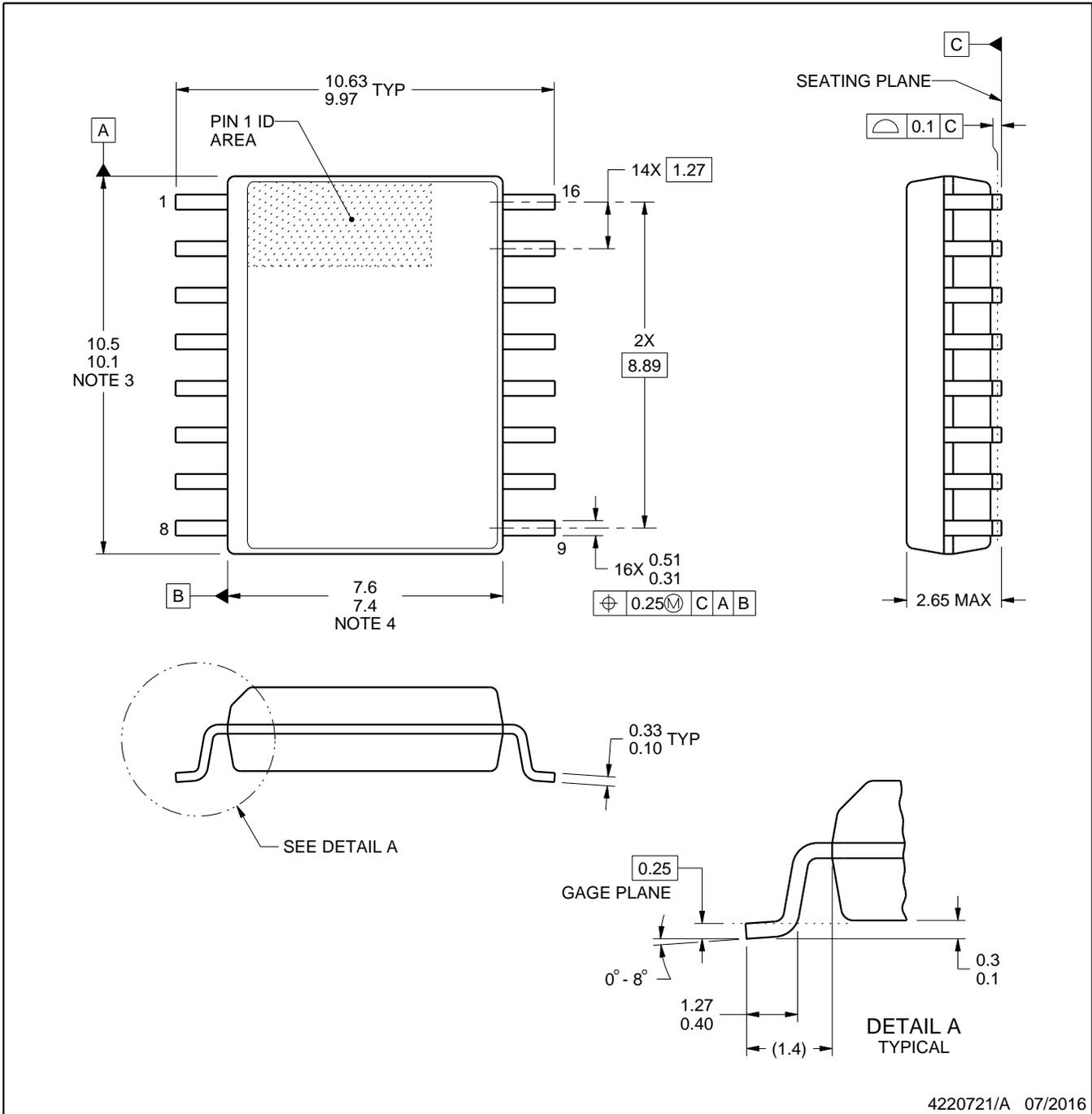
4040000-2/H



# DW0016A

# PACKAGE OUTLINE SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

### NOTES:

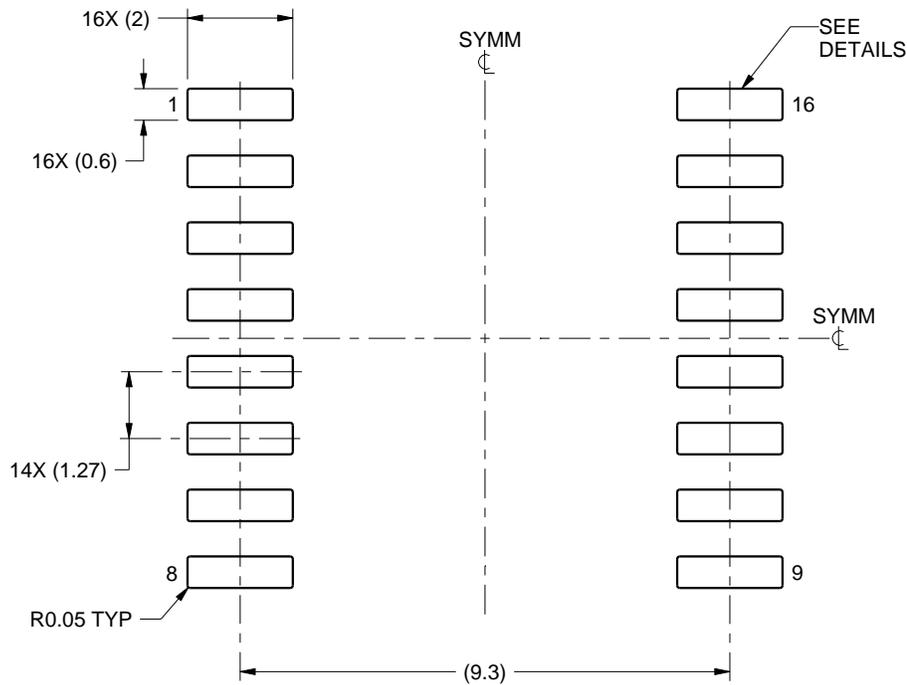
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

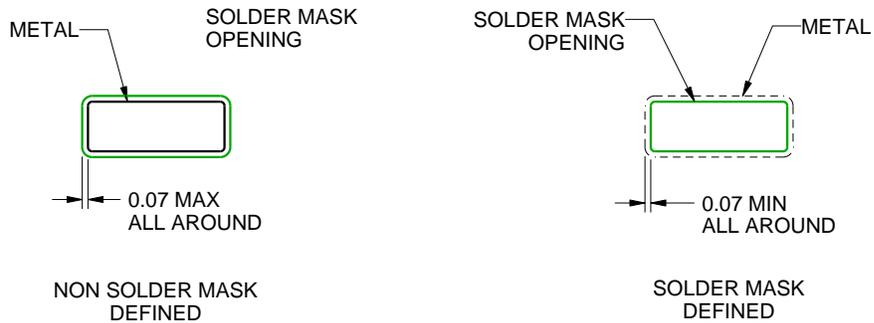
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:7X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

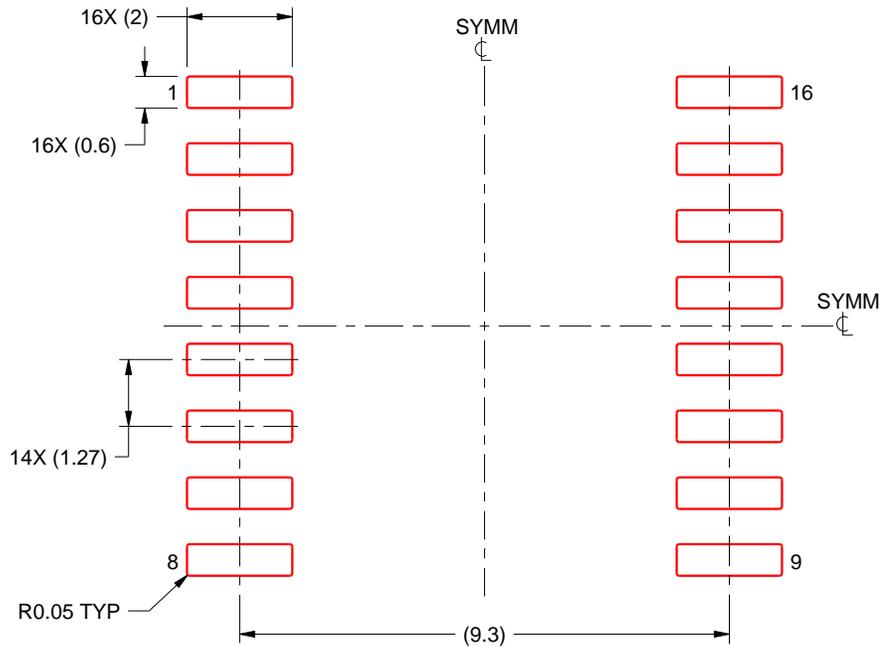
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

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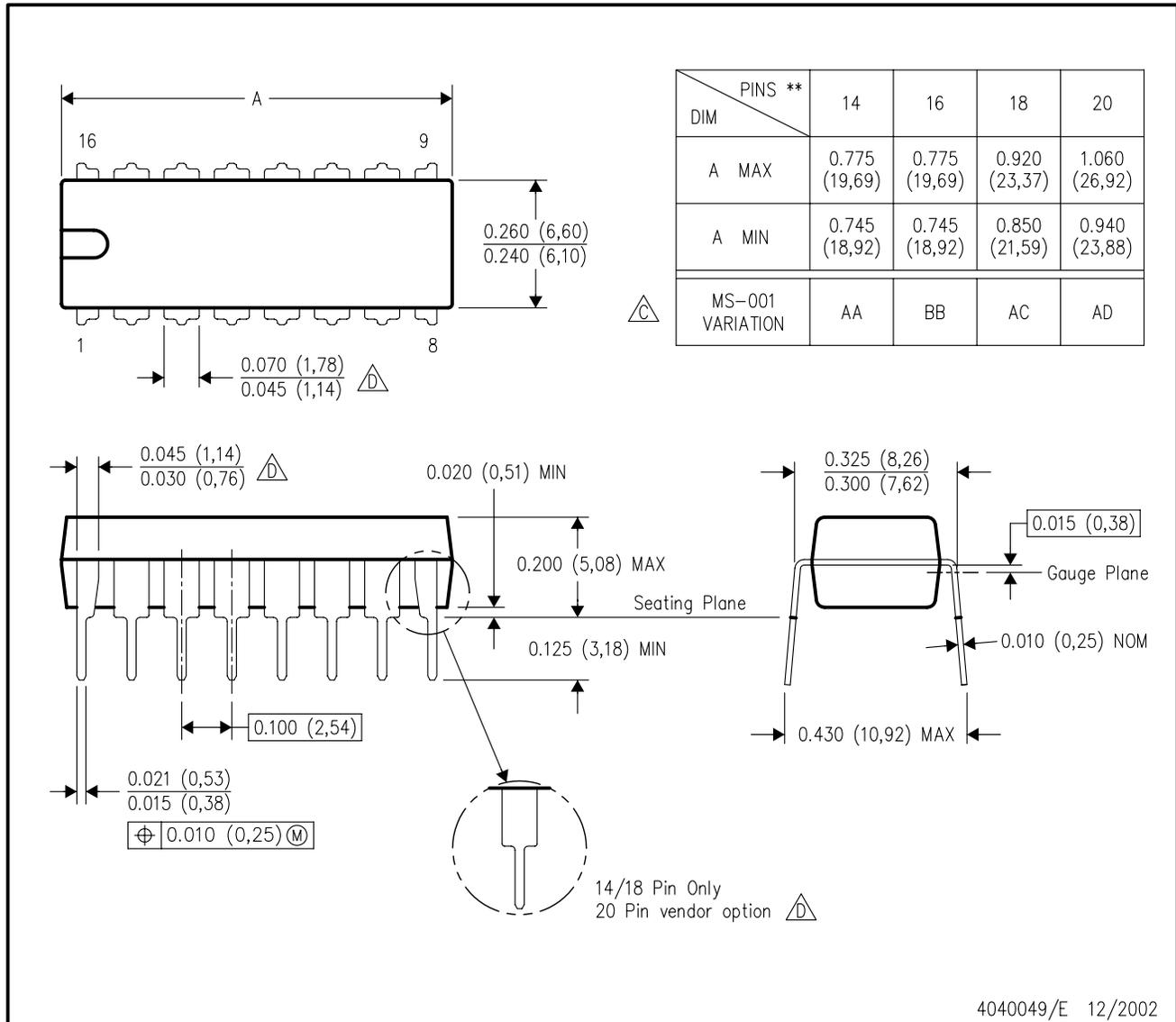
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

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