

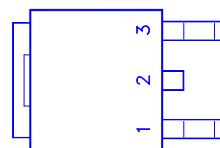
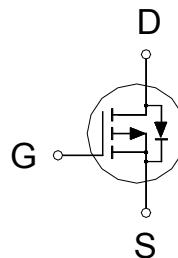
NIKO-SEM
**P-Channel Logic Level Enhancement
Mode Field Effect Transistor**
P4004ED

TO-252(DPAK)

Halogen-Free & Lead-Free

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-40V	40m Ω	-21A

**ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)**

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	-21	A
		-17	
Pulsed Drain Current ¹	I_{DM}	-70	
Avalanche Current	I_{AS}	-27	
Avalanche Energy ²	E_{AS}	36	mJ
Power Dissipation	P_D	30	W
		20	
Junction & Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$		4.1	°C / W
Junction-to-Ambient	$R_{\theta JA}$		40	°C / W

¹Pulse width limited by maximum junction temperature.² $V_{DD} = -20\text{V}$. Starting $T_J = 25^\circ\text{C}$.**ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, Unless Otherwise Noted)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$	-40			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	-2.0	-2.5	-3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$			± 250	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -32\text{V}, V_{GS} = 0\text{V}$			1	μA
		$V_{DS} = -30\text{V}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$			10	
On-State Drain Current ¹	$I_{D(\text{ON})}$	$V_{DS} = -5\text{V}, V_{GS} = -10\text{V}$	-70			A

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Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = -5V, I_D = -8A$		65	73	$m\Omega$
		$V_{GS} = -7V, I_D = -8A$		35	50	
		$V_{GS} = -10V, I_D = -10A$		30	40	
Forward Transconductance ¹	g_{fs}	$V_{DS} = -10V, I_D = -10A$		20		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = -20V, f = 1MHz$		1090		pF
Output Capacitance	C_{oss}			175		
Reverse Transfer Capacitance	C_{rss}			91		
Total Gate Charge ²	$Q_g(V_{GS} = -10V)$	$V_{DS} = 0.5V_{(BR)DSS}, I_D = -18A$		17		nC
Total Gate Charge ²	$Q_g(V_{GS} = -4.5V)$			8.5		
Gate-Source Charge ²	Q_{gs}			5.5		
Gate-Drain Charge ²	Q_{gd}			3		
Gate Resistance	R_g	$V_{GS} = 0V, V_{DS} = 0V, f = 1MHz$		4.95		Ω
Turn-On Delay Time ²	$t_{d(on)}$	$V_{DS} = -20V, R_L = 2\Omega$		6		nS
Rise Time ²	t_r			16		
Turn-Off Delay Time ²	$t_{d(off)}$			26		
Fall Time ²	t_f			10		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_J = 25^\circ C$)						
Continuous Current	I_S				-21	A
Forward Voltage ¹	V_{SD}	$I_F = -1A, V_{GS} = 0V$			-1	V
Reverse Recovery Time	t_{rr}	$I_F = -10 A, dI_F/dt = 100A / \mu S$		15.5		nS
Reverse Recovery Charge	Q_{rr}			7.9		nC

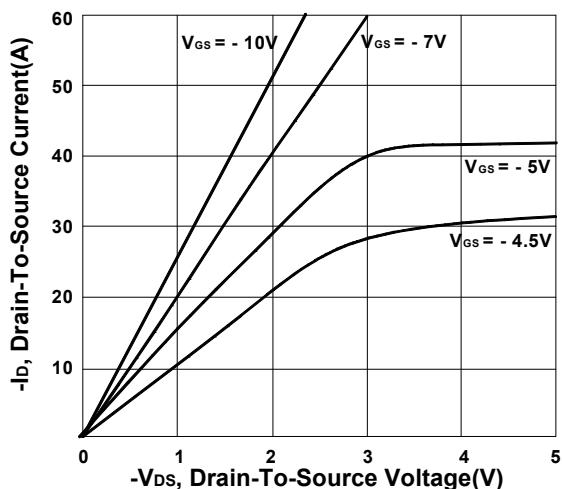
¹Pulse test : Pulse Width $\leq 300 \mu sec$, Duty Cycle $\leq 2\%$.²Independent of operating temperature.

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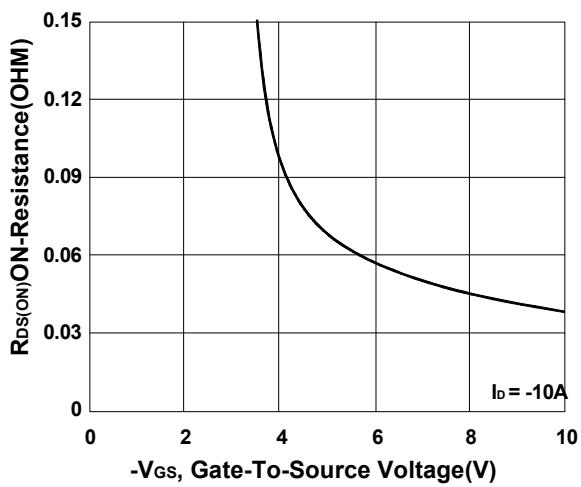
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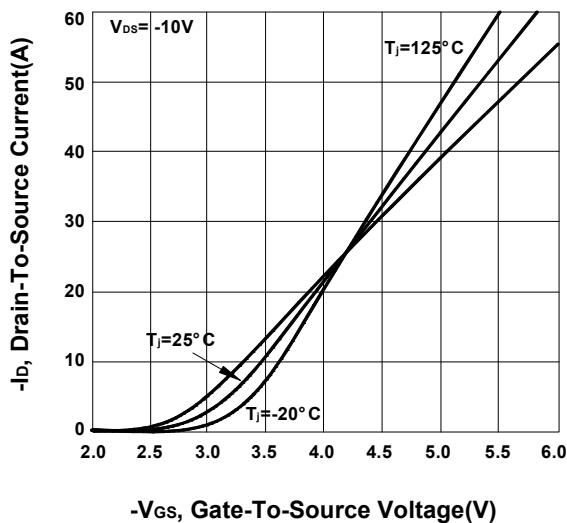
Output Characteristics



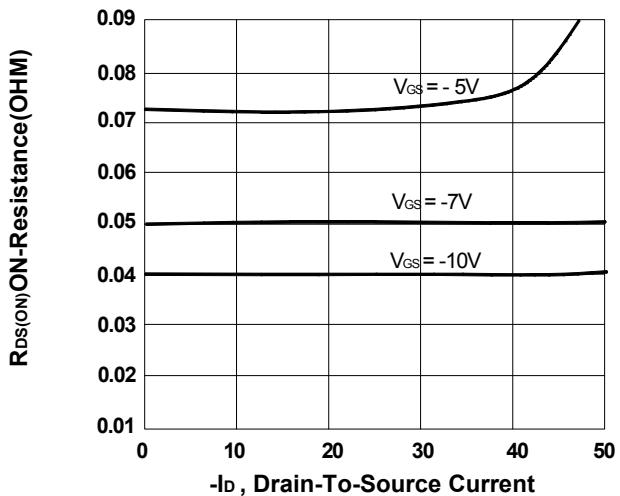
On-Resistance VS Gate-To-Source



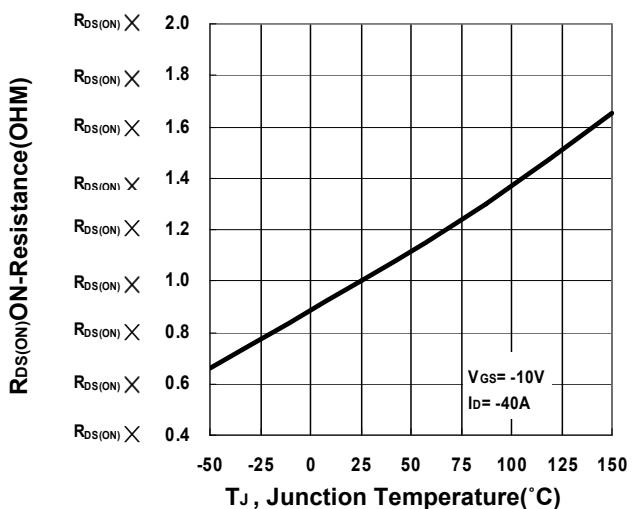
Transfer Characteristics



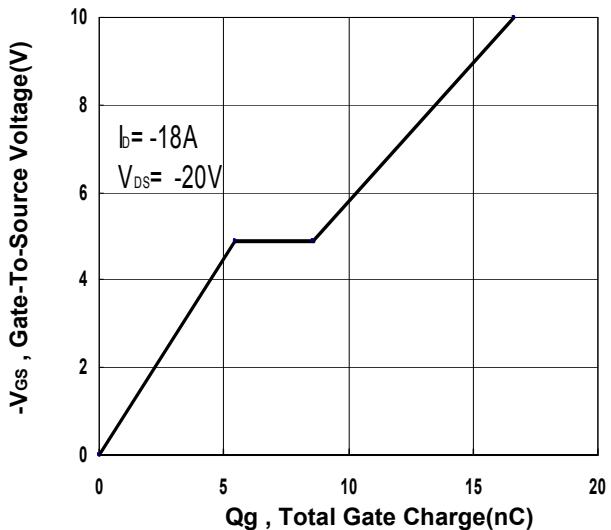
On-Resistance VS Drain Current



On-Resistance VS Temperature



Gate charge Characteristics

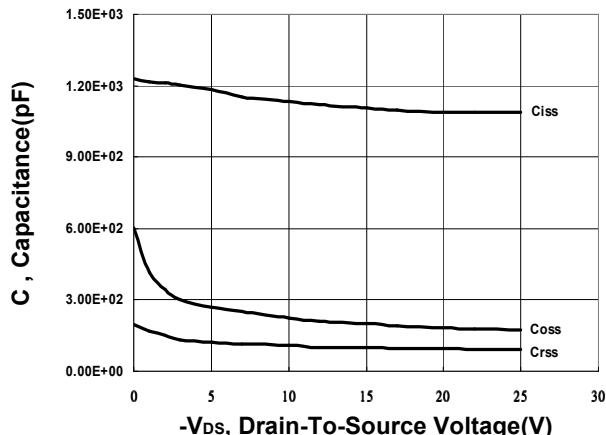


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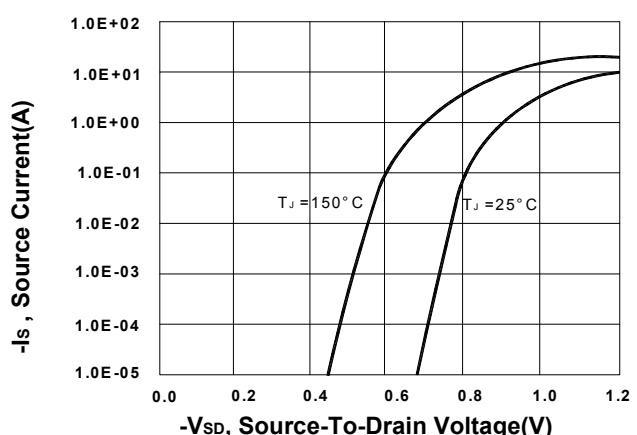
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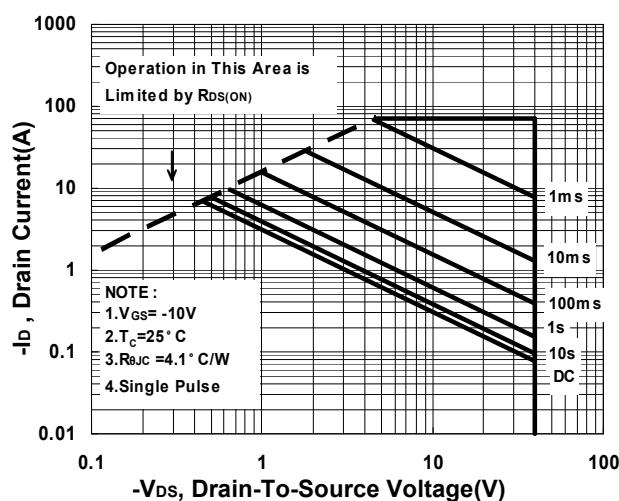
Capacitance Characteristic



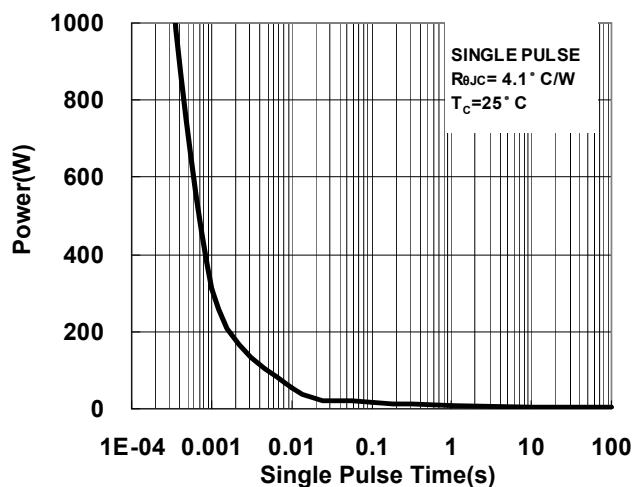
Body Diode Forward Voltage VS Source current



Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve

