

## SN74AUP1T17 Low Power, 1.8/2.5/3.3-V Input, 3.3-V CMOS Output, Single Schmitt-Trigger Buffer Gate

### 1 Features

- Single-Supply Voltage Translator
- Output Level Up to Supply  $V_{CC}$  CMOS Level
  - 1.8 V to 3.3 V (at  $V_{CC} = 3.3$  V)
  - 2.5 V to 3.3 V (at  $V_{CC} = 3.3$  V)
  - 1.8 V to 2.5 V (at  $V_{CC} = 2.5$  V)
  - 3.3 V to 2.5 V (at  $V_{CC} = 2.5$  V)
- Schmitt-Trigger Inputs Reject Input Noise and Provide Better Output Signal Integrity
- $I_{off}$  Supports Partial Power Down ( $V_{CC} = 0$  V)
- Very Low Static Power Consumption: 0.1  $\mu$ A
- Very Low Dynamic Power Consumption: 0.9  $\mu$ A
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- Pb-Free Packages Available: SC-70 (DCK) 2 x 2.1 x 0.65 mm (Height 1.1 mm)
- More Gate Options Available at [www.ti.com/littlelogic](http://www.ti.com/littlelogic)
- ESD Performance Tested Per JESD 22
  - 2000-V Human Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

### 2 Applications

- AV Receivers
- Audio Dock: Portable
- Blu-ray Players and Home Theaters
- MP3 Players and Recorders
- Personal Digital Assistant (PDA)
- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Solid State Drive (SSD): Client and Enterprise
- TV: LCD/Digital and High-Definition (HDTV)
- Tablet: Enterprise
- Video Analytics: Servers
- Wireless Headsets, Keyboards, and Mice

### 3 Description

The SN74AUP1T17 performs the Boolean function  $Y = A$  with designation for logic-level translation applications with output referenced to supply  $V_{CC}$ .

AUP technology is the industry's lowest-power logic technology designed for use in extending battery-life in operating. All input levels that accept 1.8-V LVCMOS signals, while operating from either a single 3.3-V or 2.5-V  $V_{CC}$  supply. This product also maintains excellent signal integrity (see [Figure 4](#) and [Figure 1](#)).

The wide  $V_{CC}$  range of 2.3 V to 3.6 V allows the possibility of switching output level to connect to external controllers or processors.

Schmitt-trigger inputs ( $\Delta V_T = 210$  mV between positive and negative input transitions) offer improved noise immunity during switching transitions, which is especially useful on analog mixed-mode designs. Schmitt-trigger inputs reject input noise, ensure integrity of output signals, and allow for slow input signal transition.

$I_{off}$  is a feature that allows for powered-down conditions ( $V_{CC} = 0$  V) and is important in portable and mobile applications. When  $V_{CC} = 0$  V, signals in the range from 0 V to 3.6 V can be applied to the inputs and outputs of the device. No damage occurs to the device under these conditions.

The SN74AUP1T17 is designed with optimized current-drive capability of 4 mA to reduce line reflections, overshoot, and undershoot caused by high-drive outputs.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AUP1T17DCK	SC70 (5)	2.00 mm x 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Simplified Schematic



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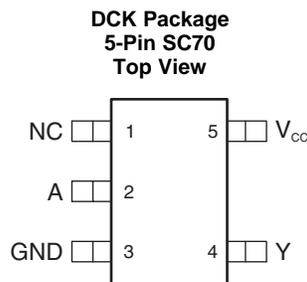
## 4 Revision History

### Changes from Original (April 2010) to Revision A

**Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ..... **1**

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
NC	1	—	Not connected
A	2	I	Input
GND	3	—	Ground
Y	4	O	Output
V <sub>CC</sub>	5	—	Power terminal

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage	−0.5	4.6	V	
V <sub>I</sub>	Input voltage <sup>(2)</sup>	−0.5	4.6	V	
V <sub>O</sub>	Voltage applied to any output in the high-impedance or power-off state <sup>(2)</sup>	−0.5	4.6	V	
V <sub>O</sub>	Output voltage in the high or low state <sup>(2)</sup>	−0.5	V <sub>CC</sub> + 0.5	V	
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		−50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		−50	mA
I <sub>O</sub>	Continuous output current			±20	mA
	Continuous current through V <sub>CC</sub> or GND			±50	mA
T <sub>stg</sub>	Storage temperature	−65	150	°C	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2.3	3.6	V
V <sub>I</sub>	Input voltage	0	3.6	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2.3 V	-3.1	mA
		V <sub>CC</sub> = 3 V	-4	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2.3 V	3.1	mA
		V <sub>CC</sub> = 3 V	4	
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See the TI application report *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SN74AUP1T17		UNIT
	DCK (SC70)		
	5 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance		280 °C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

### 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V <sub>T+</sub> Positive-going input threshold voltage		2.3 V to 2.7 V	0.6		1.1	0.6	1.1	V
		3 V to 3.6 V	0.75		1.16	0.75	1.19	
V <sub>T-</sub> Negative-going input threshold voltage		2.3 V to 2.7 V	0.35		0.6	0.35	0.6	V
		3 V to 3.6 V	0.5		0.85	0.5	0.85	
ΔV <sub>T</sub> Hysteresis (V <sub>T+</sub> - V <sub>T-</sub> )		2.3 V to 2.7 V	0.23		0.6	0.1	0.6	V
		3 V to 3.6 V	0.25		0.56	0.15	0.56	
V <sub>OH</sub>	I <sub>OH</sub> = -20 μA	2.3 V to 3.6 V	V <sub>CC</sub> - 0.1			V <sub>CC</sub> - 0.1		V
	I <sub>OH</sub> = -2.3 mA	2.3 V	2.05			1.97		
	I <sub>OH</sub> = -3.1 mA		1.9			1.85		
	I <sub>OH</sub> = -2.7 mA	3 V	2.72			2.67		
	I <sub>OH</sub> = -4 mA		2.6			2.55		
V <sub>OL</sub>	I <sub>OL</sub> = 20 μA	2.3 V to 3.6 V				0.1		V
	I <sub>OL</sub> = 2.3 mA	2.3 V				0.31		
	I <sub>OL</sub> = 3.1 mA					0.44		
	I <sub>OL</sub> = 2.7 mA	3 V				0.31		
	I <sub>OL</sub> = 4 mA					0.44		
I <sub>I</sub>	All inputs	V <sub>I</sub> = 3.6 V or GND	0 V to 3.6 V			0.1		μA
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V	0 V			0.1		μA
ΔI <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 3.6 V	0 V to 0.2 V			0.2		μA
I <sub>CC</sub>		V <sub>I</sub> = 3.6 V or GND, I <sub>O</sub> = 0	2.3 V to 3.6 V			0.5		μA

## Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = –40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
ΔI <sub>CC</sub>	One input at 0.3 V or 1.1 V, Other inputs at 0 or V <sub>CC</sub> , I <sub>O</sub> = 0	2.3 V to 2.7 V					4	μA
	One input at 0.45 V or 1.2 V, Other inputs at 0 or V <sub>CC</sub> , I <sub>O</sub> = 0	3 V to 3.6 V					12	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		1.5				pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V		3				pF

### 6.6 Switching Characteristics, V<sub>CC</sub> = 2.5 V and V<sub>I</sub> = 1.8 V

over recommended operating free-air temperature range, V<sub>CC</sub> = 2.5 V ± 0.2 V, V<sub>I</sub> = 1.8 V ± 0.15 V (unless otherwise noted)  
(see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C <sub>L</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	5 pF	1.8	2.3	2.9	0.5	6.8	ns
			10 pF	2.3	2.8	3.4	1	7.9	
			15 pF	2.6	3.1	3.8	1	8.7	
			30 pF	3.8	4.4	5.1	1.5	10.8	

### 6.7 Switching Characteristics, V<sub>CC</sub> = 2.5 V and V<sub>I</sub> = 2.5 V

over recommended operating free-air temperature range, V<sub>CC</sub> = 2.5 V ± 0.2 V, V<sub>I</sub> = 2.5 V ± 0.2 V (unless otherwise noted)  
(see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C <sub>L</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	5 pF	1.8	2.3	3.1	0.5	6	ns
			10 pF	2.2	2.8	3.5	1	7.1	
			15 pF	2.6	3.2	5.2	1	7.9	
			30 pF	3.7	4.4	5.2	1.5	10	

### 6.8 Switching Characteristics, V<sub>CC</sub> = 2.5 V and V<sub>I</sub> = 3.3 V

over recommended operating free-air temperature range, V<sub>CC</sub> = 2.5 V ± 0.2 V, V<sub>I</sub> = 3.3 V ± 0.3 V (unless otherwise noted)  
(see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C <sub>L</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	5 pF	2	2.7	3.5	0.5	5.5	ns
			10 pF	2.4	3.1	3.9	1	6.5	
			15 pF	2.8	3.5	4.3	1	7.4	
			30 pF	4	4.7	5.5	1.5	9.5	

### 6.9 Switching Characteristics, $V_{CC} = 3.3\text{ V}$ and $V_I = 1.8\text{ V}$

over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_I = 1.8\text{ V} \pm 0.15\text{ V}$  (unless otherwise noted) (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A	Y	5 pF	1.6	2	2.5	0.5	8	ns
			10 pF	2	2.4	2.9	1	8.5	
			15 pF	2.3	2.8	3.3	1	9.1	
			30 pF	3.4	3.9	4.4	1.5	9.8	

### 6.10 Switching Characteristics, $V_{CC} = 3.3\text{ V}$ and $V_I = 2.5\text{ V}$

over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_I = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A	Y	5 pF	1.6	1.9	2.4	0.5	5.3	ns
			10 pF	2	2.3	2.7	1	6.1	
			15 pF	2.3	2.7	3.1	1	6.8	
			30 pF	3.4	3.8	4.2	1.5	8.5	

### 6.11 Switching Characteristics, $V_{CC} = 3.3\text{ V}$ and $V_I = 3.3\text{ V}$

over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_I = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see [Figure 2](#))

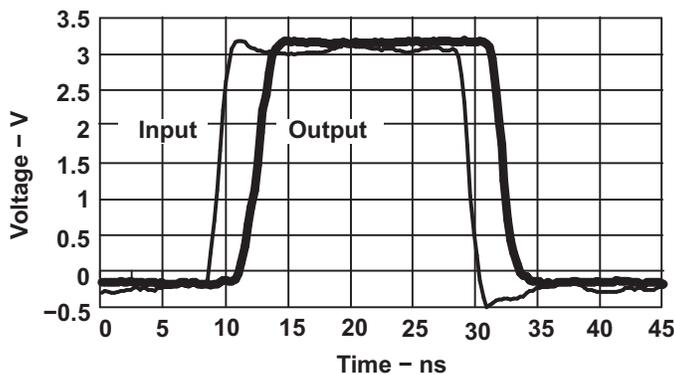
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A	Y	5 pF	1.6	2.1	2.7	0.5	4.7	ns
			10 pF	2	2.4	3	1	5.7	
			15 pF	2.3	2.7	3.3	1	6.2	
			30 pF	3.4	3.8	4.4	1.5	7.8	

### 6.12 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
		TYP	TYP	
$C_{pd}$ Power dissipation capacitance	$f = 10\text{ MHz}$	4	5	pF

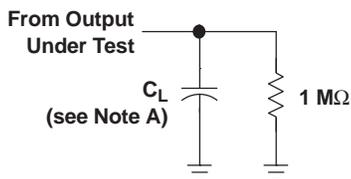
### 6.13 Typical Characteristics



AUP1G08 data at  $C_L = 15 \text{ pF}$

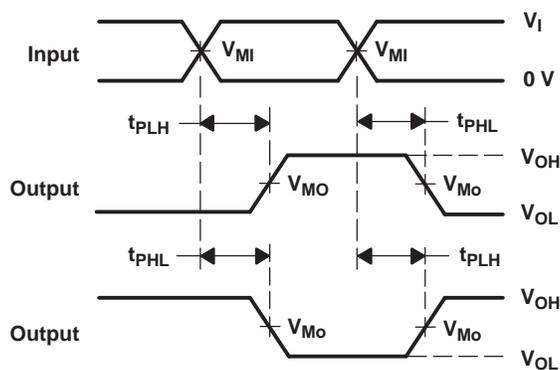
Figure 1. Switching Characteristics at 25 MHz

## 7 Parameter Measurement Information



LOAD CIRCUIT

	$V_{CC} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$
$C_L$	5, 10, 15, 30 pF	5, 10, 15, 30 pF
$V_{MI}$	$V_I/2$	$V_I/2$
$V_{MO}$	$V_{CC}/2$	$V_{CC}/2$



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \text{ }\Omega$ , slew rate  $\geq 1 \text{ V/ns}$ .  
 C. The outputs are measured one at a time, with one transition per measurement.  
 D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 2. Load Circuit and Voltage Waveforms

## 8 Detailed Description

### 8.1 Overview

The SN74AUP1T17 device contains one Schmitt trigger buffer and performs the Boolean function  $Y = A$ . The device functions as an independent buffer, but because of Schmitt action, it will have different input threshold levels for a positive-going ( $V_{T+}$ ) and negative-going signals.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

The distinguishing feature of the SN74AUP1T17 versus its standard-logic counterpart, the SN74AUP1G17, is the lowered switching input threshold. The SN74AUP1T17 will switch to a high output at a lower voltage threshold, which allows up-translation from signals that may not reach  $V_{CC}$  levels.

The  $I_{OFF}$  feature prevents the outputs from sinking current when  $V_{CC} = 0$  V, providing extra isolation in systems where not all modules are powered simultaneously.

### 8.4 Device Functional Modes

[Table 1](#) lists the functional modes for SN74AUP1T17.

**Table 1. Function Table**

INPUT A	OUTPUT Y
H	H
L	L

## 9 Application and Implementation

### NOTE

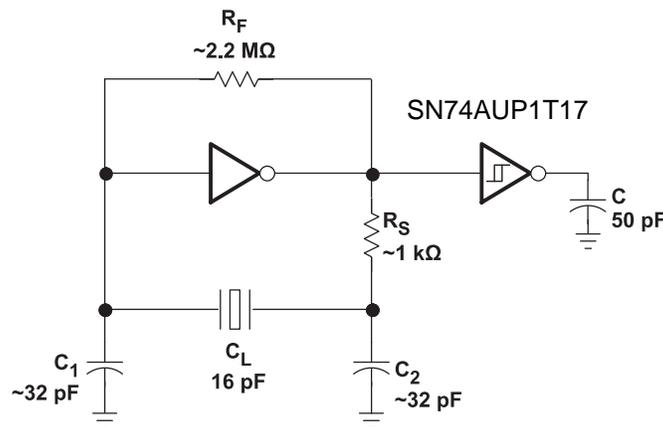
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The SN74AUP1T17 is a low-power CMOS device that can be used for a multitude of buffer type functions where the input is slow or noisy. The inputs are 5.5-V tolerant allowing it to translate down to  $V_{CC}$ . In addition, the device can translate a signal up to  $V_{CC}$  when the input is at least  $V_{T+}$  (max).

### 9.2 Typical Application

This application is for a low-cost oscillator. The SN74AUP1T17 at the output cleans up the noise from the clock generator so that it can be used in the system.



**Figure 3. Low-Cost Oscillator**

#### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

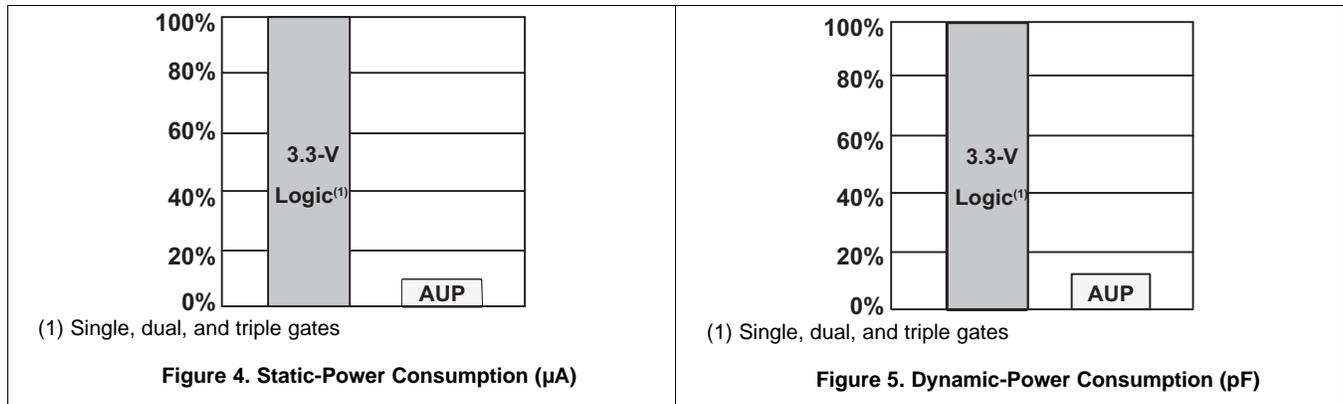
#### 9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
  - Specified high and low levels. See ( $V_{T+}$  and  $V_{T-}$ ) in the [Recommended Operating Conditions](#) table.
  - Inputs are overvoltage tolerant allowing them to go as high as ( $V_I$  max) in the [Recommended Operating Conditions](#) table at any valid  $V_{CC}$ .
2. Recommend Output Conditions
  - Load currents should not exceed ( $I_O$  max) per output and should not exceed (continuous current through  $V_{CC}$  or GND) total current for the part. These limits are located in the [Absolute Maximum Ratings](#) table.
  - Outputs should not be pulled above  $V_{CC}$ .

## Typical Application (continued)

### 9.2.3 Application Curves

Figure 4 and Figure 5 show the power consumption with the AUP family.



## 10 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the [Recommended Operating Conditions](#) table.

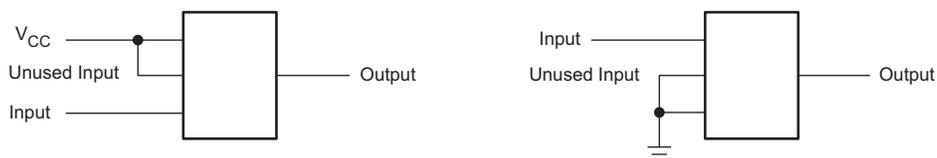
Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply a 0.1-µF capacitor is recommended and if there are multiple  $V_{CC}$  pins then a 0.01-µF or 0.022-µF capacitor is recommended for each power pin. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input terminals should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to Gnd or  $V_{CC}$  whichever make more sense or is more convenient.

### 11.2 Layout Example



**Figure 6. Layout Example Schematic**

## 12 Device and Documentation Support

### 12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.2 Trademarks

E2E is a trademark of Texas Instruments.  
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### 12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUP1T17DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(675 ~ 67F)	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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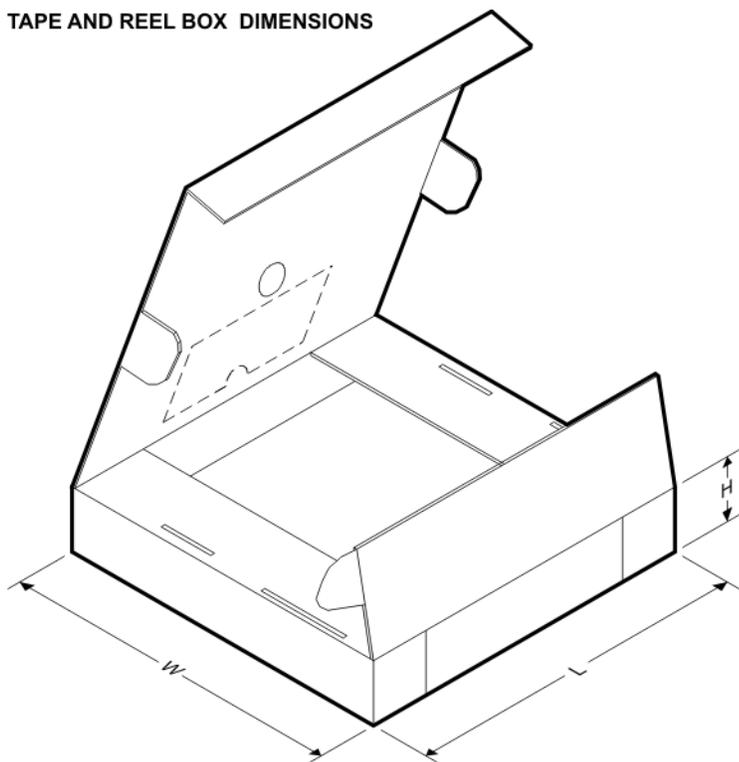


**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1T17DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1T17DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

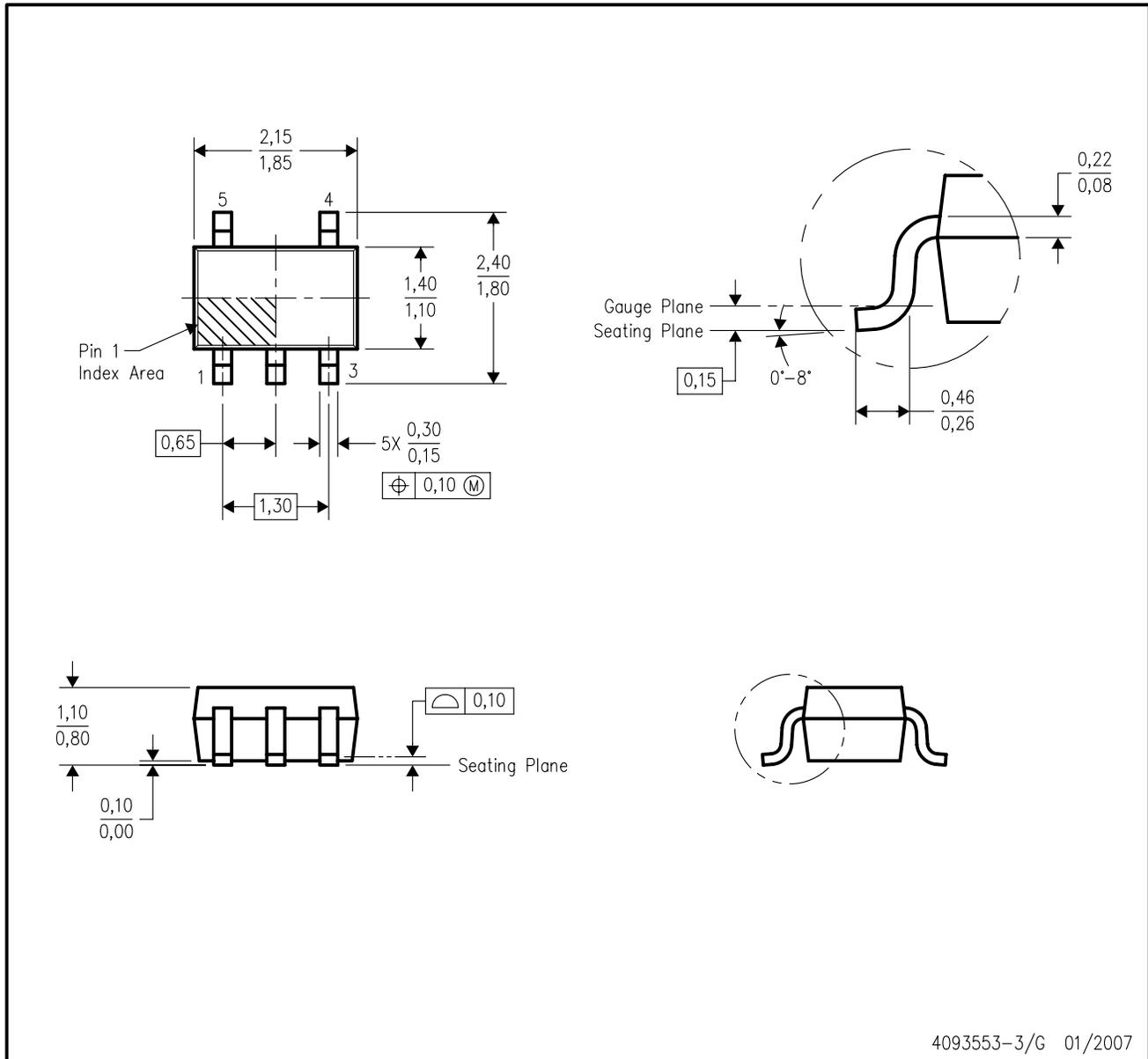
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1T17DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AUP1T17DCKR	SC70	DCK	5	3000	180.0	180.0	18.0

DCK (R-PDSO-G5)

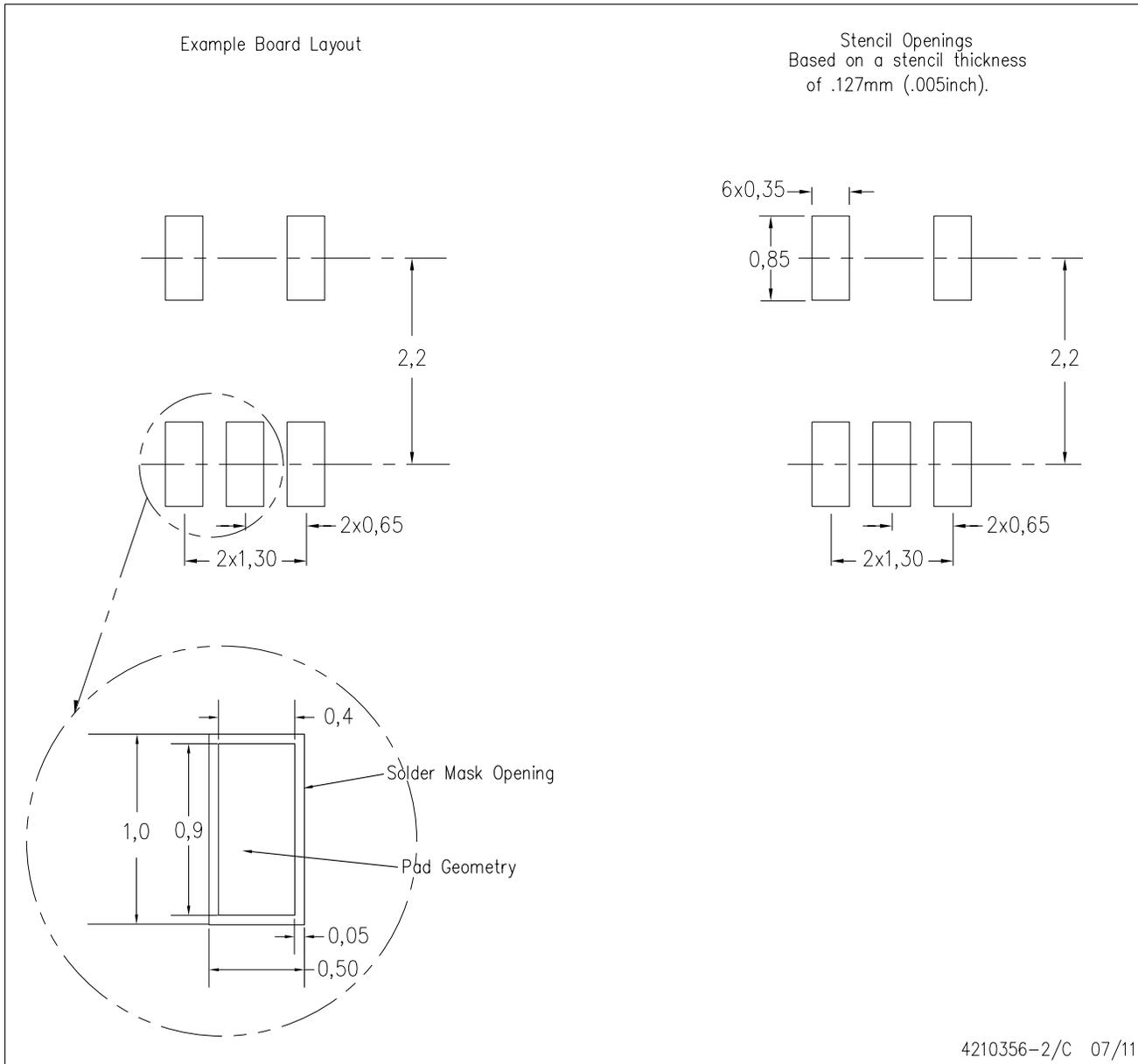
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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