

STRUCTURE Silicon Monolithic Integrated Circuit

NAME OF PRODUCT DC-AC Inverter Control IC

TYPE **BD9240F / BD9240FV**

FUNCTION

- 20V High voltage process
- 2CH control with Push-Pull
- Lamp current and voltage sense feed back control
- Sequencing easily achieved with Soft Start Control
- Short circuit protection with Timer Latch
- Under Voltage Lock Out
- Mode-selectable the operating or stand-by mode by stand-by pin
- Automatic Judge function for External synchronization of lamp oscillation
- BURST mode controlled by PWM and DC input

○ Absolute Maximum Ratings (T<sub>a</sub> = 25°C)

Parameter	Symbol	Limits	Unit
Supply Voltage	VCC	20	V
Operating Temperature Range	Topr	-40~+85	°C
Storage Temperature Range	Tstg	-55~+150	°C
Maximum Junction Temperature	Tjmax	+150	°C
Power Dissipation	Pd	*1 1063 (BD9240FV)	mW
		*2 750 (BD9240F)	

\*1Pd derate at 8.5mW/°C for temperature above Ta = 25°C (When mounted on a PCB 70.0mm×70.0mm×1.6mm)

\*2Pd derate at 6.0mW/°C for temperature above Ta = 25°C (When mounted on a PCB 70.0mm×70.0mm×1.6mm)

○ Operating condition

Parameter	Symbol	Limits	Unit
Supply voltage	VCC	8.0 ~ 19.0	V
oscillation frequency	FOUT	30 ~ 90	kHz
BCT oscillation frequency	FBCT	0.05 ~ 1.00	kHz

○ Electric Characteristics (Ta=25°C, VCC=12V)

Parameter	Symbol	Limits			Unit	Conditions
		MIN.	TYP.	MAX.		
<b>((WHOLE DEVICE))</b>						
Operating current	I <sub>cc1</sub>	—	6.2	12.0	mA	F <sub>OUT</sub> =60kHz, FB=GND
Stand-by current	I <sub>cc2</sub>	—	21	60	uA	
<b>((STAND BY CONTROL))</b>						
Stand-by voltage H 1	V <sub>sth1</sub>	VCC×0.85	—	VCC	V	System ON (DUTY 2ch input mode)
Stand-by voltage H 2	V <sub>sth2</sub>	2	—	VCC×0.5	V	System ON (DUTY 1ch input mode)
Stand-by voltage L	V <sub>stL</sub>	-0.3	—	0.8	V	System OFF
<b>((UVLO BLOCK))</b>						
Operating voltage (VCC)	V <sub>uvlo</sub>	6.65	7.00	7.35	V	
Hysteresis width (VCC)	ΔV <sub>uvlo</sub>	0.37	0.50	0.63	v	
Operating voltage (UVLO)	V <sub>vlo_u</sub>	2.4	2.5	2.6	V	
Hysteresis width (UVLO)	ΔV <sub>vlo_u</sub>	0.075	0.100	0.125	V	
<b>((SOFT START BLOCK))</b>						
Soft start current	I <sub>ss</sub>	1.5	2.0	2.5	uA	
SS_COMP detect voltage	V <sub>ss</sub>	2.3	2.5	2.7	V	
<b>((OSC BLOCK))</b>						
RT Output Voltage	V <sub>RT</sub>	1.05	1.50	1.95	V	
STR ON Resistor value	R <sub>SRT</sub>	—	100	200	Ω	
<b>((BOSC BLOCK))</b>						
BOSC Max voltage	V <sub>BCTH</sub>	1.94	2.00	2.06	V	f <sub>BCT</sub> =0.3kHz
BOSC Min voltage	V <sub>BCTL</sub>	0.40	0.50	0.60	V	f <sub>BCT</sub> =0.3kHz
BOSC constant current	I <sub>BCT</sub>	1.35/BRT	1.50/BRT	1.65/BRT	A	
BOSC frequency	f <sub>BCT</sub>	291	300	309	Hz	(BRT=36.2kΩ, BCT=0.047uF)
<b>((FEED BACK BLOCK))</b>						
IS threshold voltage 1	V <sub>is1</sub>	1.225	1.250	1.275	V	
IS threshold voltage 2	V <sub>is2</sub>	—	V <sub>REF IN</sub>	V <sub>IS1</sub>	V	V <sub>REF</sub> applying voltage
VS threshold voltage	V <sub>vs</sub>	1.220	1.250	1.280	V	
IS source current 1	I <sub>is1</sub>	—	—	0.9	uA	DUTY=2.0V
IS source current 2	I <sub>is2</sub>	40	50	60	uA	DUTY=0V, IS=1.0V
VS source current	I <sub>vs</sub>	—	—	0.9	uA	
IS COMP detect voltage 1	V <sub>ISCOMP1</sub>	0.64	0.66	0.68	V	V <sub>REF IN</sub> ≥1.25V
IS COMP detect voltage 2	V <sub>ISCOMP2</sub>	—	0.5	—	V	V <sub>REF IN</sub> =1V
V <sub>REF</sub> input voltage range	V <sub>REF IN</sub>	0.6	—	1.6	V	No effect at V <sub>REF</sub> >1.25V
<b>((OUTPUT BLOCK))</b>						
NA output voltage H	V <sub>outAH</sub>	VCC-0.3	VCC-0.1	—	V	
NB output voltage H	V <sub>outBH</sub>	VCC-0.3	VCC-0.1	—	V	
NA output voltage L	V <sub>outAL</sub>	—	0.1	0.3	V	
NB output voltage L	V <sub>outBL</sub>	—	0.1	0.3	V	
NA output sink resistance	R <sub>sink_NA</sub>	1.3	2.5	5.0	Ω	
NA output source resistance	R <sub>source_NA</sub>	4.0	8.0	16.0	Ω	
NB output sink resistance	R <sub>sink_NB</sub>	1.3	2.5	5.0	Ω	
NB output source resistance	R <sub>source_NB</sub>	4.0	8.0	16.0	Ω	
Drive output frequency	f <sub>out</sub>	57.9	60.0	62.1	kHz	RT=21kΩ
<b>((GT SYNCHRONOUS BLOCK : CLKIN pin))</b>						
Input High voltage range	V <sub>CT_CLKIN_H</sub>	2.5	—	5.0	V	
Input Low voltage range	V <sub>CT_CLKIN_L</sub>	-0.3	—	0.5	V	



**ONOTE FOR USE**

1. This product is produced with strict quality control, but might be destroyed if used beyond its absolute maximum ratings. Once IC is destroyed, failure mode will be difficult to determine, like short mode or open mode. Therefore, physical protection countermeasure, like fuse is recommended in case operating conditions go beyond the expected absolute maximum ratings.
2. The circuit functionality is guaranteed within of ambient temperature operation range as long as it is within recommended operating range. The standard electrical characteristic values cannot be guaranteed at other voltages in the operating ranges, however the variation will be small.
3. Mounting failures, such as misdirection or miscounts, may harm the device.
4. A strong electromagnetic field may cause the IC to malfunction.
5. The GND pin should be the location within  $\pm 0.3V$  compared with the PGND pin.
6. BD9240F/FV incorporate a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation of the thermal shutdown circuit is assumed.
7. Absolute maximum ratings are those values that, if exceeded, may cause the life of a device to become significantly shortened. Moreover, the exact failure mode caused by short or open is not defined. Physical countermeasures, such as a fuse, need to be considered when using a device beyond its maximum ratings.
8. About the external FET, the parasitic Capacitor may cause the gate voltage to change, when the drain voltage is switching. Make sure to leave adequate margin for this IC variation.
9. Under operating CP charge (under error mode) analog dimming and burst dimming are not operate.
10. By STB and PH voltage, BD9240F/FV are changed to 3 states. Therefore, do not input STB and PH pin voltage between one state and the other state (0.8~2.0V,  $VCC \times 0.5 \sim VCC \times 0.85$  V)
11. By the DUTY1 pin for setting of Burst dimming Mode, When Burst dimming by DC signal do not input DUTY1 voltage between one state and the other state (0.485~0.515V, 1.985~2.015V)  
When Burst dimming by PWM signal, set ON time and OFF time of the input PWM pulse signal to more than 30us (Dimming of 0% and Dimming of 100% are no problem)
12. The pin connected a connector need to connect to the resistor for electrical surge destruction.
13. This IC is a monolithic IC which (as shown is Fig.1)has P<sup>+</sup> substrate and between the various pins. A P-N junction is formed from this P layer of each pin. For example, the relation between each potential is as follows.  
○(When GND > PinB and GND > PinA, the P-N junction operates as a parasitic diode.)  
○(When PinB > GND > PinA, the P-N junction operates as a parasitic transistor.)  
Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits as well as operation faults and physical damage. Accordingly you must not use methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin.

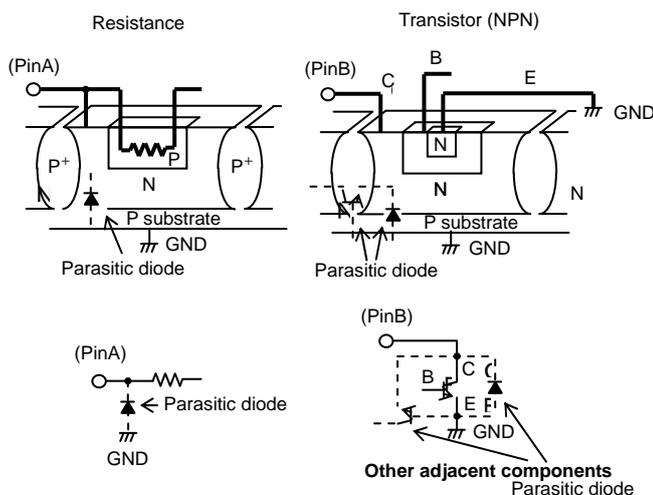


Fig.1 Simplified structure of a Bipolar IC

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