



FAN7382

Half-Bridge Gate Driver

Features

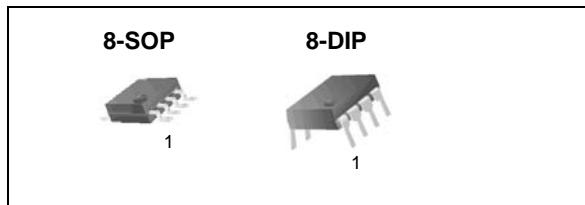
- Floating Channels Designed for Bootstrap Operation to +600V
- Typically 350mA/650mA Sourcing/Sinking Current Driving Capability for Both Channels
- Common-Mode dv/dt Noise Canceling Circuit
- Extended Allowable Negative VS Swing to -9V for Signal Propagation @ VCC=VBS=15V
- VCC & VBS Supply Range from 10V to 20V
- UVLO Functions for Both Channels
- TTL Compatible Input Logic Threshold Levels
- Matched Propagation Delay Below 50nsec
- Output In-phase with Input

Applications

- PDP Scan Driver
- Fluorescent Lamp Ballast
- SMPS
- Motor Driver

Description

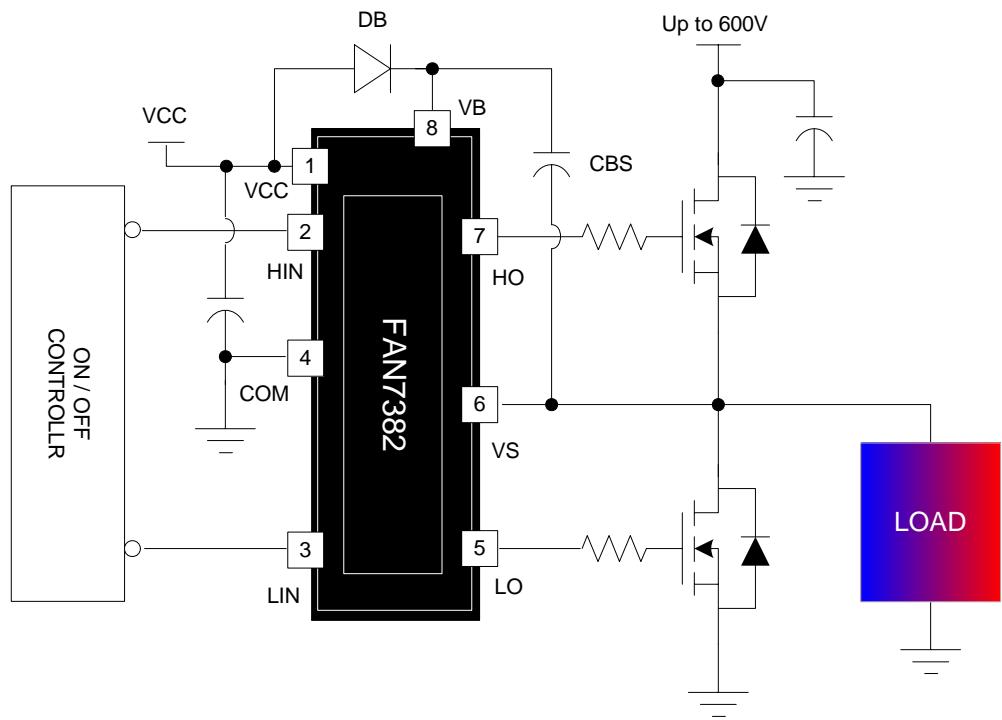
The FAN7382, a monolithic half-bridge gate driver IC, can drive MOSFETs and IGBTs that operate up to +600V. Fairchild's high-voltage process and common-mode noise canceling technique provides stable operation of the high-side driver under high dv/dt noise circumstances. An advanced level shift circuit allows high-side gate driver operation up to $V_S=-9.8$ V(typ.) for $VBS=15$ V. The input logic level is compatible with standard TTL-series logic gates. UVLO circuits for both channels prevent malfunction when VCC and VBS are lower than the specified threshold voltage. Output drivers typically source/sink 350mA/650mA, respectively, which is suitable for fluorescent lamp ballasts, PDP scan drivers, motor controls, etc.



Ordering Information

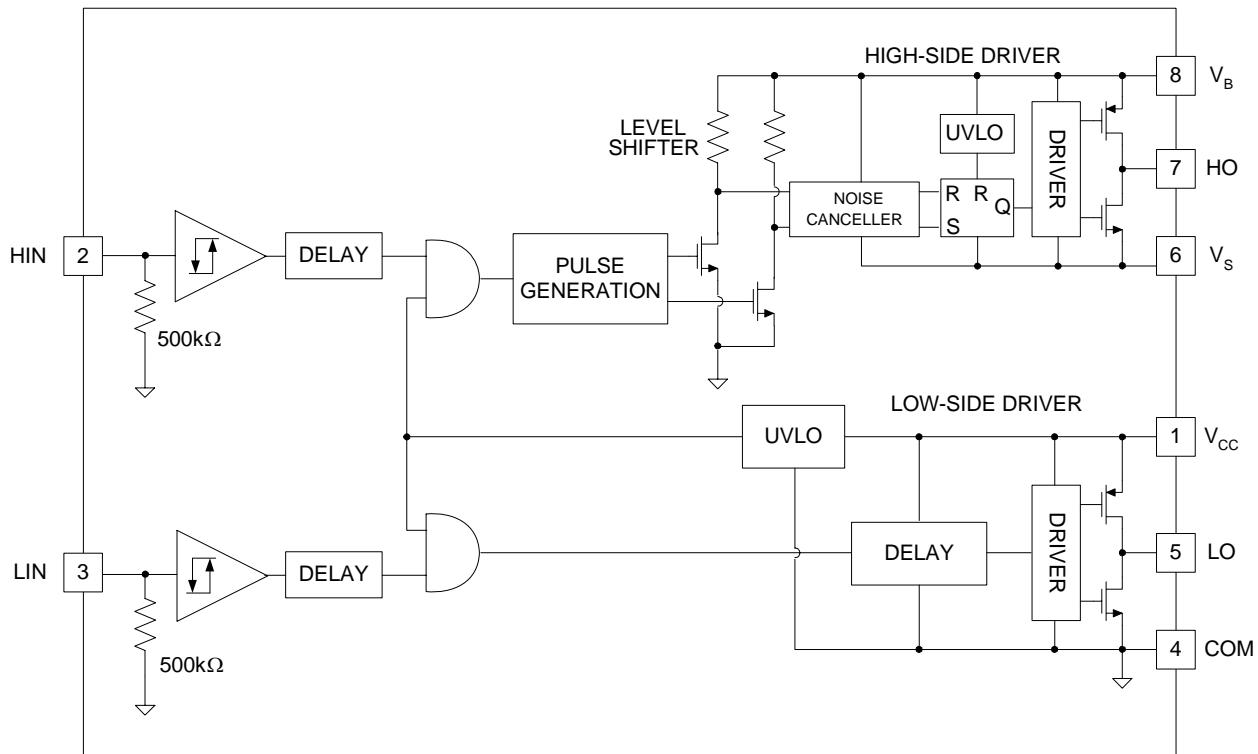
Part Number	Package	Pb-Free	Operating Temperature Range	Packing Method
FAN7382N	8-DIP	Yes	-40°C ~ 125°C	TUBE
FAN7382M	8-SOP	Yes		TUBE
FAN7382MX		Yes		TAPE & REEL

Typical Application Circuit



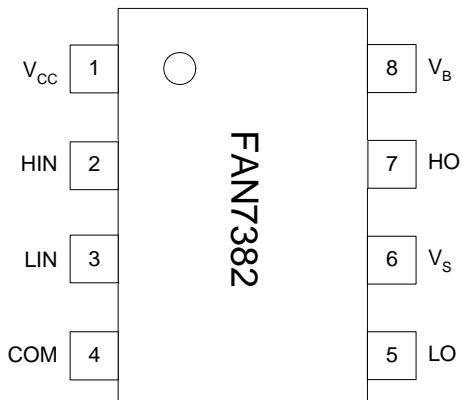
FAN7382 Rev.03

Internal Block Diagram



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Pin Assignments



FAN7382 Rev.03

Pin Definitions

Pin	Name	Function/ Description
1	VCC	Low-Side Supply Voltage
2	HIN	Logic Input for High-Side Gate Driver Output
3	LIN	Logic Input for Low-Side Gate Driver Output
4	COM	Logic Ground and Low-Side Driver Return
5	LO	Low-Side Driver Output
6	VS	High-Voltage Floating Supply Return
7	HO	High-Side Driver Output
8	VB	High-Side Floating Supply

Absolute Maximum Ratings

The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings.

Symbol	Characteristics	Min.	Max.	Unit
V_S	High-side offset voltage	V_B-25	$V_B+0.3$	V
V_B	High-side floating supply voltage	-0.3	625	
V_{HO}	High-side floating output voltage HO	$V_S-0.3$	$V_B+0.3$	
V_{CC}	Low-side and logic fixed supply voltage	-0.3	25	
V_{LO}	Low-side output voltage LO	-0.3	$V_{CC}+0.3$	
V_{IN}	Logic input voltage(HIN, LIN)	-0.3	$V_{CC}+0.3$	
COM	Logic ground	$V_{CC}-25$	$V_{CC}+0.3$	
dVs/dt	Allowable offset voltage SLEW RATE	-	50	V/ns
P_D	Power dissipation	SOP	0.625	W
		DIP	1.2	
R_{thja}	Thermal resistance, junction-to-ambient	SOP	200	°C/W
		DIP	100	
T_J	Junction temperature	-	150	°C
T_S	Storage temperature	-	150	°C

Electrical Characteristics

($V_{BIAS}(V_{CC}, V_{BS})=15.0V$, $T_A = 25^\circ C$, unless otherwise specified. The V_{IN} , V_{TH} , and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and V_S is applicable to HO and LO.)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
VCCUV+	VCC and VBS supply under-voltage positive going threshold		8.2	9.2	10.0	V
VCCUV-	VCC and VBS supply under-voltage negative going threshold		7.6	8.7	9.6	
VCCUVH VBSUVH	VCC supply under-voltage lockout hysteresis		-	0.6	-	
I_{LK}	Offset supply leakage current	$V_B=V_S=600V$	-	-	50	μA
I_{QBS}	Quiescent VBS supply current	$V_{IN}=0V$ or $5V$	-	45	120	
I_{QCC}	Quiescent VCC supply current	$V_{IN}=0V$ or $5V$	-	70	180	
I_{PBS}	Operating VBS supply current	$f_{in}=20kHz$, rms value	-	-	600	μA
I_{PCC}	Operating VCC supply current	$f_{in}=20kHz$, rms value	-	-	600	
V_{IH}	Logic "1" input voltage		2.9	-	-	V
V_{IL}	Logic "0" input voltage		-	-	0.8	
V_{OH}	High level output voltage, $V_{BIAS}-VO$		-	-	1.0	
V_{OL}	Low level output voltage, VO	$I_O=20mA$	-	-	0.6	
I_{IN+}	Logic "1" input bias current		-	10	20	
I_{IN-}	Logic "0" input bias current	$V_{IN}=0V$	-	1.0	2.0	μA
I_{O+}	Output high short circuit pulse current	$V_O=0V, VIN=5V$ with $PW<10\mu s$	250	350	-	mA
I_{O-}	Output low short circuit pulsed current	$V_O=15V=VB, VIN=0V$ with $PW<10\mu s$	500	650	-	
V_S	Allowable negative VS pin voltage for HIN signal propagation to HO		-	-9.8	-7	V

Dynamic Electrical Characteristics

($V_{BIAS}(V_{CC}, V_{BS})=15.0V$, $V_S=COM$, $C_L=1000pF$ and $T_A = 25^\circ C$, unless otherwise specified.)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
t_{on}	Turn-on propagation delay	$V_S=0V$	100	170	300	ns
t_{off}	Turn-off propagation delay	$V_S=0V$ or $600V$	100	200	300	
t_r	Turn-on rise time		20	60	140	
t_f	Turn-off fall time		-	30	80	
MT	Delay matching, HS & LS turn-on/off		-	-	50	

Typical Characteristics

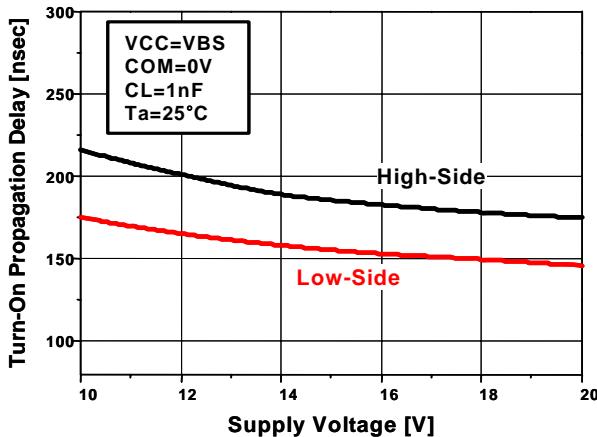


Figure 1. Turn-On Propagation Delay vs. Supply Voltage

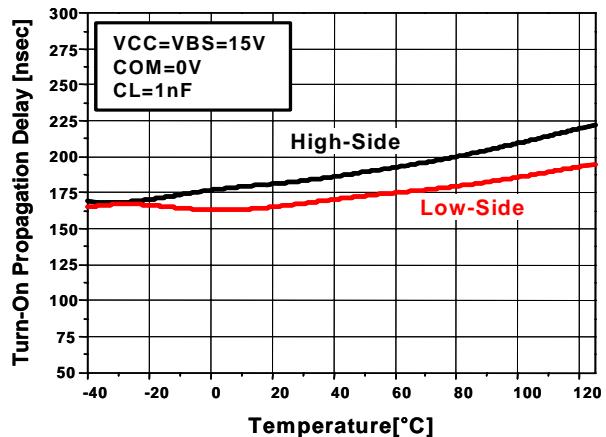


Figure 2. Turn-On Propagation Delay vs. Temp.

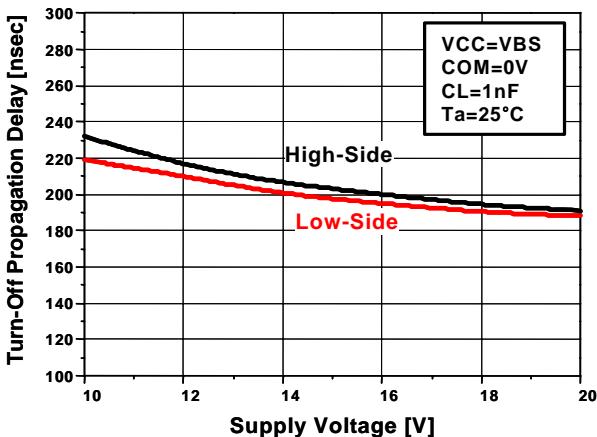


Figure 3. Turn-Off Propagation Delay vs. Supply Voltage

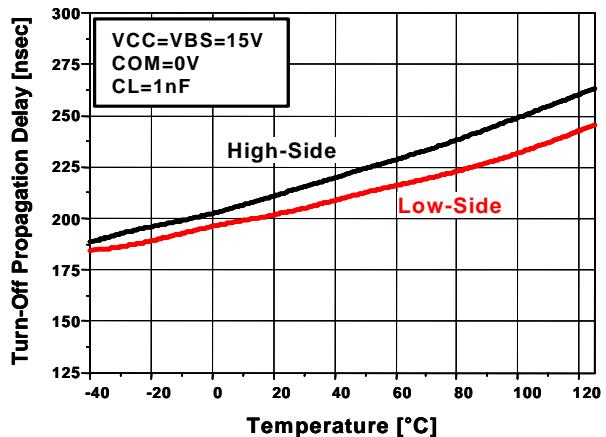


Figure 4. Turn-Off Propagation Delay vs. Temp.

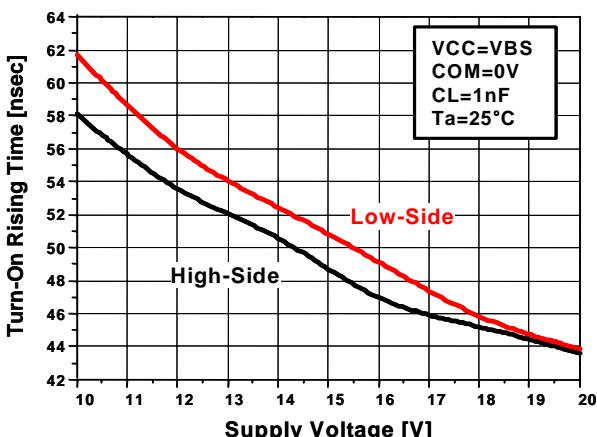


Figure 5. Turn-On Rising Time vs. Supply Voltage

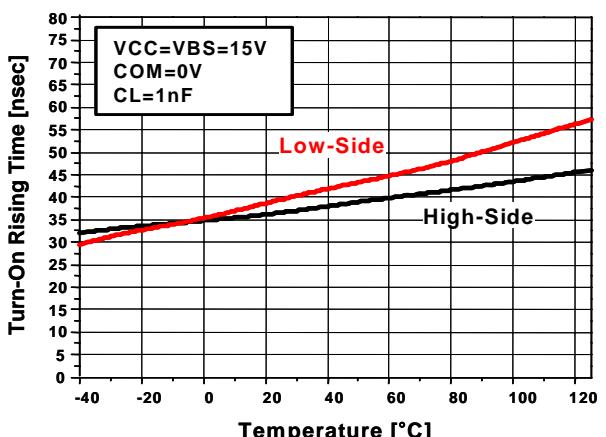


Figure 6. Turn-On Rising Time vs. Temp.

Typical Characteristics (Continued)

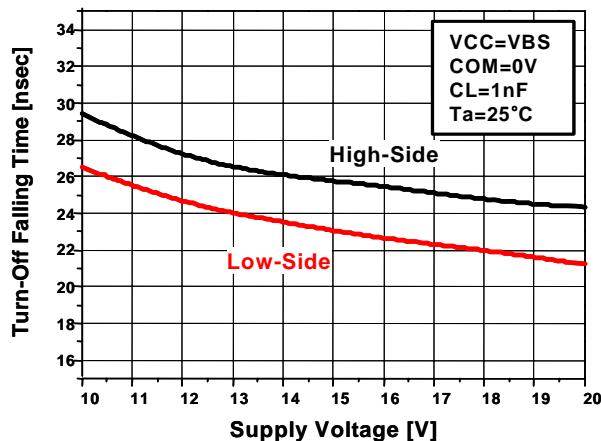


Figure 7. Turn-Off Falling Time vs. Supply Voltage

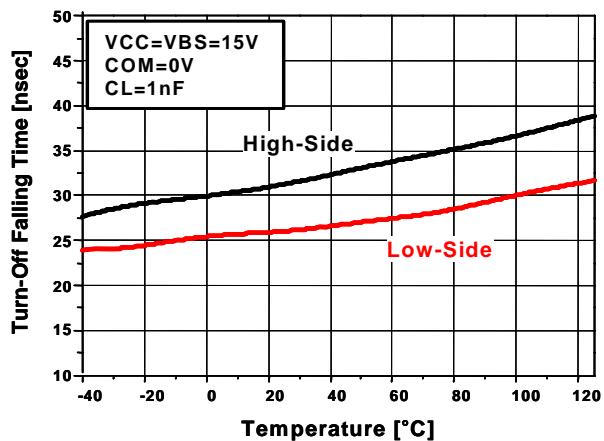


Figure 8. Turn-Off Falling Time vs. Temp.

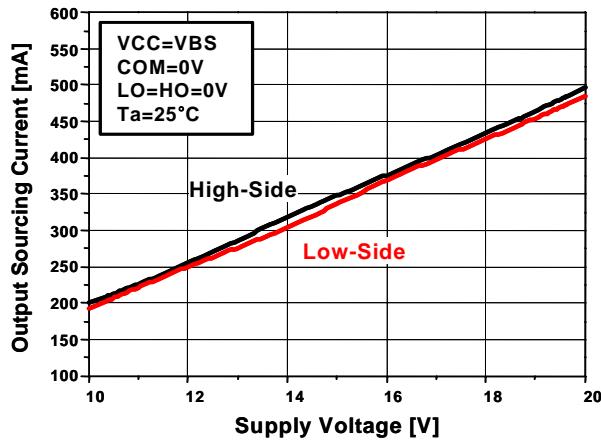


Figure 9. Output Sourcing Current vs. Supply Voltage

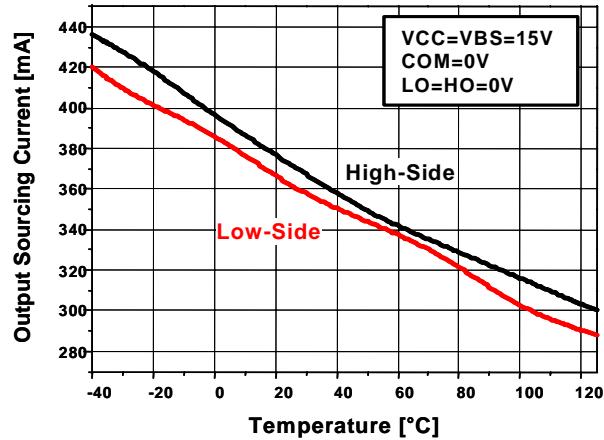


Figure 10. Output Sourcing Current vs. Temp.

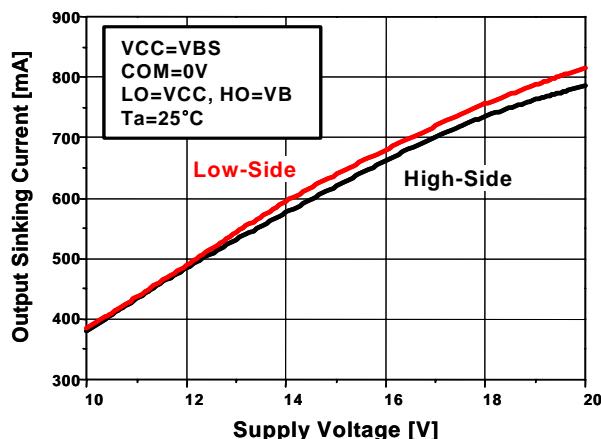


Figure 11. Output Sinking Current vs. Supply Voltage

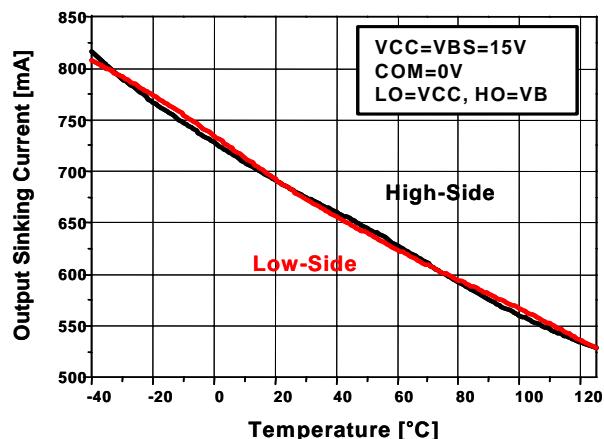


Figure 12. Output Sinking Current vs. Temp.

Typical Characteristics (Continued)

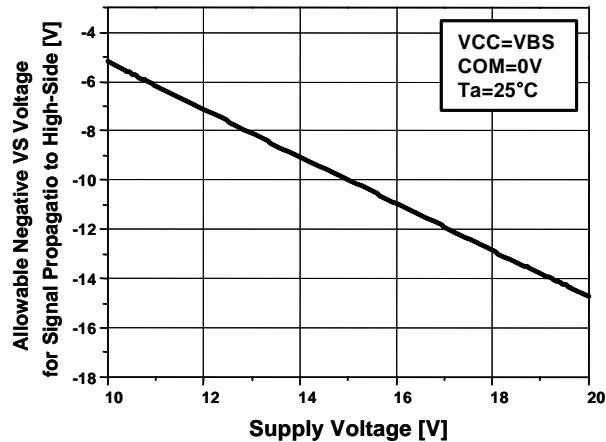


Figure 13. Allowable Negative VS Voltage for Signal Propagation to High Side vs. Supply Voltage

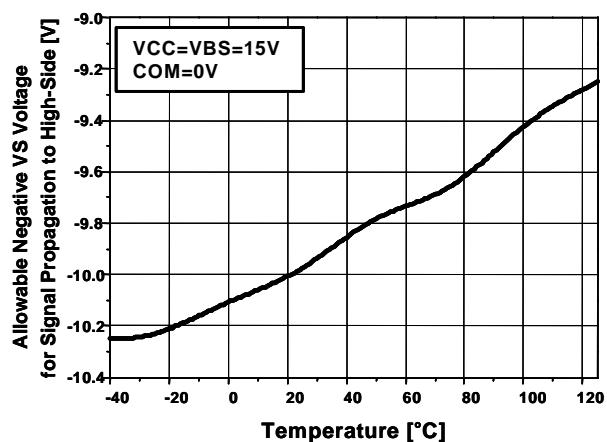


Figure 14. Allowable Negative VS Voltage for Signal Propagation to High Side vs. Temp.

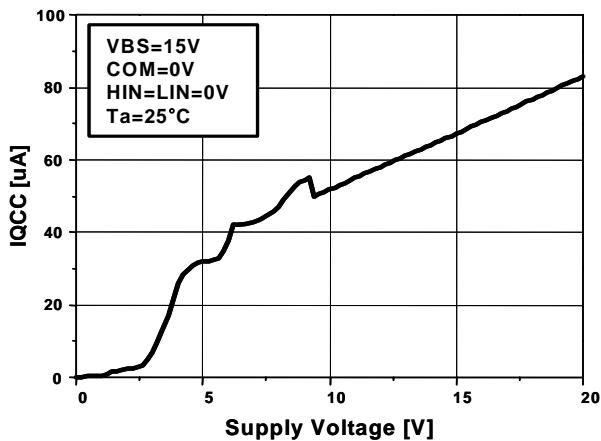


Figure 15. I_{QCC} vs. Supply Voltage

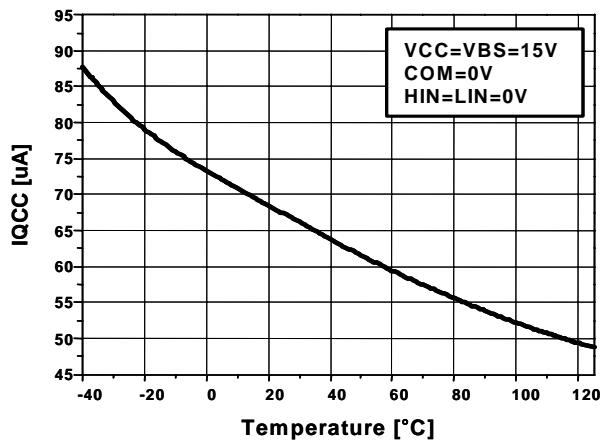


Figure 16. I_{QCC} vs. Temp.

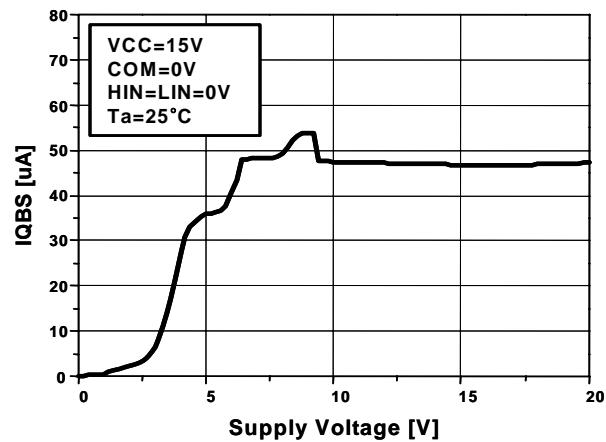


Figure 17. I_{QBS} vs. Supply Voltage

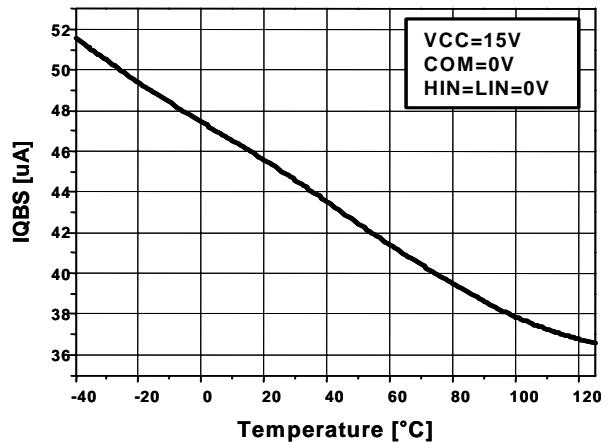
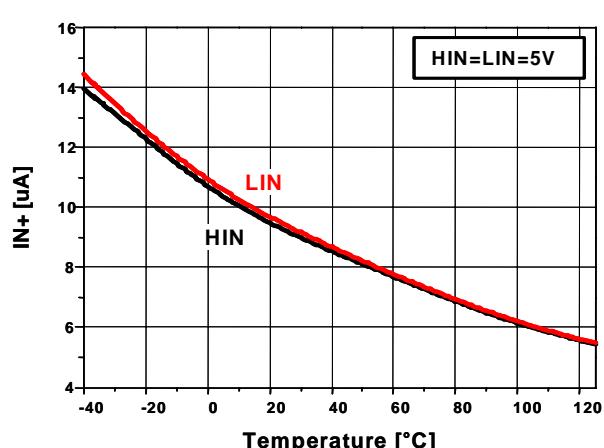
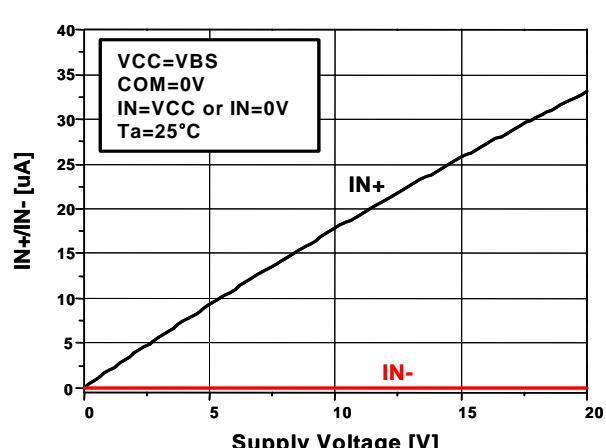
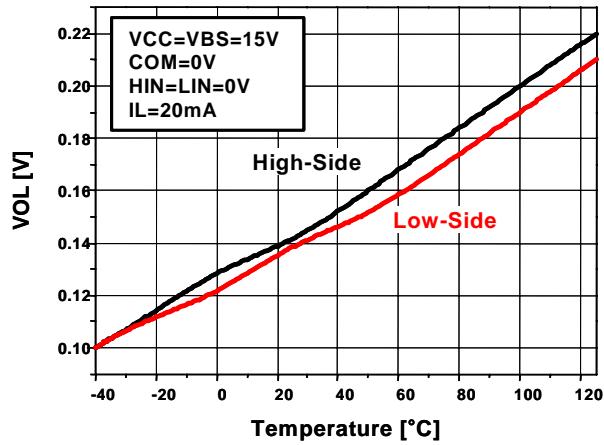
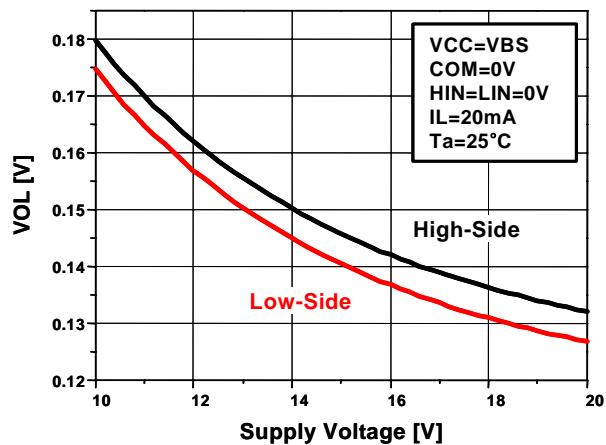
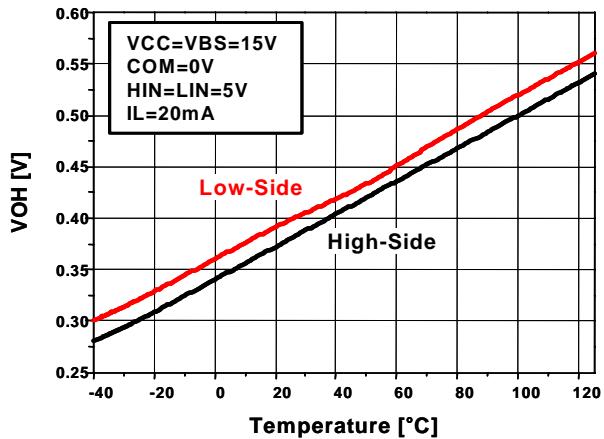
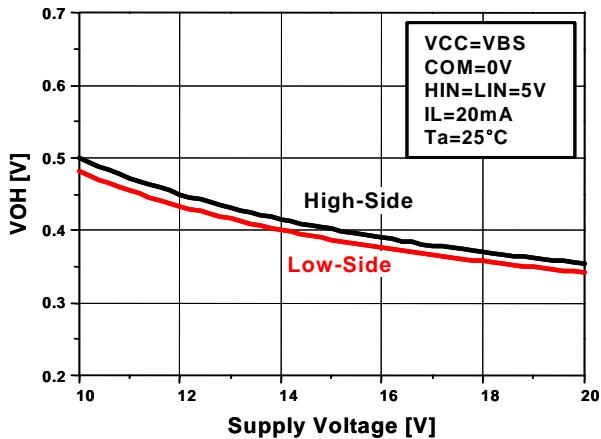


Figure 18. I_{QBS} vs. Temp.

Typical Characteristics (Continued)



Typical Characteristics (Continued)

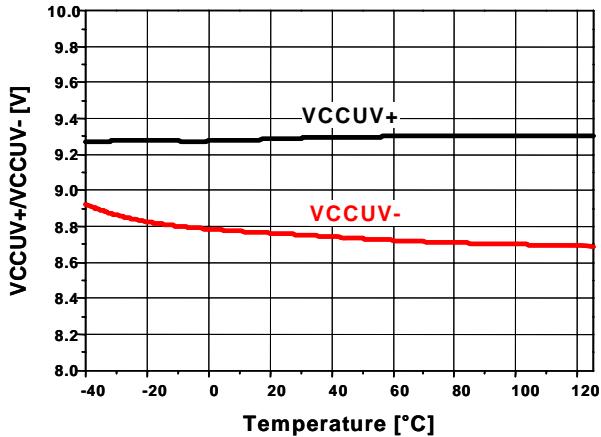


Figure 25. VCC UVLO Threshold Voltage vs. Temp.

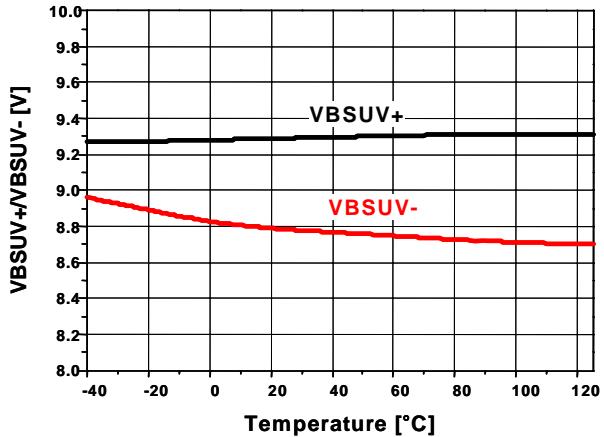


Figure 26. VBS UVLO Threshold Voltage vs. Temp.

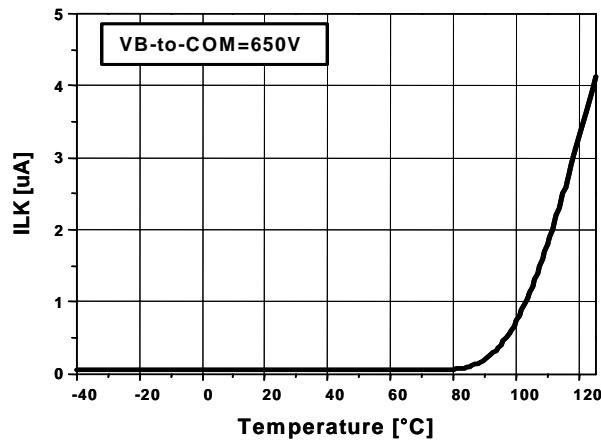


Figure 27. VB to COM Leakage Current vs. Temp.

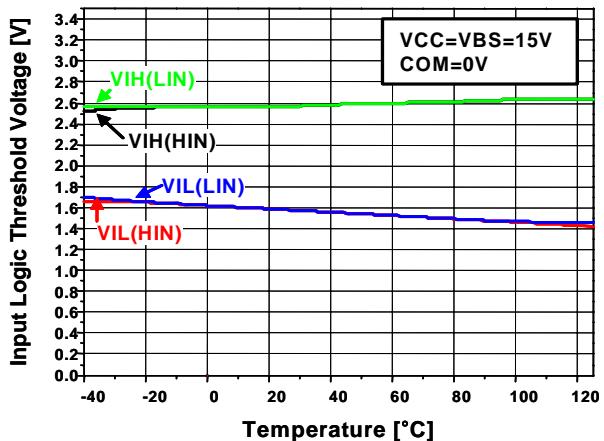


Figure 28. Input Logic Threshold Voltage vs. Temp.

Typical Characteristics (Continued)

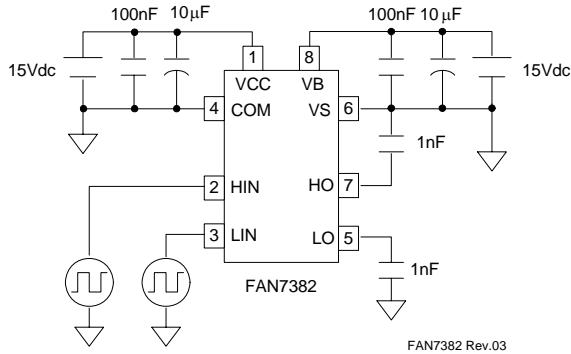


Figure 29. Switching Time Test Circuit

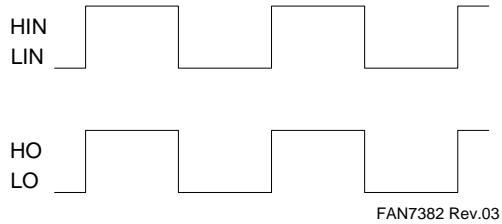


Figure 30. Input / Output Timing Diagram

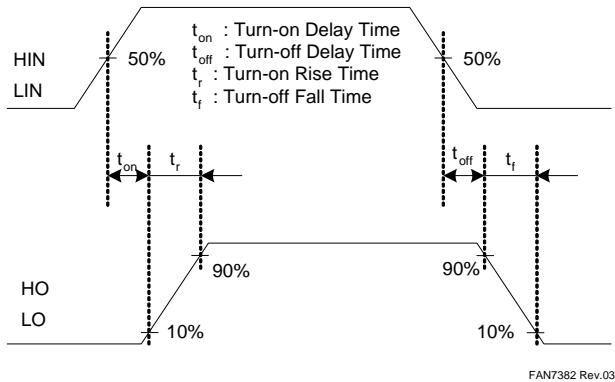


Figure 31. Switching Time Waveform Definitions

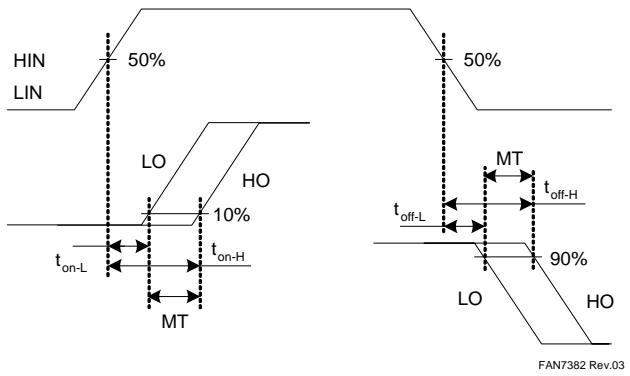
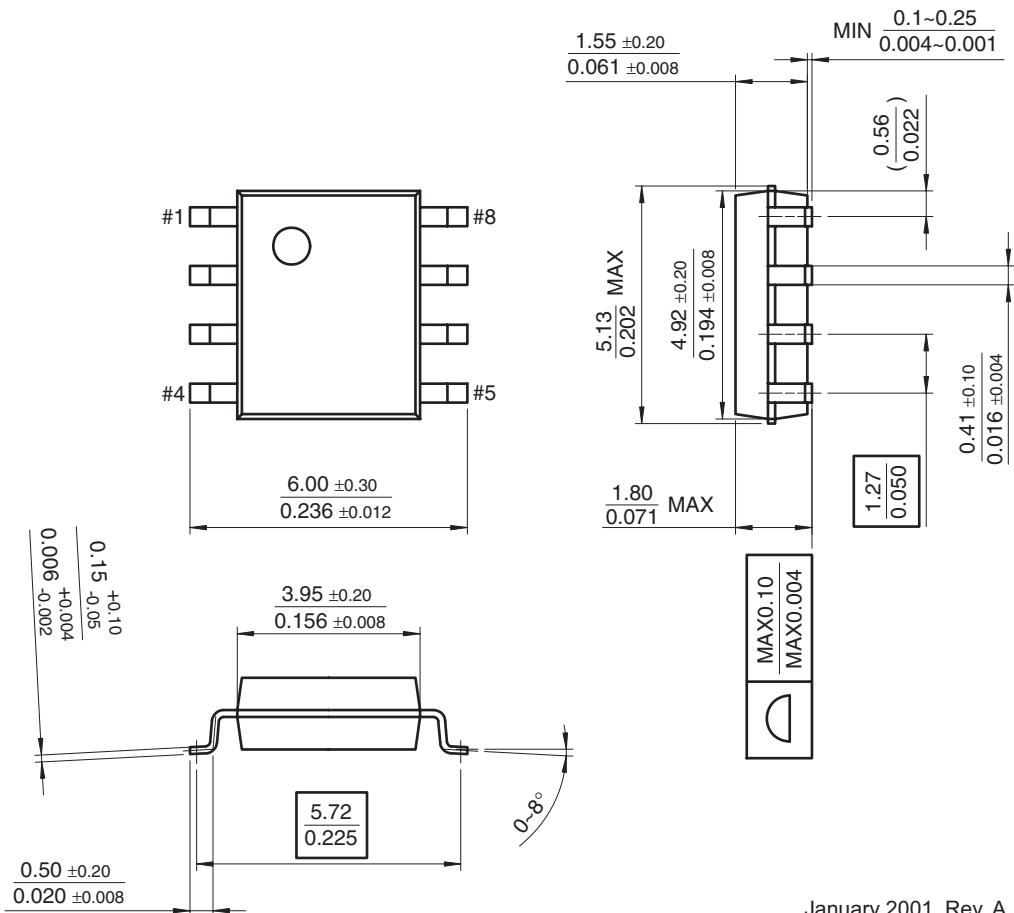


Figure 32. Delay Matching Waveform Definition

Mechanical Dimensions

8-SOP

Dimensions are in millimeters (inches) unless otherwise noted.

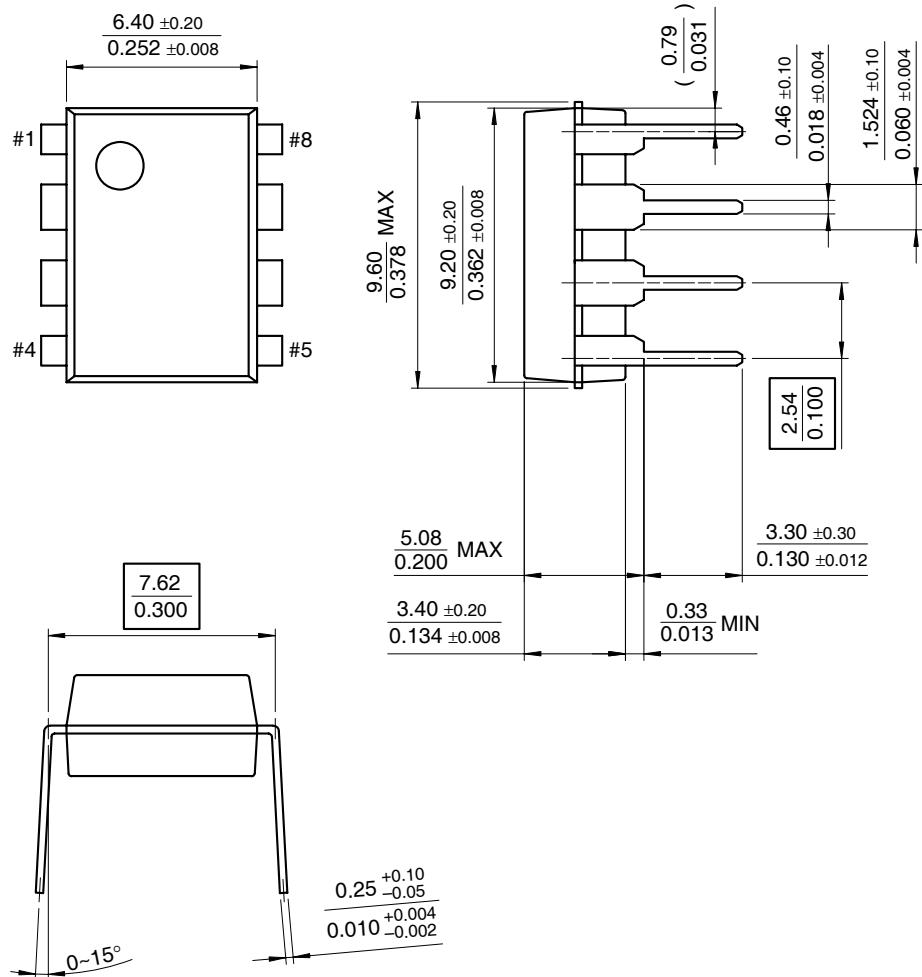


January 2001, Rev. A

Mechanical Dimensions (Continued)

8-DIP

Dimensions are in millimeters (inches) unless otherwise noted.



September 1999, Rev B

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EnSigna™	MICROCOUPLER™	QFET®	SyncFET™	VCX™
FACT™	MicroFET™	QS™	TCM™	Wire™
FACT Quiet Series™	MicroPak™	QT Optoelectronics™	TinyBoost™	
FAST®	MICROWIRE™	Quiet Series™		Across the board. Around the world.™
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Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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Rev. I20