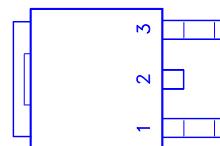
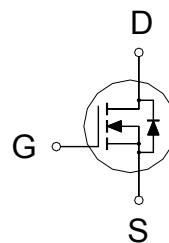


NIKO-SEM
**N-Channel Logic Level Enhancement
Mode Field Effect Transistor**
P2503BDG
TO-252
Halogen-Free & Lead-Free
PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
30	25mΩ	12A


1.GATE
2.DRAIN
3.SOURCE
ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25^\circ\text{C}$	I_D	12	A
	$T_C = 70^\circ\text{C}$		10	
Pulsed Drain Current ¹		I_{DM}	30	A
Avalanche Current		I_{AR}	10	
Avalanche Energy	$L = 0.1\text{mH}$	E_{AS}	5	mJ
Repetitive Avalanche Energy ²	$L = 0.05\text{mH}$	E_{AR}	0.625	
Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	32	W
	$T_C = 70^\circ\text{C}$		22	
Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$		3.9	°C / W
Junction-to-Ambient	$R_{\theta JA}$		75	°C / W

¹Pulse width limited by maximum junction temperature.²Duty cycle ≤ 1%**ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$, Unless Otherwise Noted)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	30			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1	1.5	2.5	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$			± 250	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24\text{V}, V_{GS} = 0\text{V}$			1	μA
		$V_{DS} = 20\text{V}, V_{GS} = 0\text{V}, T_J = 55^\circ\text{C}$			10	

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On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 5V, V _{GS} = 10V	30			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = 4.5V, I _D = 6A		25	37	mΩ
		V _{GS} = 10V, I _D = 12A		18	25	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 12A		19		S

DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 10V, f = 1MHz		790		pF
Output Capacitance	C _{oss}			175		
Reverse Transfer Capacitance	C _{rss}			65		
Total Gate Charge ²	Q _g	V _{DS} = 0.5V _{(BR)DSS} , V _{GS} = 10V, I _D = 12A		16		nC
Gate-Source Charge ²	Q _{gs}			2.5		
Gate-Drain Charge ²	Q _{gd}			2.1		
Turn-On Delay Time ²	t _{d(on)}	V _{DD} = 10V I _D ≈ 1A, V _{GS} = 10V, R _{GEN} = 6Ω		2.2	4.4	nS
Rise Time ²	t _r			7.5	15	
Turn-Off Delay Time ²	t _{d(off)}			11.8	21.3	
Fall Time ²	t _f			3.7	7.4	

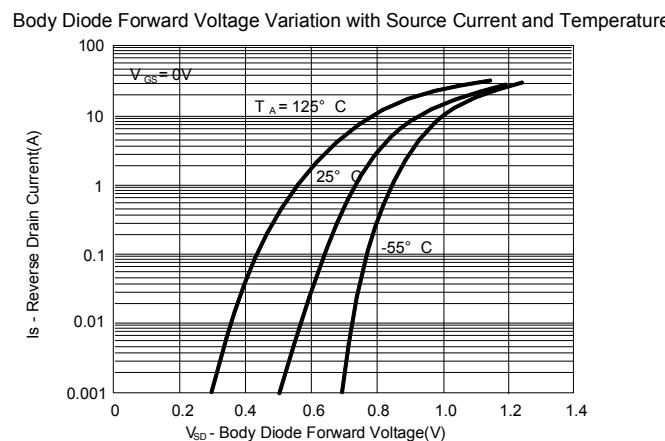
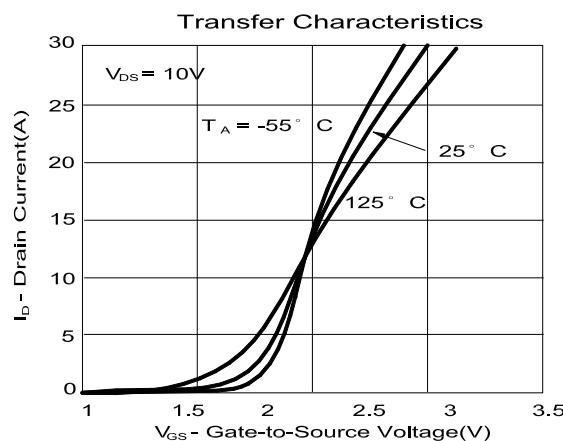
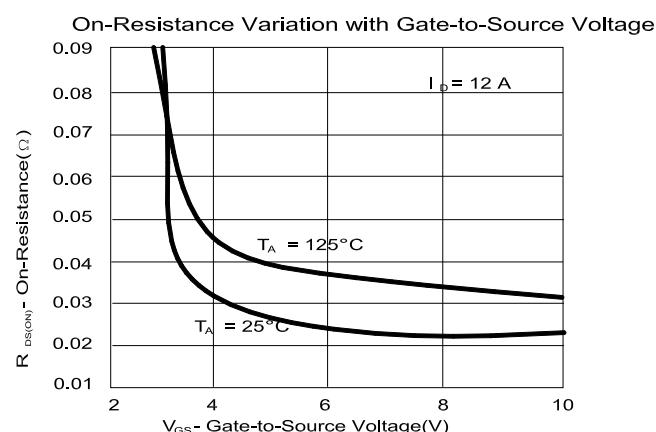
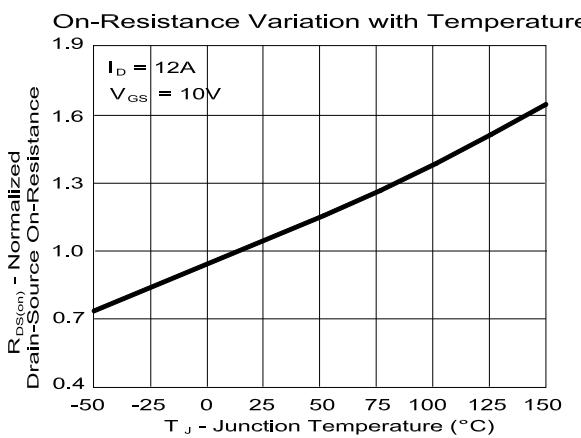
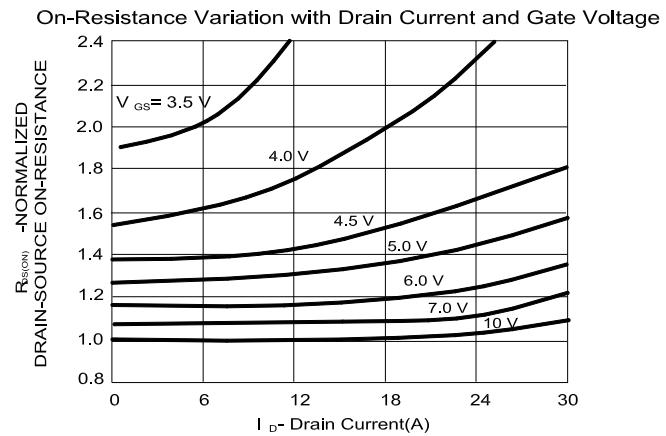
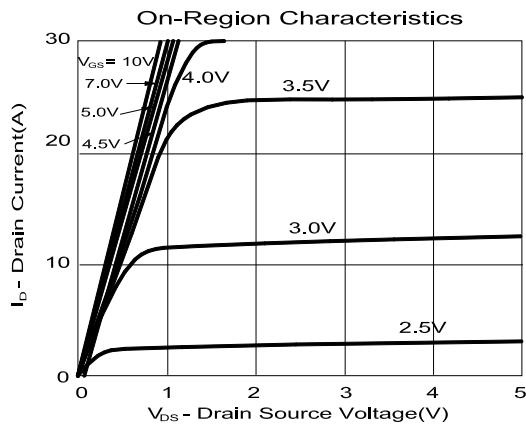
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_c = 25 °C)

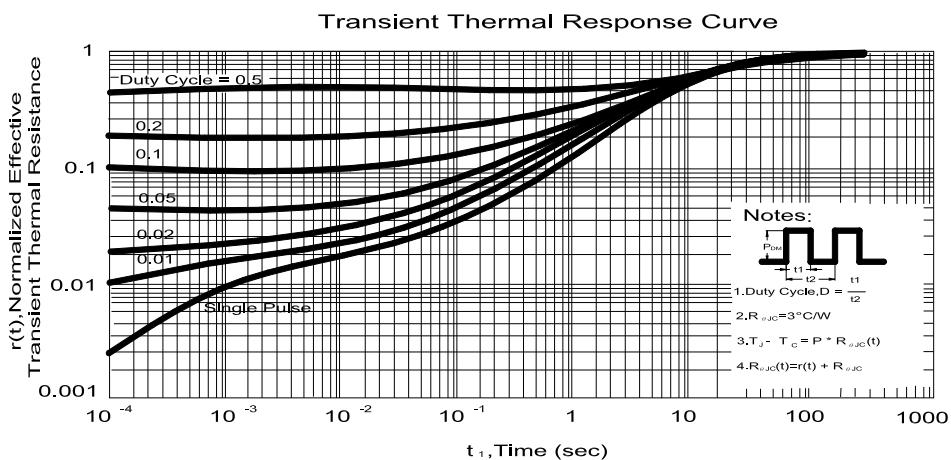
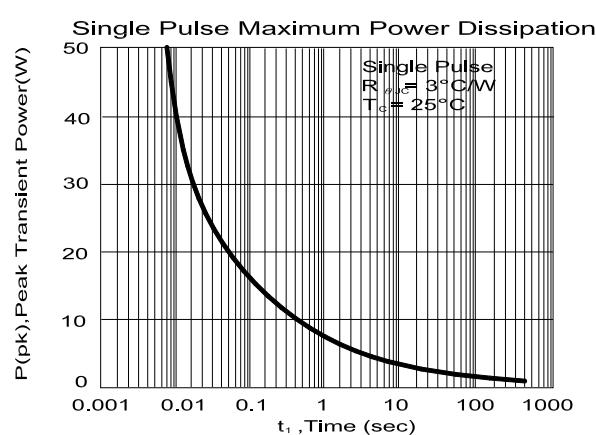
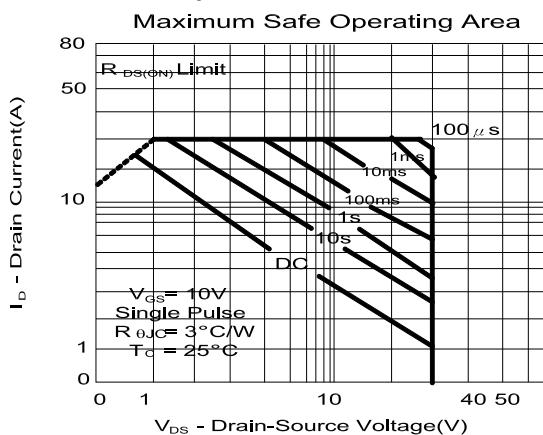
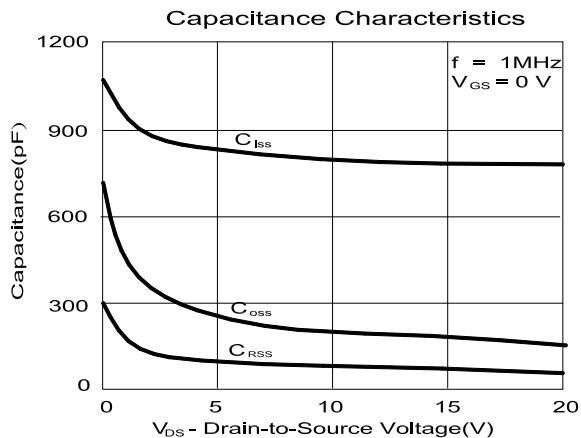
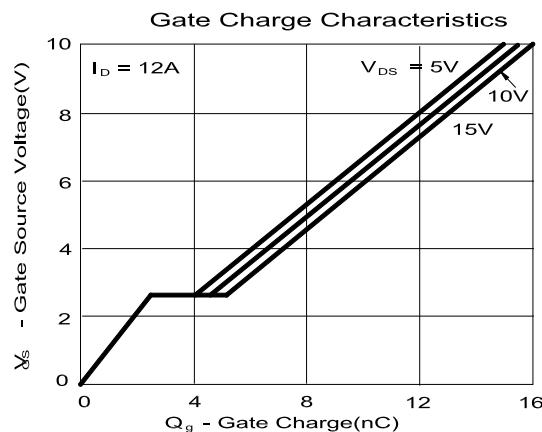
Continuous Current	I _S	I _F = 1A, V _{GS} = 0V I _F = 5 A, dI _F /dt = 100A / μS			1.3	A
Pulsed Current ³	I _{SM}				2.6	
Forward Voltage ¹	V _{SD}				1	V
Reverse Recovery Time	t _{rr}			18.8		ns
Reverse Recovery Charge	Q _{rr}			17.6		nC

¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.²Independent of operating temperature.³Pulse width limited by maximum junction temperature.

REMARK: THE PRODUCT MARKED WITH "P2503BDG", DATE CODE or LOT #

TYPICAL PERFORMANCE CHARACTERISTICS



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NIKO-SEM**N-Channel Logic Level Enhancement
Mode Field Effect Transistor****P2503BDG
TO-252
Halogen-Free & Lead-Free****TO-252 (DPAK) MECHANICAL DATA**

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	8.9	9.5	10.4	H	0.8	1.27	2.03
B	2.19	2.3	2.435	I	6.35	6.6	6.8
C	0.35	0.5	0.65	J	4.8	5.34	5.5
D	0.89		1.5	K	0.5		1.5
E	0.35		0.65	L	0.4	0.76	0.89
F	0.0		0.23	M	3.96		5.18
G	5.4		6.2	W	3.38	3.58	3.78

