DS90C387A,DS90CF388A

DS90C387A/DS90CF388A Dual Pixel LVDS Display Interface / FPD-Link

Literature Number: SNLS065D

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DS90C387A/DS90CF388A
Dual Pixel LVDS Display Interface / FPD-Link

General Description

The DS90C387A/DS90CF388A transmitter/receiver pair is designed to support dual pixel data transmission between Host and Flat Panel Display up to QXGA resolutions. The transmitter converts 48 bits (Dual Pixel 24-bit color) of CMOS/TTL data and 3 control bits into 8 LVDS (Low Voltage Differential Signalling) data streams. At a maximum dual pixel rate of 112MHz, LVDS data line speed is 784Mbps, providing a total throughput of 5.7Gbps (714 Megabytes per second).

The LDI chipset is improved over prior generations of FPD-Link devices and offers higher bandwidth support and longer cable drive. To increase bandwidth, the maximum pixel clock rate is increased to 112 MHz and 8 serialized LVDS outputs are provided. Cable drive is enhanced with a user selectable pre-emphasis feature that provides additional output current during transitions to counteract cable loading effects.

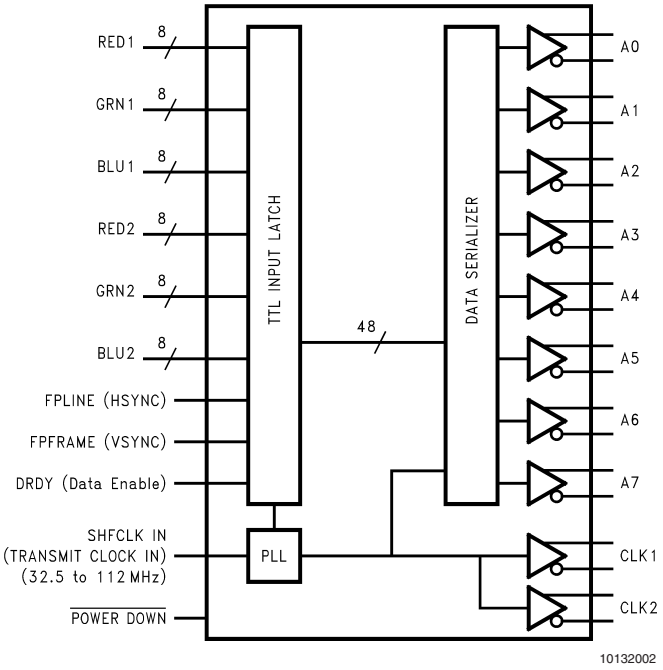
The DS90C387A transmitter provides a second LVDS output clock. Both LVDS clocks are identical. This feature supports backward compatibility with the previous generation of FPD-Link Receivers - the second clock allows the transmitter to interface to panels using a 'dual pixel' configuration of two 24-bit or 18-bit FPD-Link receivers.

This chipset is an ideal means to solve EMI and cable size problems for high-resolution flat panel applications. It provides a reliable interface based on LVDS technology that delivers the bandwidth needed for high-resolution panels while maximizing bit times, and keeping clock rates low to reduce EMI and shielding requirements. For more details, please refer to the "Applications Information" section of this datasheet.

Features

- Supports SVGA through QXGA panel resolutions
- 32.5 to 112/170MHz clock support
- Drives long, low cost cables
- Up to 5.7 Gbps bandwidth
- Pre-emphasis reduces cable loading effects
- Dual pixel architecture supports interface to GUI and timing controller; optional single pixel transmitter inputs support single pixel GUI interface
- Transmitter rejects cycle-to-cycle jitter
- 5V tolerant on data and control input pins
- Programmable transmitter data and control strobe select (rising or falling edge strobe)
- Backward compatible with FPD-Link
- Compatible with ANSI/TIA/EIA-644-1995 LVDS Standard

Generalized Transmitter Block Diagram



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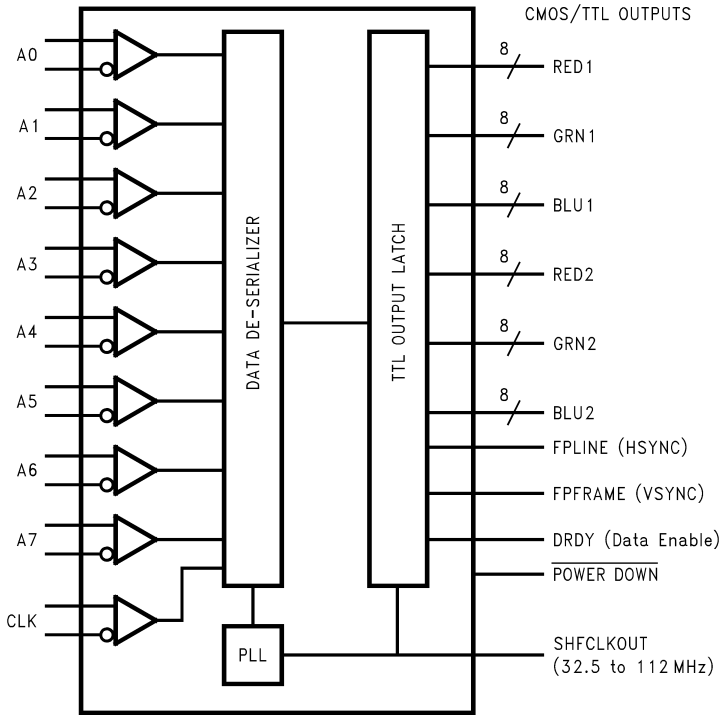
Generalized Receiver Block Diagram



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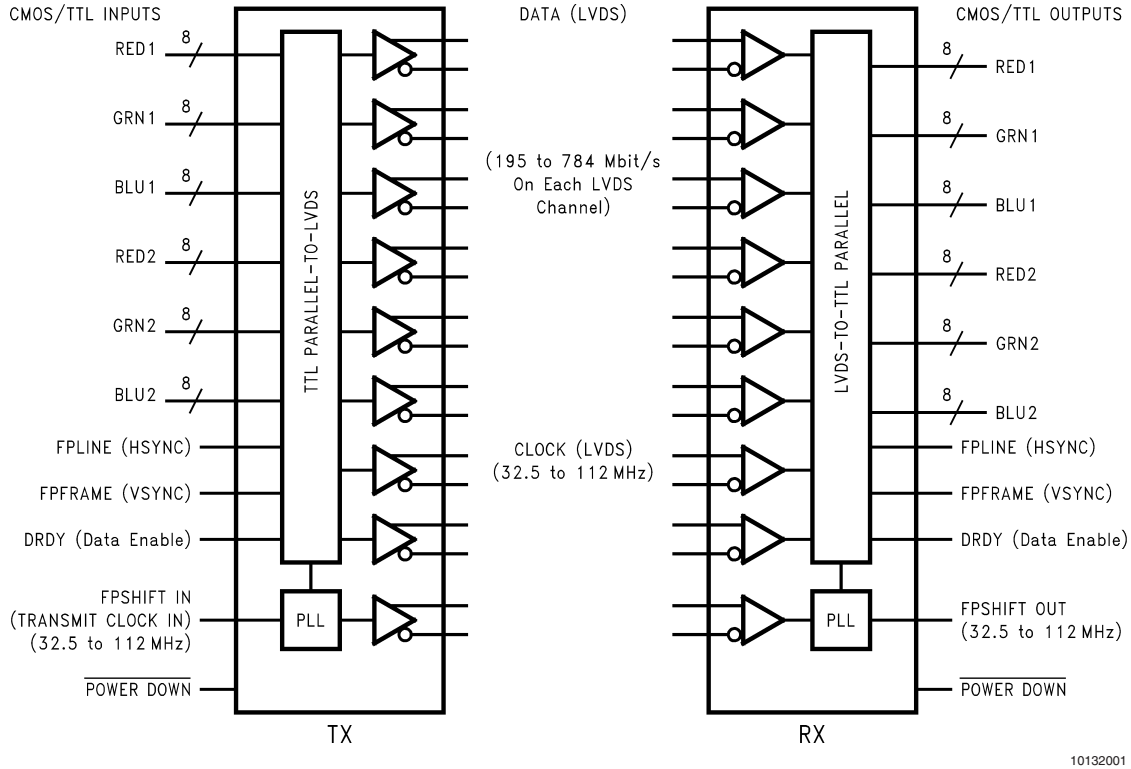
Generalized Block Diagrams



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +4V
CMOS/TTL Input Voltage	−0.3V to +5.5V
CMOS/TTL Output Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Receiver Input Voltage	−0.3V to +3.6V
LVDS Driver Output Voltage	−0.3V to +3.6V
LVDS Output Short Circuit Duration	Continuous
Junction Temperature	+150˚C
Storage Temperature	−65˚C to +150˚C
Lead Temperature (Soldering, 4 sec.)	+260˚C
Maximum Package Power Dissipation Capacity @ 25˚C	
100 TQFP Package:	
DS90C387A	2.8W
DS90CF388A	2.8W
Package Derating:	
DS90C387 A	18.2mW/˚C above +25˚C
DS90CF388 A	18.2mW/˚C above +25˚C
ESD Rating:	
DS90C387A	
(HBM, 1.5kΩ, 100pF)	> 6 kV
(EIAJ, 0Ω, 200pF)	> 300 V
DS90CF388A	
(HBM, 1.5kΩ, 100pF)	> 2 kV
(EIAJ, 0Ω, 200pF)	> 200 V

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−10	+25	+70	˚C
Receiver Input Range	0		2.4	V
Supply Noise Voltage (V_{CC})			100	mV_{p-p}

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS/TTL DC SPECIFICATIONS (Tx inputs, Rx outputs, control inputs and outputs)						
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA	2.7	2.9		V
		I_{OH} = −2 mA	2.7	2.85		V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA		0.1	0.3	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA		−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = 0.4V, 2.5V or V_{CC}		+1.8	+15	µA
		V_{IN} = GND	−15	0		µA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V			−120	mA
LVDS DRIVER DC SPECIFICATIONS						
V_{OD}	Differential Output Voltage	R_L = 100Ω	250	345	450	mV
ΔV_{OD}	Change in V_{OD} between Complimentary Output States				35	mV
V_{OS}	Offset Voltage		1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between Complimentary Output States				35	mV
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω		−3.5	−10	mA
I_{OZ}	Output TRI-STATE® Current	$\overline{PD}$ = 0V, V_{OUT} = 0V or V_{CC}		±1	±10	µA
LVDS RECEIVER DC SPECIFICATIONS						
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V			+100	mV
V_{TL}	Differential Input Low Threshold		−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V, V_{CC} = 3.6V			±10	µA
		V_{IN} = 0V, V_{CC} = 3.6V			±10	µA

Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
TRANSMITTER SUPPLY CURRENT							
ICCTW	Transmitter Supply Current Worst Case	R_L = 100Ω, C_L = 5 pF, Worst Case Pattern (*Figures 1, 3*), DUAL=High (48-bit RGB)	f = 32.5 MHz		115	160	mA
			f = 65 MHz		145	200	mA
			f = 85 MHz		165	230	mA
			f = 112 MHz		210	260	mA
	Transmitter Supply Current 16 Grayscale	100Ω, C_L = 5 pF, 16 Grayscale Pattern (*Figures 2, 3*), DUAL=High (48-bit RGB)	f = 32.5 MHz		92	140	mA
			f = 65 MHz		100	150	mA
			f = 85 MHz		110	170	mA
			f = 112 MHz		130	190	mA
ICCTZ	Transmitter Supply Current Power Down	$\overline{PD}$ = Low Driver Outputs in TRI-STATE under Powerdown Mode			4.8	50	µA
RECEIVER SUPPLY CURRENT							
ICCRW	Receiver Supply Current Worst Case	C_L = 8 pF, Worst Case Pattern (*Figures 1, 4*), DUAL = High (48-bit RGB)	f = 32.5 MHz		100	140	mA
			f = 65 MHz		150	200	mA
			f = 85 MHz		170	220	mA
			f = 112 MHz		185	240	mA
ICCRG	Receiver Support Current 16 Grayscale	C_L = 8 pF, 16 Grayscale Pattern (*Figures 2, 4*), DUAL = High (48-bit RGB)	f = 32.5 MHz		45	80	mA
			f = 65 MHz		60	110	mA
			f = 85 MHz		85	130	mA
			f = 112 MHz		110	160	mA
ICCRZ	Receiver Supply Current Power Down	$\overline{PD}$ = Low Receiver Outputs stay low during Powerdown mode.			255	300	µA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for V_{CC} = 3.3V and T_A = +25˚C.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

Recommended Transmitter Input Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter		Min	Typ	Max	Units
TCIT	TxCLK IN Transition Time (*Figure 5*)	DUAL=Gnd or Vcc	1.0	2.0	3.0	ns
		DUAL=1/2Vcc	1.0	1.5	1.7	ns
TCIP	TxCLK IN Period (*Figure 6*)	DUAL=Gnd or Vcc	8.928	T	30.77	ns
		DUAL=1/2Vcc	5.88		15.38	ns
TCIH	TxCLK in High Time (*Figure 6*)		0.35T	0.5T	0.65T	ns
TCIL	TxCLK in Low Time (*Figure 6*)		0.35T	0.5T	0.65T	ns
TXIT	TxIN Transition Time		1.5		6.0	ns

Transmitter Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter		Min	Typ	Max	Units
LLHT	LVDS Low-to-High Transition Time (*Figure 3*), PRE = 0.75V (disabled)			0.14	0.7	ns
	LVDS Low-to-High Transition Time (*Figure 3*), PRE = Vcc (max)			0.11	0.6	ns
LHLT	LVDS High-to-Low Transition Time (*Figure 3*), PRE = 0.75V (disabled)			0.16	0.8	ns
	LVDS High-to-Low Transition Time (*Figure 3*), PRE = Vcc (max)			0.11	0.7	ns
TBIT	Transmitter Output Bit Width	DUAL=Gnd or Vcc		1/7 TCIP		ns
		DUAL=1/2Vcc		2/7 TCIP		ns
TPPOS	Transmitter Pulse Positions - Normalized	f = 33 to 70 MHz	–250	0	+250	ps
		f = 70 to 112 MHz	–200	0	+200	ps
TCCS	TxOUT Channel to Channel Skew			100		ps
TSTC	TxIN Setup to TxCLK IN (*Figure 6*)		2.7			ns
THTC	TxIN Hold to TxCLK IN (*Figure 6*)		0			ns
TJCC	Transmitter Jitter Cycle-to-cycle (*Figures 13, 14*) (Note 5), DUAL=Vcc	f = 112 MHz		85	100	ps
		f = 85 MHz		60	75	ps
		f = 65 MHz		70	80	ps
		f = 56 MHz		100	120	ps
		f = 32.5 MHz		75	110	ps
TPLLS	Transmitter Phase Lock Loop Set (*Figure 8*)				10	ms
TPDD	Transmitter Powerdown Delay (*Figure 10*)				100	ns

Receiver Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter		Min	Typ	Max	Units
CLHT	CMOS/TTL Low-to-High Transition Time (*Figure 4*), Rx data out			1.52	2.0	ns
	CMOS/TTL Low-to-High Transition Time (*Figure 4*), Rx clock out			0.5	1.0	ns
CHLT	CMOS/TTL High-to-Low Transition Time (*Figure 4*), Rx data out			1.7	2.0	ns
	CMOS/TTL High-to-Low Transition Time (*Figure 4*), Rx clock out			0.5	1.0	ns
RCOP	RxCLK OUT Period (*Figure 7*)		8.928	T	30.77	ns
RCOH	RxCLK OUT High Time (*Figure 7*)(Note 4)	f = 112 MHz	3.5			ns
		f = 85 MHz	4.5			ns
RCOL	RxCLK OUT Low Time (*Figure 7*)(Note 4)	f = 112 MHz	3.5			ns
		f = 85 MHz	4.5			ns
RSRC	RxOUT Setup to RxCLK OUT (*Figure 7*)(Note 4)	f = 112 MHz	2.4			ns
		f = 85 MHz	3.0			ns
RHRC	RxOUT Hold to RxCLK OUT (*Figure 7*)(Note 4)	f = 112 MHz	3.4			ns
		f = 85 MHz	4.75			ns
RPLLS	Receiver Phase Lock Loop Set (*Figure 9*)				10	ms
RPDD	Receiver Powerdown Delay (*Figure 11*)				1	µs
RSKM	Receiver Skew Margin (*Figure 12*) (Notes 4, 6),	f = 112 MHz	170			ps
		f = 100 MHz	170	240		ps
		f = 85MHz	300	350		ps
		f = 66MHz	300	350		ps

Note 4: The Minimum and Maximum Limits are based on statistical analysis of the device performance over voltage and temperature ranges. This parameter is functionally tested on Automatic Test Equipment (ATE). ATE is limited to 85MHz. A sample of characterization parts have been bench tested at 112MHz to verify functional performance.

Note 5: The limits are based on bench characterization of the device's jitter response over the power supply voltage range. Output clock jitter is measured with a cycle-to-cycle jitter of ±3ns applied to the input clock signal while data inputs are switching (see figures 15 and 16). A jitter event of 3ns, represents worse case jump in the clock edge from most graphics VGA chips currently available. This parameter is used when calculating system margin as described in AN-1059.

Note 6: Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account transmitter output pulse positions (min and max) and the receiver input setup and hold time (internal data sampling window - RSPOS). This margin allows for LVDS interconnect skew, inter-symbol interference (both dependent on type/length of cable) and clock jitter.

RSKM ≥ cable skew (type, length) + source clock jitter (cycle to cycle).

AC Timing Diagrams

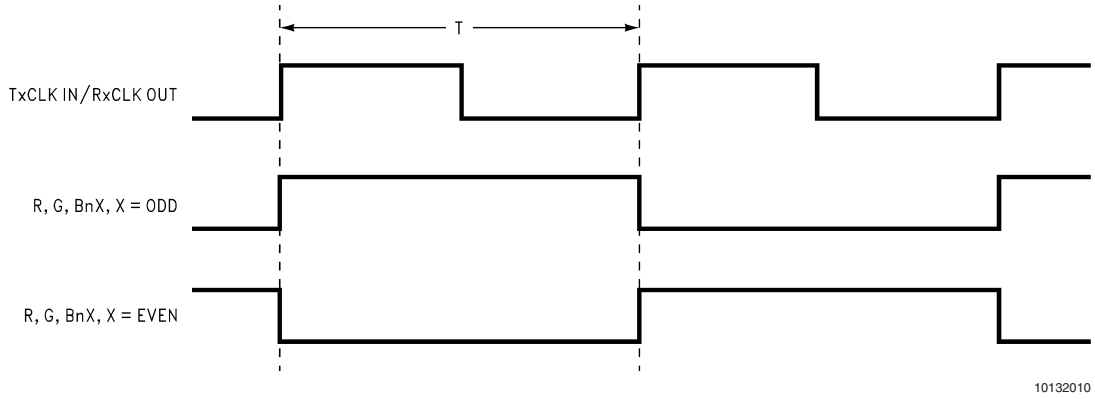


FIGURE 1. "Worst Case" Test Pattern

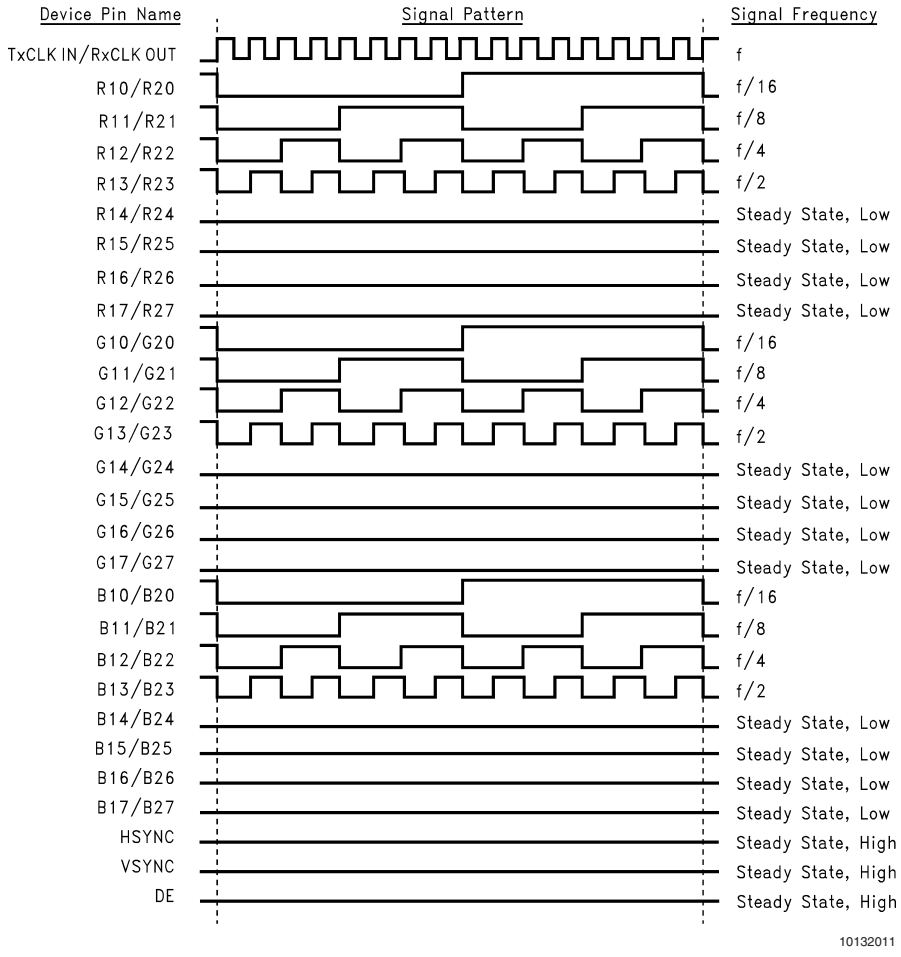


FIGURE 2. "16 Grayscale" Test Pattern (Notes 7, 8, 9)

Note 7: The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

Note 8: The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

Note 9: *Figures 1, 2* show a falling edge data strobe (TxCLK IN/RxCLK OUT).

AC Timing Diagrams (Continued)

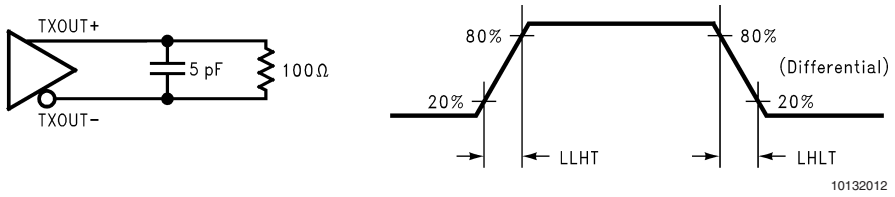


FIGURE 3. DS90C387A (Transmitter) LVDS Output Load and Transition Times

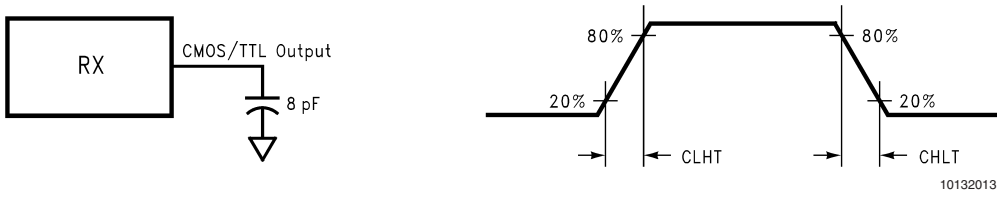


FIGURE 4. DS90CF388A (Receiver) CMOS/TTL Output Load and Transition Times

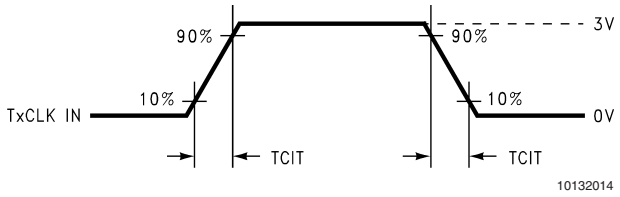


FIGURE 5. DS90C387A (Transmitter) Input Clock Transition Time

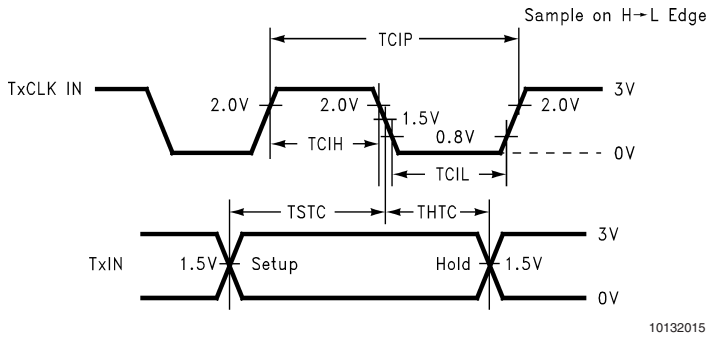


FIGURE 6. DS90C387A (Transmitter) Setup/Hold and High/Low Times (Falling Edge Strobe)

AC Timing Diagrams (Continued)

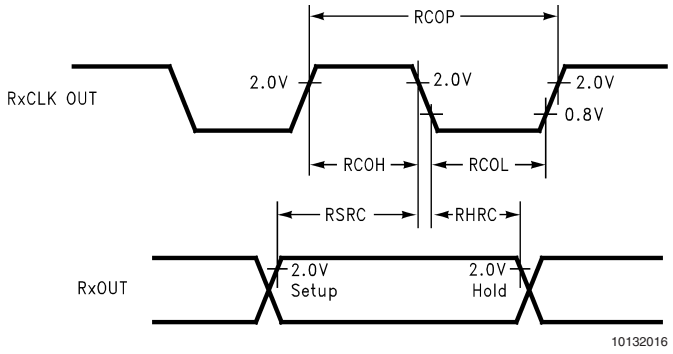


FIGURE 7. DS90CF388A (Receiver) Setup/Hold and High/Low Times

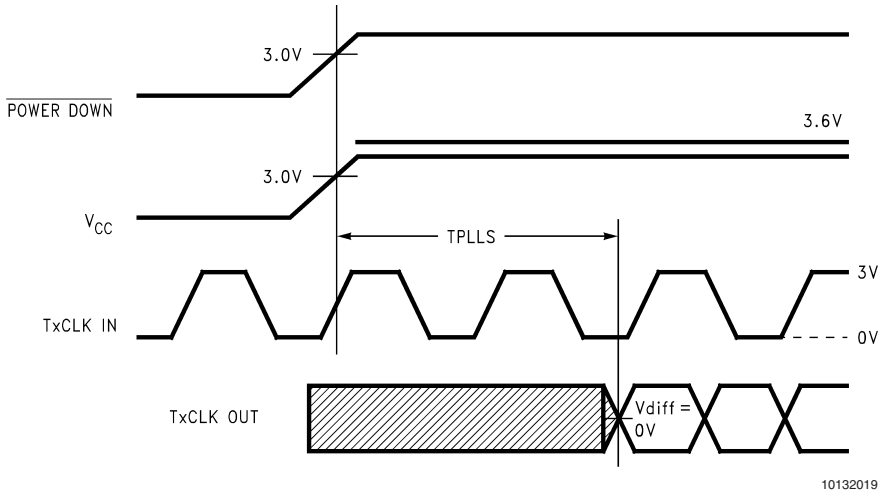


FIGURE 8. DS90C387A (Transmitter) Phase Lock Loop Set Time

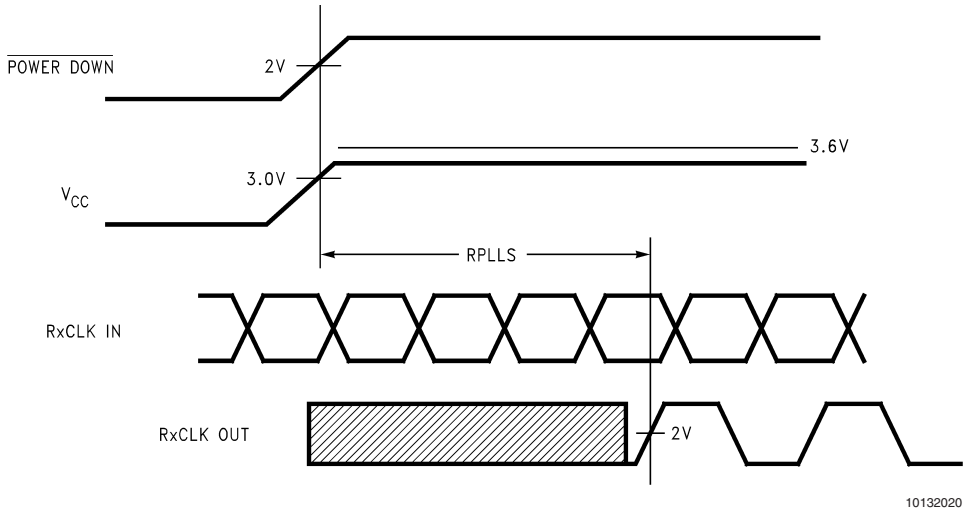


FIGURE 9. DS90CF388A (Receiver) Phase Lock Loop Set Time

AC Timing Diagrams (Continued)

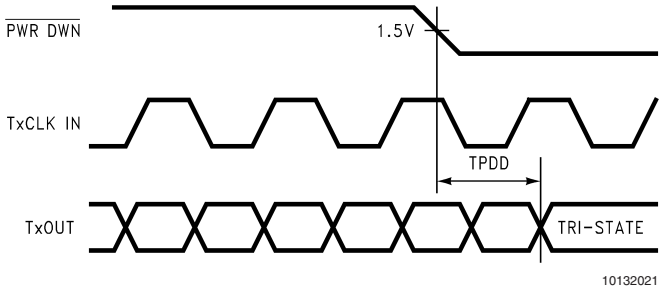


FIGURE 10. Transmitter Power Down Delay

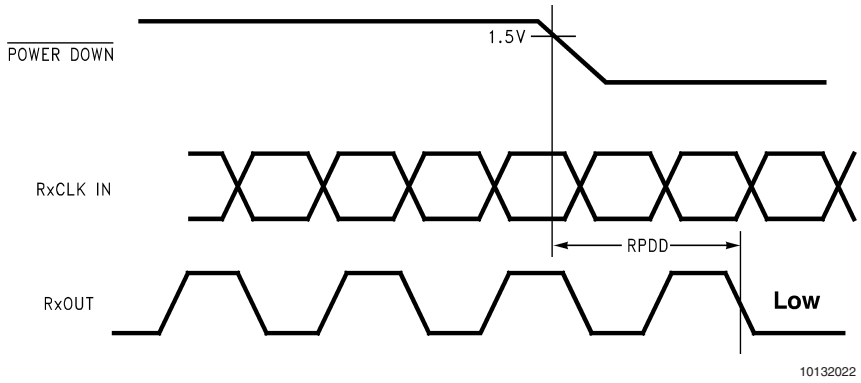
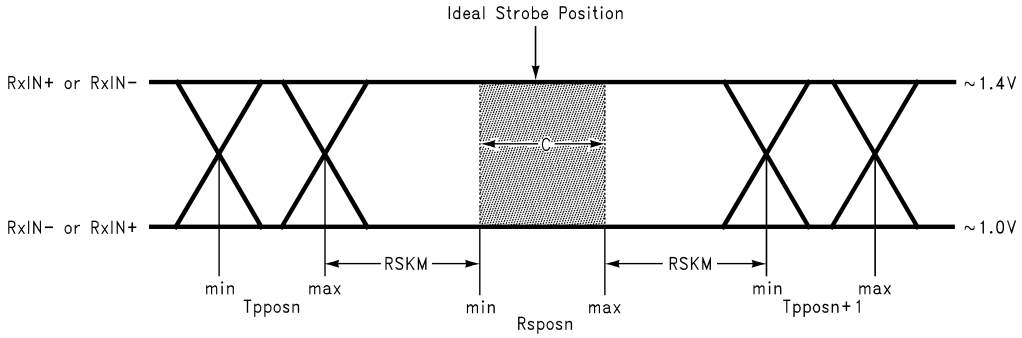


FIGURE 11. Receiver Power Down Delay



C — Setup and Hold Time (Internal data sampling window) defined by RSPOS (receiver input strobe position) min and max

TPPOS — Transmitter output pulse position (min and max)

RSKM ≥ Cable Skew (type, length) + LVDS Source Clock Jitter (cycle to cycle) + ISI (Inter-symbol interference)

■ Cable Skew — typically 10 ps to 40 ps per foot, media dependent

■ TJCC — Cycle-to-cycle LVDS Output jitter (TJCC) is less than 100 ps (worse case estimate).

■ ISI is dependent on interconnect length; may be zero

See Applications Informations section for more details.

FIGURE 12. Receiver Skew Margin

AC Timing Diagrams (Continued)

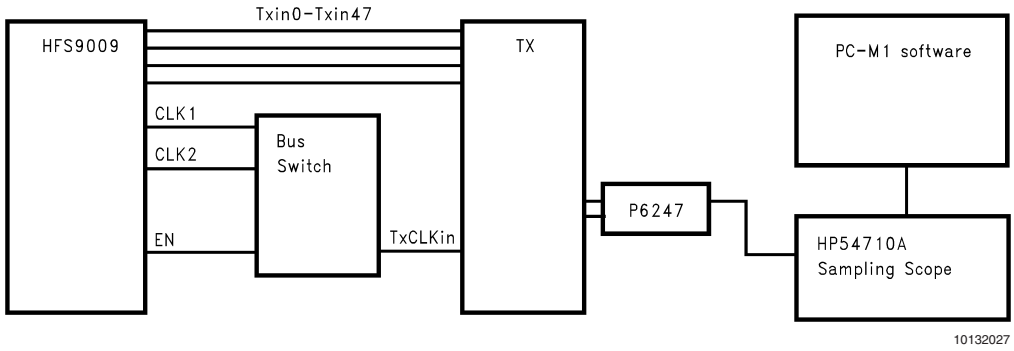


FIGURE 13. TJCC Test Setup - DS90C387A

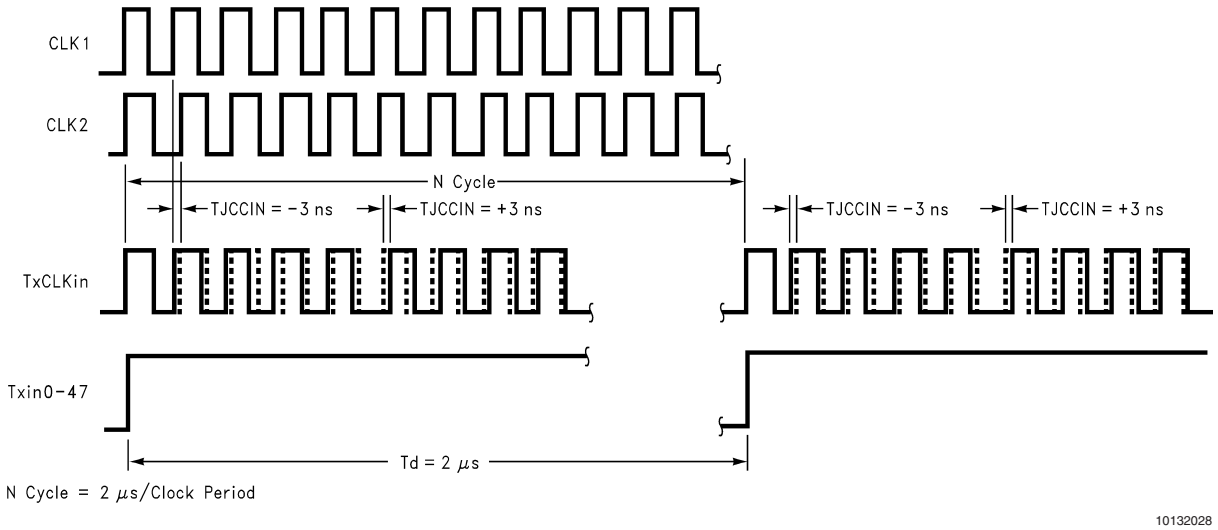


FIGURE 14. Timing Diagram of the Input Cycle-to-Cycle Clock Jitter

DS90C387A Pin Descriptions — FPD Link Transmitter

Pin Name	I/O	No.	Description
Rn, Gn, Bn, DE, HSYNC, VSYNC	I	51	TTL level input. This includes: 16 Red, 16 Green, 16 Blue, and 3 control lines HSYNC, VSYNC, DE (Data Enable).(Note 10)
AnP	O	8	Positive LVDS differential data output.
AnM	O	8	Negative LVDS differential data output.
CLKIN	I	1	TTL level clock input.
R_FB	I	1	Programmable data strobe select. Rising data strobe edge selected when input is high. (Note 10)
R_FDE	I	1	Programmable control (DE) strobe select. Tied high for data active when DE is high. (Note 10)
CLK1P	O	1	Positive LVDS differential clock output.
CLK1M	O	1	Negative LVDS differential clock output.
$\overline{PD}$	I	1	TTL level input. Assertion (low input) tri-states the outputs, ensuring low current at power down. (Note 10)
PLLSEL	I	1	PLL range select. This pin must be tied to V_{CC} for auto-range. NC or tied to Ground is reserved for future use. Typical shift point is between 55 and 68 MHz. (Notes 10, 11)
PRE	I	1	Pre-emphasis level select. Pre-emphasis is active when input is tied to V_{CC} through external pull-up resistor. Resistor value determines pre-emphasis level (see table in application section). For normal LVDS drive level (No pre-emphasis) leave this pin open (do not tie to ground).(Note 10)
DUAL	I	1	Three-mode select for dual pixel, single pixel, or single pixel input to dual pixel output operation. Single pixel mode when input is low (only LVDS channels A0 thru A3 and CLK1 are active) for power savings. Dual mode is active when input is high. Single in - dual out when input is at 1/2 Vcc. (Note 10)
V_{CC}	I	4	Power supply pins for TTL inputs and digital circuitry.
GND	I	6	Ground pins for TTL inputs and digital circuitry.
$PLLV_{CC}$	I	2	Power supply pin for PLL circuitry.
PLLGND	I	3	Ground pins for PLL circuitry.
$LVDSV_{CC}$	I	3	Power supply pin for LVDS outputs.
LVDSGND	I	4	Ground pins for LVDS outputs.
CLK2P/NC	O	1	Additional positive LVDS differential clock output. Identical to CLK1P. No connect if not used.
CLK2M/NC	O	1	Additional negative LVDS differential clock output. Identical to CLK1M. No connect if not used.

Note 10: Inputs default to “low” when left open due to internal pull-down resistor.

Note 11: The PLL range shift point is in the 55 - 68 MHz range, typically the shift will occur during the lock time.

DS90CF388A Pin Descriptions — FPD Link Receiver

Pin Name	I/O	No.	Description
AnP	I	8	Positive LVDS differential data inputs.
AnM	I	8	Negative LVDS differential data inputs.
Rn, Gn, Bn, DE, HSYNC, VSYNC	O	51	TTL level data outputs. This includes: 16 Red, 16 Green, 16 Blue, and 3 control lines— HSYNC (LP), VSYNC (FLM), DE (Data Enable).
RxCLK INP	I	1	Positive LVDS differential clock input.
RxCLK INM	I	1	Negative LVDS differential clock input.
RxCLK OUT	O	1	TTL level clock output. The falling edge acts as data strobe.
R_FDE	I	1	Programmable control (DE) strobe select. Tied high for data active when DE is high. (Note 10)
PLLSEL	I	1	PLL range select. This pin must be tied to V_{CC} for auto-range. NC or tied to Ground is reserved for future use. Typical shift point is between 55 and 68 MHz. (Notes 10, 11)
$\overline{PD}$	I	1	TTL level input. When asserted (low input) the receiver data outputs are low and clock output is high. (Note 10)
STOPCLK	O	1	Indicates receiver clock input signal is not present with a logic high. With a clock input present, a low logic is indicated.
V_{CC}	I	6	Power supply pins for TTL outputs and digital circuitry.
GND	I	10	Ground pins for TTL outputs and digital circuitry
$PLLV_{CC}$	I	1	Power supply for PLL circuitry.
PLLGND	I	2	Ground pin for PLL circuitry.
$LVDSV_{CC}$	I	2	Power supply pin for LVDS inputs.
LVDSGND	I	3	Ground pins for LVDS inputs.
CNTLE, CNTLF		2	No Connect. Make NO Connection to these pins - leave these pins open, do not tie to ground or V_{CC}.

LVDS Interface / TFT Data (Color) Mapping

Different color mapping options exist. See National Application Notes 1127 and 1163 for details.

The LVDS Clock waveshape is shown in *Figure 15*. Note that the rising edge of the LVDS clock occurs two LVDS sub symbols before the current cycle of data. The clock is compose of a 4 LVDS sub symbol HIGH time and a 3 LVDS sub symbol LOW time. The respective pin (transmitter and receiver) names are show in *Figure 15*. As stated above these names are not the color mapping information (MSB/LSB) but pin names only.

Inputs B17 and B27 are double wide bits. If using the DS90CF388A, this bits are sampled in the back half of the bit only. Also, the DE signal is mapped to two LVDS sub symbols. The DS90CF388A only samples the DE bit on channel A2. Two FPD-Link receivers may also be used in place of the DS90CF388A, since the DS90C387A provides two LVDS clocks. If this is the case, the FPD-Link receiver datasheet needs to be consulted for recovery mapping information. In this application, it is possible to recover two signals of: DE, B17 and B27 from the transmitter.

There are two reserved bits (RES). The DS90CF388A ignores these bits. If using separate FPD-Link receivers, the corresponding receiver outputs for these two bits should be left open (NC).

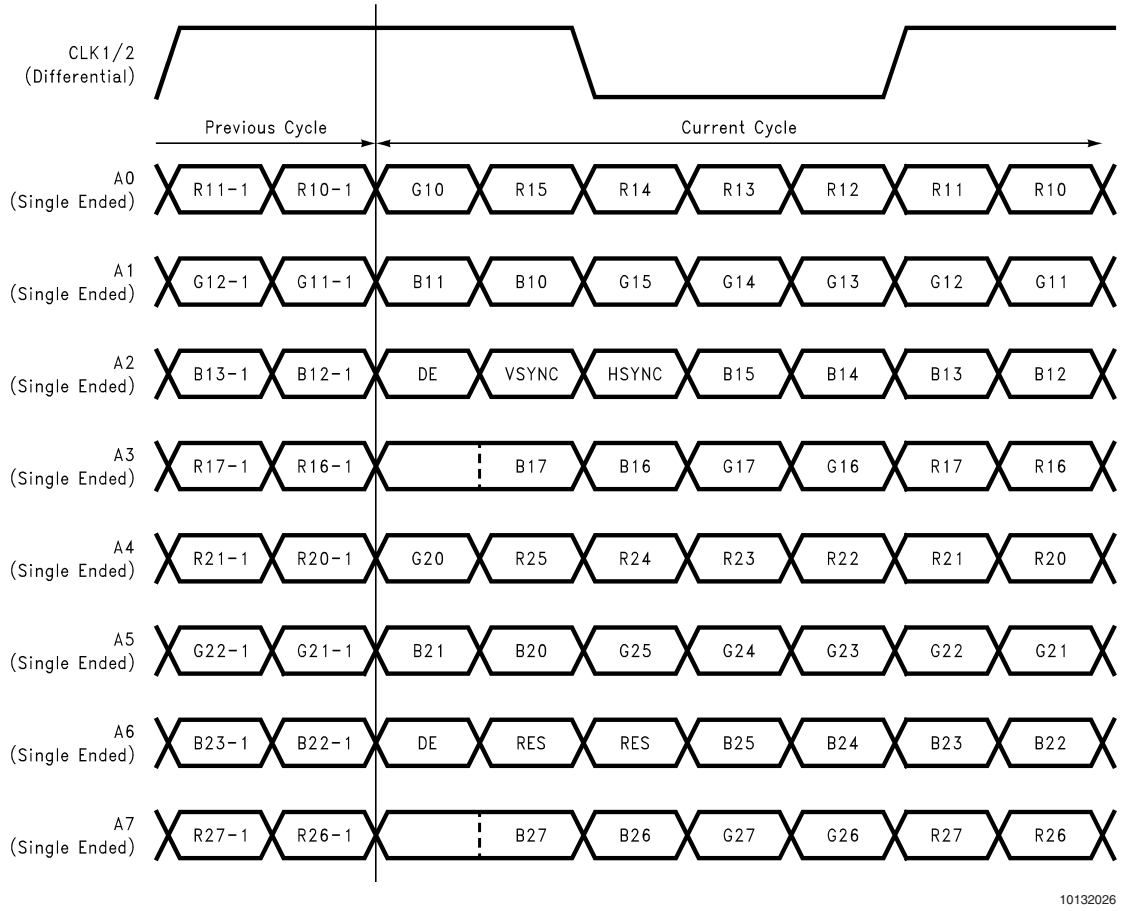


FIGURE 15. TTL Data Inputs Mapped to LVDS Outputs 387A/388A

Applications Information

HOW TO CONFIGURE THE DS90C387A AND DS90CF388A FOR MOST COMMON APPLICATION

1. To configure for single input pixel-to-dual pixel output application, the DS90C387 “DUAL” pin must be set to 1/2 Vcc=1.65V. This may be implemented using pull-up and pull-down resistors of 10kΩ. In this configuration, the input signals (single pixel) are split into odd and even pixel (dual pixels) starting with the odd (first) pixel outputs A0-to-A3 the next even (second) pixel outputs to A4-to-A7. The splitting of the data signal also starts with DE (data enable) transitioning from logic low to high indicating active data. The "R_FDE" pin must be set high in this case. The number of clock cycles during blanking must be an EVEN number. This configuration will allow the user to interface to an LDI receiver (DS90CF388A) or to two FPD-Link ’notebook’ receivers (DS90CF384A or DS90CF386).

2. To configure for single pixel or dual pixel application using the DS90C387A/DS90CF388A, the “DUAL” pin must be set to Vcc (dual) or Gnd (single). In dual mode, the transmitter-DS90C387A has two LVDS clock outputs enabling an interface to two FPD-Link ’notebook’ receivers (DS90CF384A or DS90CF386). In single mode, outputs A4-to-A7 and CLK2 are disabled which reduces power dissipation.

The DS90CF388A is able to support single or dual pixel interface up to 112MHz operating frequency. This receiver may also be used to interface to a VGA controller with an integrated LVDS transmitter.

TRANSMITTER FEATURES

The transmitter is designed to reject cycle-to-cycle jitter which may be seen at the transmitter input clock. Very low cycle-to-cycle jitter is passed on to the transmitter outputs. This significantly reduces the impact of jitter provided by the input clock source, and improves the accuracy of data sampling.

The transmitter is offered with programmable edge data strobes for convenient interface with a variety of graphics controllers. The transmitter can be programmed for rising edge strobe or falling edge strobe through a dedicated pin. A rising edge transmitter will inter-operate with a falling edge receiver without any translation logic.

PRE-EMPHASIS

Pre-Emphasis adds extra current during LVDS logic transition to reduce the cable loading effects. Pre-emphasis strength is set via a DC voltage level applied from min to max (0.75V to Vcc) at the “PRE” pin. A higher input voltage on the ”PRE” pin increases the magnitude of dynamic current during data transition. The “PRE” pin requires one pull-up resistor (Rpre) to Vcc in order to set the DC level. There is an internal resistor network, which cause a voltage drop. Please refer to the tables below to set the voltage level.

TABLE 1. Pre-Emphasis DC Voltage Level With (Rpre)

Rpre	Resulting PRE Voltage	Effects
1MΩ or NC	0.75V	Standard LVDS
50kΩ	1.0V	
9kΩ	1.5V	50% pre-emphasis
3kΩ	2.0V	
1kΩ	2.6V	
100Ω	Vcc	100% pre-emphasis

TABLE 2. Pre-Emphasis Needed Per Cable Length

Frequency	PRE Voltage	Typical cable length
112MHz	1.0V	2 meters
112MHz	1.5V	5 meters
80MHz	1.0V	2 meters
80MHz	1.2V	7 meters
65MHz	1.5V	10 meters
56MHz	1.0V	10 meters

Note 12: This is based on testing with standard shield twisted pair cable. The amount of pre-emphasis will vary depending on the type of cable, length and operating frequency.

RSKM - RECEIVER SKEW MARGIN

RSKM is a chipset parameter and is explained in AN-1059 in detail. It is the difference between the transmitter’s pulse position and the receiver’s strobe window. RSKM must be greater than the summation of: Interconnect skew, LVDS Source Clock Jitter (TJCC), and ISI (if any). See *Figure 12*. Interconnect skew includes PCB traces differences, connector skew and cable skew for a cable application. PCB trace and connector skew can be compensated for in the design of the system. Cable skew is media type and length dependant.

POWER DOWN

Both transmitter and receiver provide a power down feature. When asserted current draw through the supply pins is minimized and the PLLs are shut down. The transmitter outputs are in TRI-STATE when in power down mode. The receiver outputs are forced to a active LOW state when in the power down mode. (See Pin Description Tables). The $\overline{PD}$ pin should be driven HIGH to enable the device once V_{CC} is stable.

Applications Information (Continued)

DS90C387/DS90CF388

The DS90C387A/CF388A chipset is electrically similar to the DS90C387/CF388. The DS90C387/CF388 is intended for improved support of longer cable drive. Cable drive is enhanced with a user selectable pre-emphasis feature that provides additional output current during transitions to counteract cable loading effects. Optional DC balancing on a cycle-to-cycle basis, is also provided to reduce ISI (Inter-Symbol Interference). With pre-emphasis and DC balancing, a low distortion eye-pattern is provided at the receiver end of the cable. A cable deskew capability has been added to deskew long cables of pair-to-pair skew of up to +/−1 LVDS data bit time (up to 80 MHz Clock Rate). These three enhancements allow cables 5+ meters in length to be driven depending upon media and clock rate.

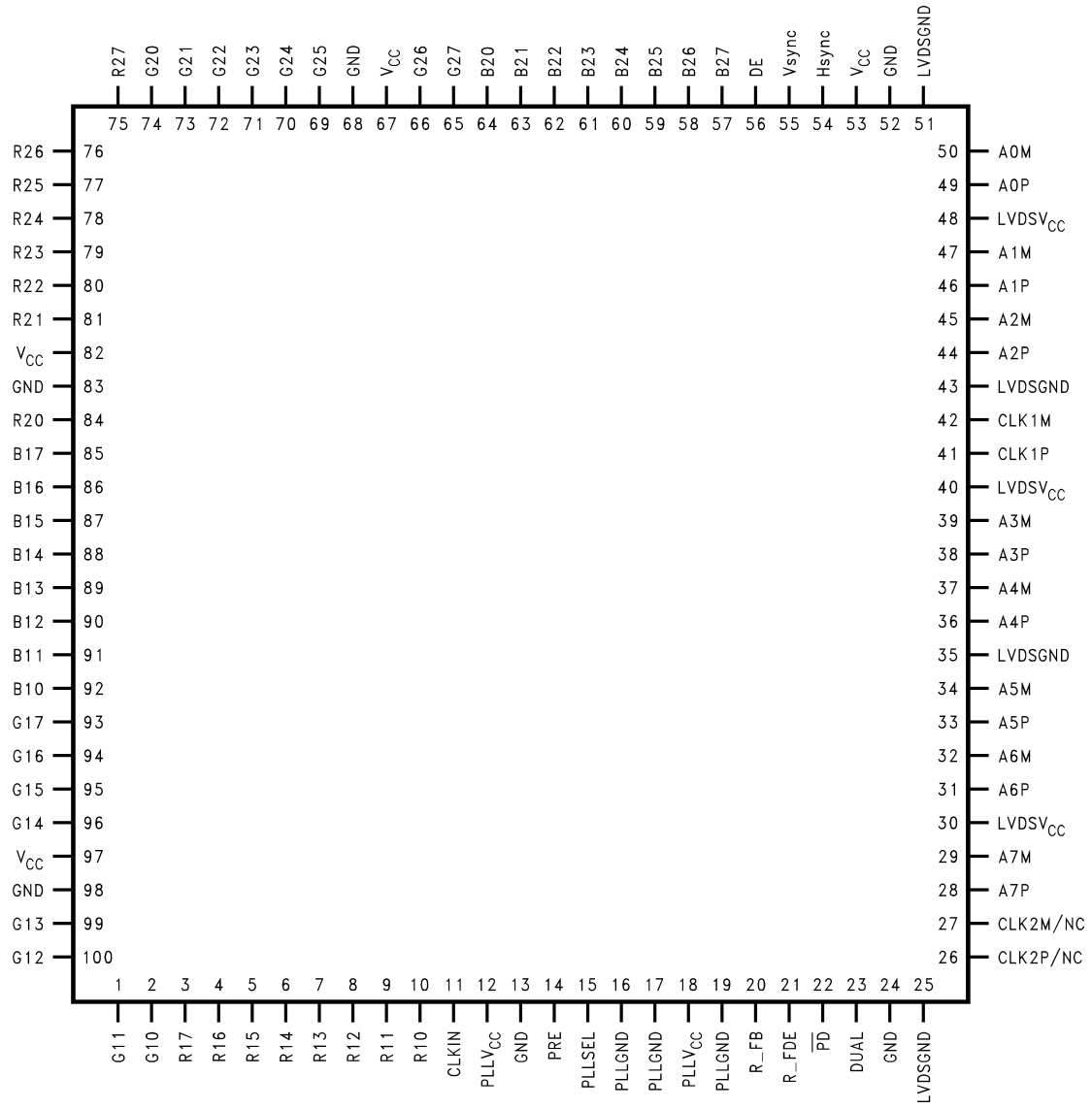
Configuration Table

TABLE 3. Transmitter / Receiver configuration table

Pin	Condition	Configuration
R_FB (Tx only)	R_FB = V_{CC}	Rising Edge Data Strobe
	R_FB = GND	Falling Edge Data Strobe
R_FDE (both Tx and Rx)	R_FDE = V_{CC}	Active data DE = High
	R_FDE = GND	Active data DE = Low
DUAL (Tx only)	DUAL=V_{CC}	48-bit color (dual pixel) support
	DUAL=1/2V_{CC}	Single-to-dual support
	DUAL=Gnd	24-bit color (single pixel) support

Pin Diagram

Transmitter-DS90C387A



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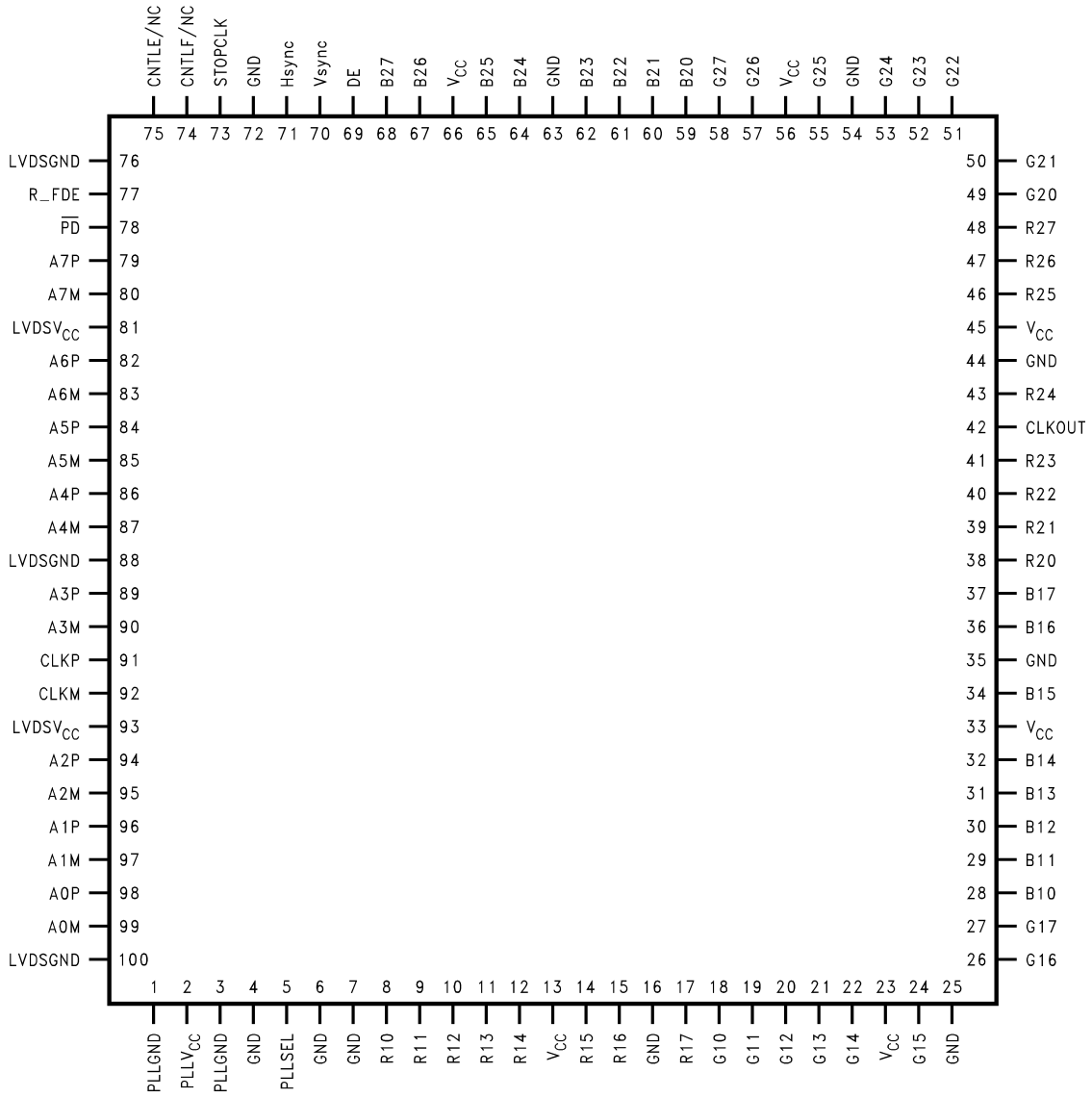
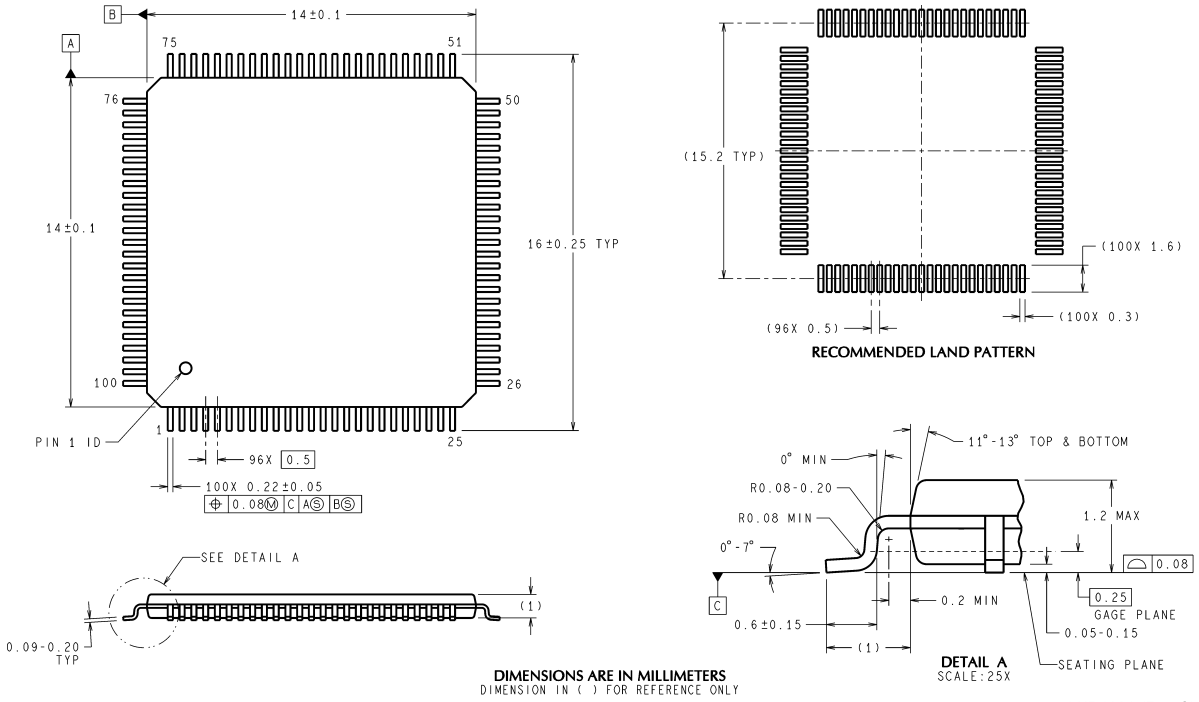
Pin Diagram

Receiver-DS90CF388A



10132007

Physical Dimensions inches (millimeters) unless otherwise noted



VJD100A (Rev C)

Dimensions show in millimeters
Order Number DS90C387AVJD and DS90CF388AVJD
NS Package Number VJD100A

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