FUJI Power Supply Control IC

Power Factor Correction

FA5601

Application Note

April-2011
Fuji Electric Co.,Ltd.

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   ▪ Measurement equipment ▪ Machine tools ▪ Audiovisual equipment ▪ Electrical home appliance
   ▪ Personal equipment ▪ Industrial robots etc.

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   ▪ Space equipment ▪ Aeronautic equipment ▪ Atomic control equipment
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7.

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CONTENTS

Note

- **The contents are subject to change without notice for specification changes or other reasons.**
- **Parts tolerance and characteristics are not defined in all application described in this Date book. When design an actual circuit for a product, you must determine parts tolerance and characteristics for safe and economical operation.**

1. Description

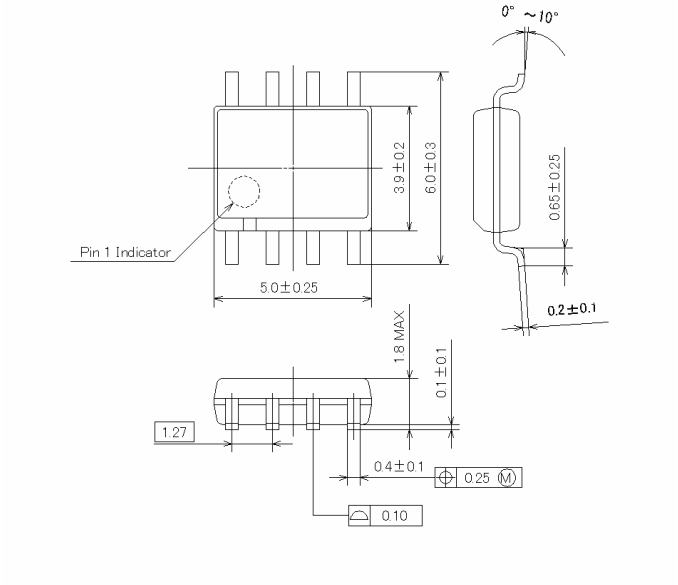
FA5601 is power-factor correction converter IC operating in critical conduction mode. It realizes low power consumption by using high voltage CMOS process. It is equipped with many fault protection functions such as FB short-circuit detection circuit which stops the operation when abnormal output voltage is detected.

2. Features

- Very Low Standby Power by disusing Input Voltage Detection Resistors
- High-precision over current protection: 0.65V±5%
- Improved power efficiency at light load due to Maximum Frequency Limitation
- No Audible Noise at Startup by dynamic OVP circuit
- Low current consumption by CMOS process
  Start-up : 80μA(max.), Operating : 2mA(typ.)
- Enabled to drive power MOSFET directly
  Output peak current, source : 0.5A, sink : 1A
- Open/short protection at feedback (FB) pin
- Under-voltage Lockout
  FA5601: 13V ON / 9V OFF
- Restart timer 30us(typ.)
- Standby function
- 8-pin package: SOP-8

3. Outline

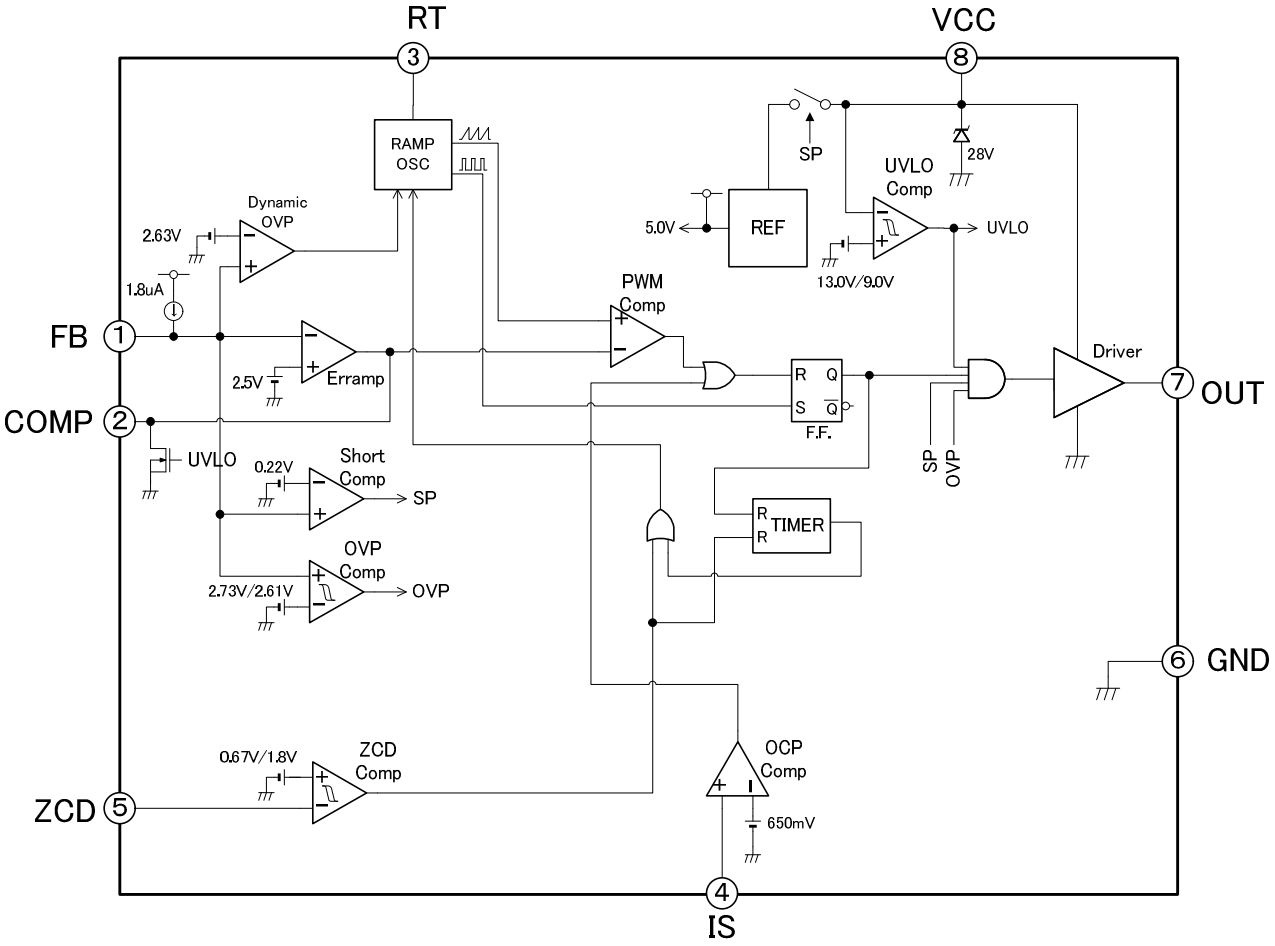
SOP-8



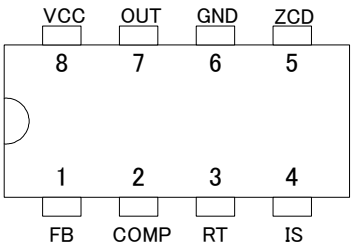
4. Type of FA5601

Type	Startup Threshold	Package
FA5601N	13V(typ.)	SOP-8

5. Block diagram



6. Pin assignment



Pin No.	Pin symbol	Function	Description
1	FB	Feedback Voltage Input	Inverting input for voltage error amplifier. Input terminal of converter output voltage.
2	COMP	Compensation	Output of error amplifier Phase compensator circuit is connected.
3	RT	Set Maximum on time	Set Maximum on time by connecting resistor
4	IS	Current Sense Input	Input for sensing current
5	ZCD	Zero Current Detection Input	Input for sensing inductor current
6	GND	Ground	Ground
7	OUT	Output	Output for driving a power MOSFET
8	VCC	Power Supply	Power supply for IC

7. Ratings and characteristics

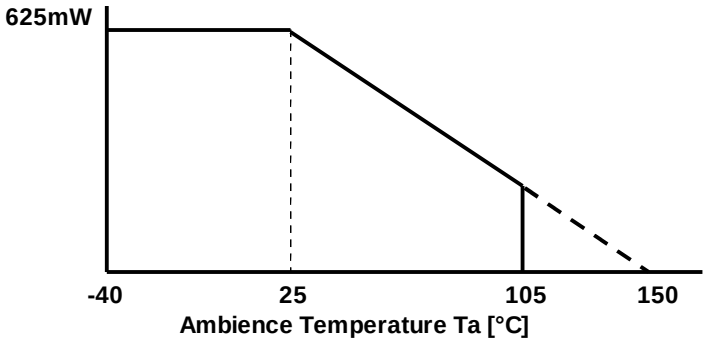
The contents are subject to change without notice. When using a product, be sure to obtain the latest specifications.

(1) Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Total Power Supply and Zener Current(VCC) *1	Icc+Iz	15	mA
Supply Voltage(VCC) *1	VCC	-0.3 to +28	V
OUT pin Voltage	VOUT	-0.3 to VCC+0.3	V
Output Current *1 Sink Source	Io	+1000 -500	mA mA
Output Peak Current *2	Io	Self Limiting	mA
Control terminal Input Voltage (FB,COMP,RT,IS)	Vinfb, Vincomp, Vinrt, Vinis	-0.3 to 5	V
Control terminal Input Current (FB,COMP,RT,IS)	Iinfb, Iincomp, Iinrt, Iinis	-100 to +100	μA
input Voltage (ZCD)	Vinzcd	-2 to 8.6	V
Input Current (ZCD) "H" Forward Current "L" Reverse Current	Iinzcd	+50 -10	mA mA
Power Dissipation (Ta=25°C)	Pd	625	mW
Operating Ambient Temperature	Ta	-40 to +105	°C
Operating Junction Temperature	Tj	-40 to +150	°C
Storage Temperature	Tstg	-40 to +150	°C

*1 The total loss shall not be exceeded.
*2 The period exceeding the sink current +1000mA and source current -500mA shall be within 100ns.

Maximum dissipation curve

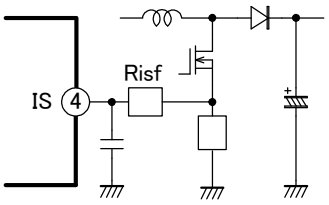


Package thermal resistor
θj-a = 200°C/W

(2) Recommended Operating Conditions

Item	Symbol	MIN	TYP	MAX	Unit
Supply Voltage	VCC	10	12	26	V
RT pin resistance	Rrt	39	82	150	kΩ
IS pin filter resistance *3	Risf	-	-	100	Ω
ZCD pin current	Izcd	-	-	±3	mA
Operating Ambient Temperature	Ta	-40	-	85	°C

*3 IS pin connected filter resistance



(3) Electrical Characteristics

(Unless otherwise specified, Tj=25°C, VCC=12V, V(FB)=1.0V, V(IS)=0V, V(ZCD)=0V, Rrt=82kΩ)

ERROR AMPLIFIER (FB,COMP Pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Voltage Feedback Input Threshold	Vfb		2.465	2.500	2.535	V
Line Regulation	Regline	VCC=10V to 26V	-20	-10	-	mV
Temperature stability	VdT	Tj=-40°C to +85°C	-	±0.5	-	mV/°C
Transconductance	Gm	V(FB)=2.25V, 2.75V V(COMP)=2.5V Gm=Icomp_2.75-Icomp_2.25/(2.75-2.25)	50	75	100	µmho
Output Current source sink	Icompso Icompsi	V(COMP)=2.5V Source:V(FB)=1.0V Sink:V(FB)=4.0V	-60 30	-40 50	-20 70	µA
COMP pin NMOS resistance (discharge resistance)	RcompUVLO	V(VCC)=8V to 12V V(COMP)=2V	2.0	4.0	6.0	kΩ

RAMP OSCILLATOR (RT Pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Maximum on-width	Tonmax	V(COMP)=5.0V V(FB)=Vfb	20	26	32	µs
Maximum oscillating frequency	Fmax	V(COMP)=0.8V	160	220	280	kHz
Maximum oscillating frequency operating voltage	Vfbmax		0.9	1.1	1.3	V
RT pin output voltage	Vrt		0.90	1.15	1.40	V

PWM COMPARATOR (COMP Pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
COMP pin Input threshold voltage	Vthcomp		0.6	0.7	0.8	V

OVERVOLTAGE PROTECTION COMPARATOR (FB Pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Static OVP threshold voltage	Vsovph	V(FB)=2.5V to 3.0V	1.070*Vfb	1.090*Vfb	1.105*Vfb	V
	Vsovpl	V(FB)=3.0V to 2.5V	1.025*Vfb	1.045*Vfb	1.065*Vfb	V
	Vsovphys	Vsovph-Vsovpl	0.020*Vfb	0.040*Vfb	0.060*Vfb	V
Dynamic OVP threshold voltage	Vdovp	V(FB)=2.5V to 3.0V Ton=Tonmax*70%	1.025*Vfb	1.050*Vfb	1.075*Vfb	V
Static to Dynamic OVP Hysteresis voltage	Vhyssd	Vsovph-Vdovp	0.020*Vfb	0.040*Vfb	0.060*Vfb	V

FB SHORT DETECTION COMPARATOR (FB Pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
FB pin Input threshold voltage	Vthfb	Vin Increasing DC Input Voltage	0.10	0.22	0.50	V
Pull-up current	Ipullup	V(FB)=2.5V	-2.4	-1.8	-1.2	µA

CURRENT SENSE COMPARATOR (IS Pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
IS pin Input threshold voltage	Vthish	Vin Increasing DC Input Voltage	0.63	0.65	0.67	V
IS pin Input threshold voltage temperature characteristics	Vthishdt	Tj=-40°C to +85°C	-	±1	±2	%
Output delay time	Tphl		-	180	500	ns

ZERO CURRENT DETECTION (ZCD pin)

Item		Symbol	Condition	MIN	TYP	MAX	Unit
ZCD pin Input threshold voltage	High	Vthzcdh	Vin Increasing DC Input Voltage	1.65	1.8	1.95	V
	Low	Vthzcdl	Vin Decreasing DC Input Voltage	0.52	0.67	0.82	V
Hysteresis width		Vhyszcd		1.03	1.13	1.23	V
Input clamp voltage		Vih	Isink=3.0mA	7.0	7.6	8.2	V
		Vil	Isource=-3.0mA	-1.6	-1.0	-0.4	V
Minimum detected pulse width		Tmw	f=110kHz ZCD pulse high level=2V low level=0.3V	100	-	-	ns
Zero current detection delay		Tzcd		-	100	300	ns
Maximum frequency lock time		Tzcdmax		1.4	2.0	2.6	μs
Maximum frequency lock time Temperature dependence		Tzcdmaxdt	Tj=-40°C to 85°C	-	±5	±10	%

OUTPUT (OUT Pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Output voltage (L)	Vol	V(COMP)=0V Isink(OUT)=200mA	-	1.2	3.3	V
Output voltage (H)	Voh	Isouce(OUT)=200mA	7.8	8.4		V
Output rise time	Tr	V(COMP)=5V C(OUT)=1000pF	-	50	120	ns
Output fall time	Tf	V(COMP)=5V C(OUT)=1000pF	-	25	100	ns

RESTART TIMER

Item	Symbol	Condition	MIN	TYP	MAX	Unit
delay time	Tdly	V(FB)=0V to 2V	10	30	50	μs

UNDERVOLTAGE LOCKOUT (VCC Pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
ON threshold voltage	Von	Vin Increasing DC Input Voltage	11.5	13.0	14.0	V
OFF threshold voltage	Voff	Vin Decreasing DC Input Voltage	8.0	9.0	10.0	V
Hysteresis width	Vhysvcc		3.0	4.0	5.0	V

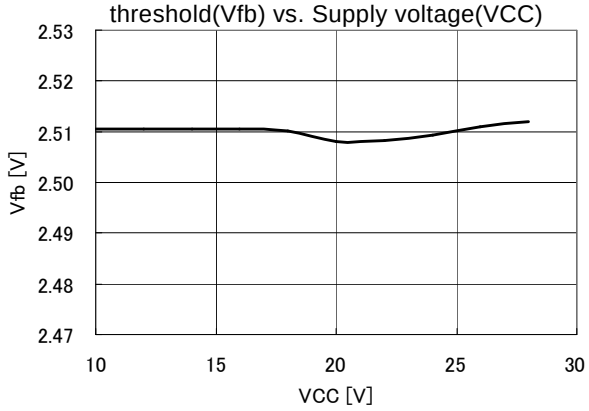
ALL DEVICES (VCC Pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Start-up current	Istart	VCC=Von-0.1V	-	-	80	μA
Operating current	Icc	V(COMP)=OPEN C(OUT)=OPEN	-	1.5	3.0	mA
Dynamic operating current	Iop	V(COMP)=OPEN C(OUT)=1000pF	-	2.0	4.0	mA
Standby current	Istb	V(FB)=0V	-	30	60	μA

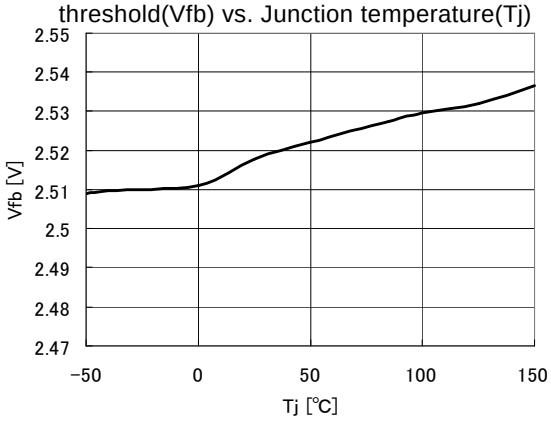
8. Characteristics curves

(Unless otherwise specified, Tj=25°C, VCC=12V, V(FB)=1.0V, V(IS)=0V, V(ZCD)=0V, Rrt=82kΩ)

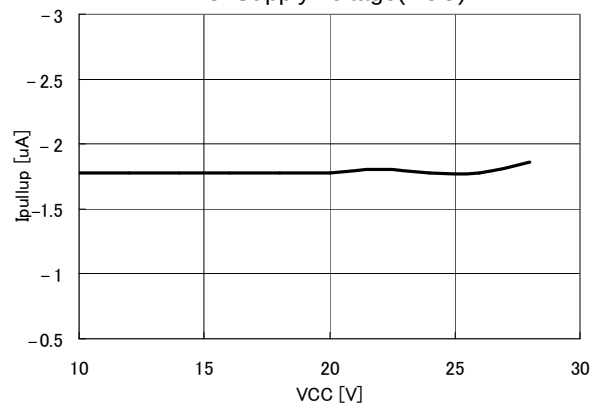
Error amplifier voltage feedback input threshold(Vfb) vs. Supply voltage(VCC)



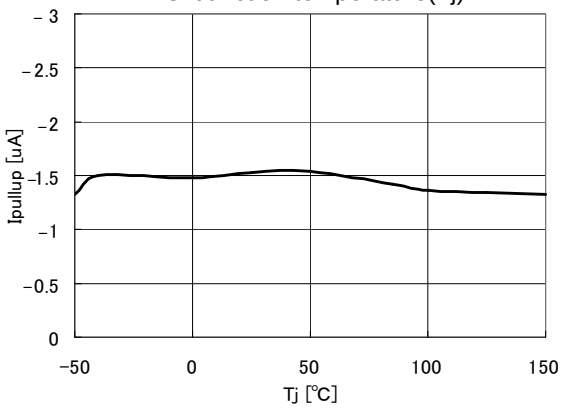
Error amplifier voltage feedback input threshold(Vfb) vs. Junction temperature(Tj)



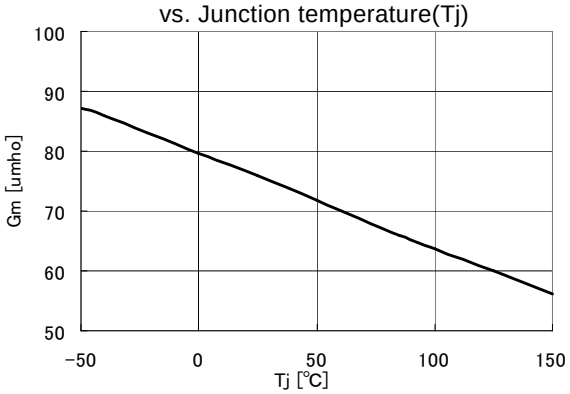
FB pull-up current(Ipullup) vs. Supply voltage(VCC)



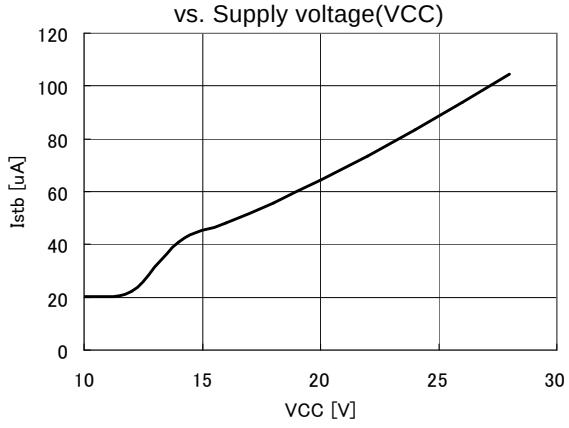
FB pull-up current(Ipullup) vs. Junction temperature(Tj)



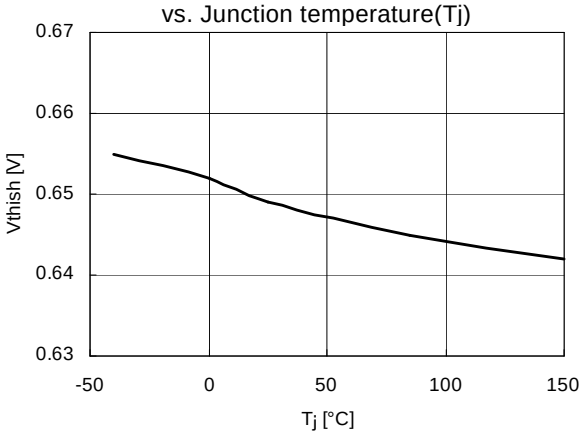
Error amplifier transconductance(Gm) vs. Junction temperature(Tj)



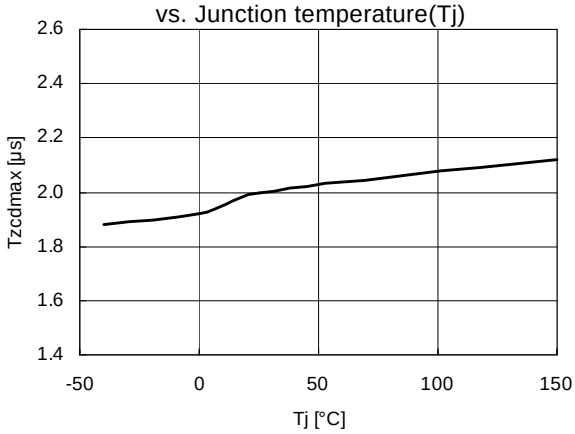
Standby current(Istb) vs. Supply voltage(VCC)



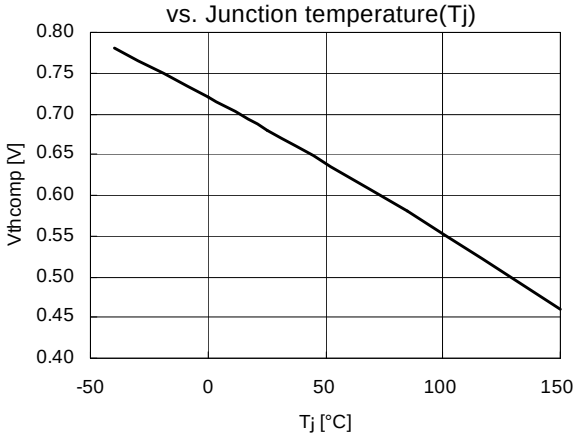
IS threshold voltage (Vthish)
vs. Junction temperature(Tj)



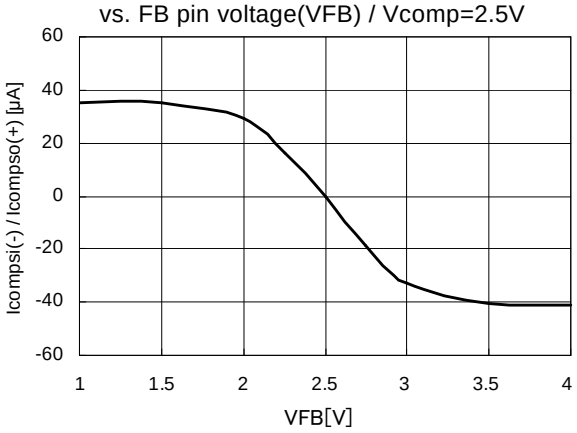
Maximum frequency lock time (Tzcdmax)
vs. Junction temperature(Tj)



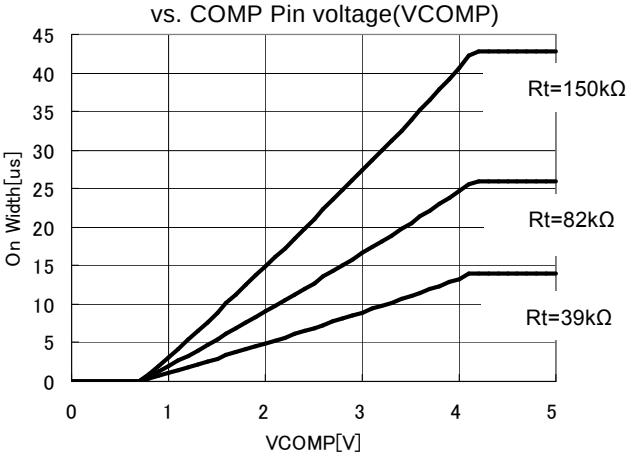
COMP pin OFF threshold voltage(Vthcomp)
vs. Junction temperature(Tj)



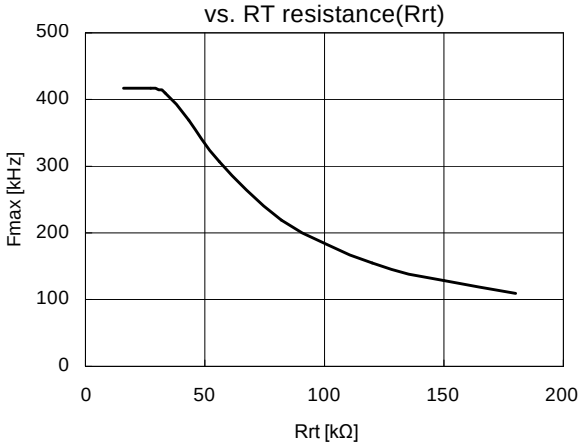
ErrAmp sink/source current(Icompsi/Icompso)
vs. FB pin voltage(VFB) / Vcomp=2.5V



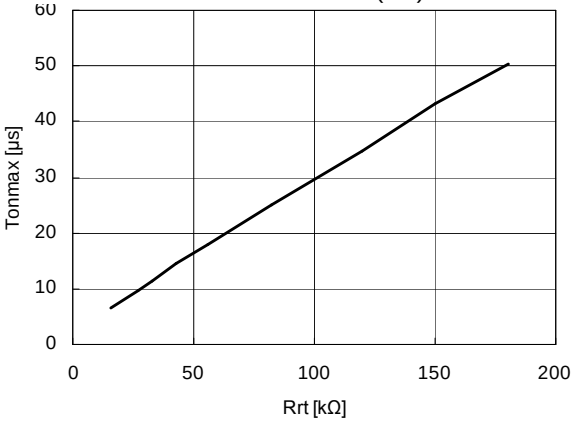
On pulse width (OUT)
vs. COMP Pin voltage(VCOMP)



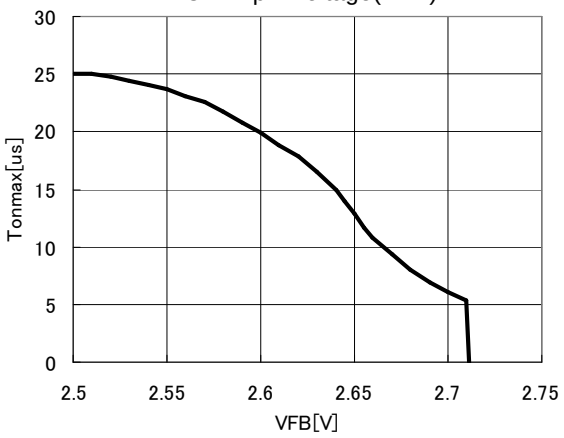
Maximum oscillating frequency(Fmax)
vs. RT resistance(Rrt)



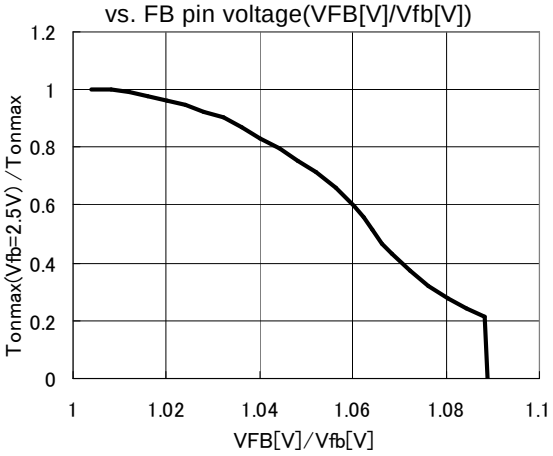
Maximum on-width(Tonmax)
vs. RT resistance(Rrt)



Maximum on-width(Tonmax)
vs. FB pin voltage(VFB)



Maximum on-width
(Tonmax(VFB=2.5V)/Tonmax)
vs. FB pin voltage(VFB[V]/Vfb[V])



9. Outline of circuit operation

This IC is a power-factor correction converter utilizing a boosting chopper or flyback, operating in critical mode. Hereinafter is outline of the operation consisting of switching operation and power-factor correction operation using the circuit diagram shown in Fig. 1.

(1) Switching operation

This IC performs the switching operation in the critical mode applying self-oscillation without using an oscillator. Fig. 2 shows the outline of waveforms of the switching operation in steady state. The operation is as follows.

t1. Q1 turns on, the current through inductor (L1) rises from zero. At the timing of Q1 on, Vramp; output of ramp oscillator states to rise.

t2. Vramp and Vcomp; output of the error amplifier are compared by the PWM comparator, and when Vramp>Vcomp, Q1 turns off and Vramp drops.
When Q1 turns off, the voltage across L1 inverts and the current through L1 decreases while the current is supplied to the output side through D1.
In the meantime, voltage Vsub of the auxiliary winding inverts and positive voltage is generated.

t3. When the current of L1 becomes zero completely, the voltage of L1 resonates with the parasitic capacitor and decreases rapidly. Voltage Vsub of the auxiliary winding installed on L1 decreases rapidly at the same time.

t4. When Vsub decreases to the internal reference voltage of 0.67V, output of the zero current detector (ZCD.comp) becomes low and pulse is output from the ramp oscillator to turn on Q1 and move to the next switching cycle (t1).

By repeating the operations of t1 to t4, the switching in critical mode is continued.

With the power-factor correction circuit in the critical mode, the switching frequency is always changing due to instantaneous values of the AC input voltage. The switching frequency also changes when the input voltage or load changes.

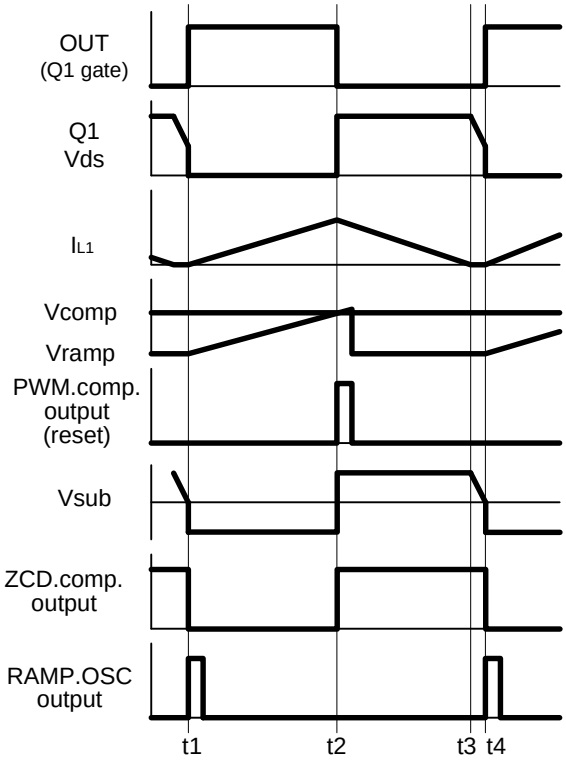


Fig.2 Switching Operation, Waveforms

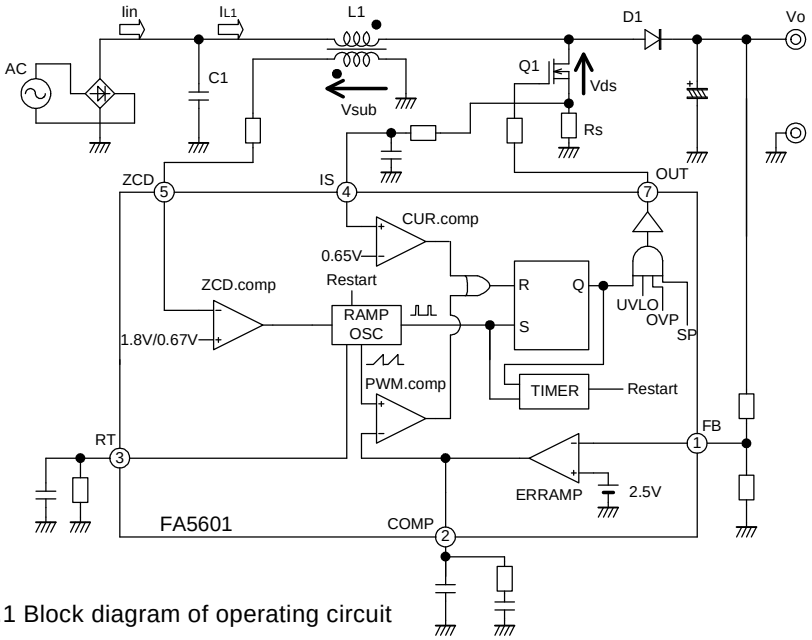


Fig.1 Block diagram of operating circuit

(2) Power-factor correction operation

As explained in the switching operation, the current through inductor repeats in triangular waveforms. The mean value (I_{L1}(mean)) of the triangular wave current becomes 1/2 of the peak value (I_{L1}(peak)). (Fig. 3)
By controlling to make outline linking the peak of the inductor current to sine wave and removing switching ripple current, the smoothed AC input current has sine wave shape.

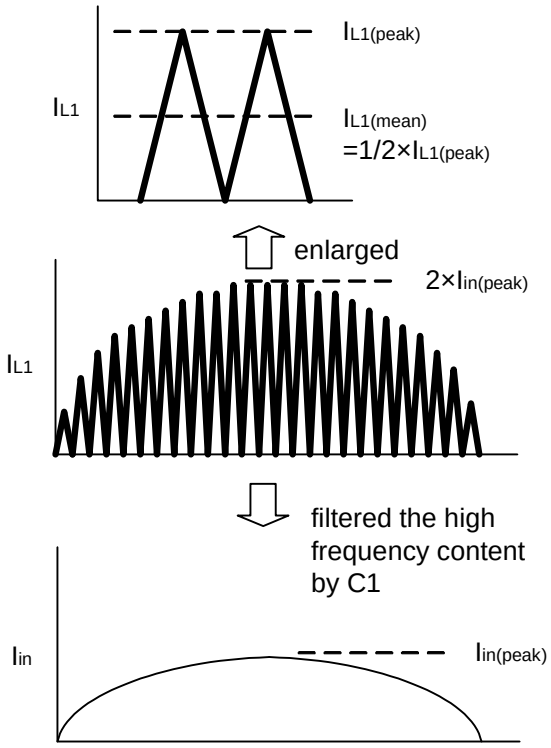


Fig.3 Power-factor correction operation waveforms

FA5601 uses fixed on time control shown in Fig. 4.
This control determines the on time of the output of IC (gate drive signal for MOSFET) with combination of the error amplifier output and saw tooth wave. While the load is constant, the output of the error amplifier is constant, and on time also stays constant.
Since an inclination of inductor current depends on input voltage (an inclination of inductor current is proportional to input voltage) and on time is constant, the outline linking the peak of the inductor current becomes same AC waveform as the input voltage, which enables power-factor correction operation.

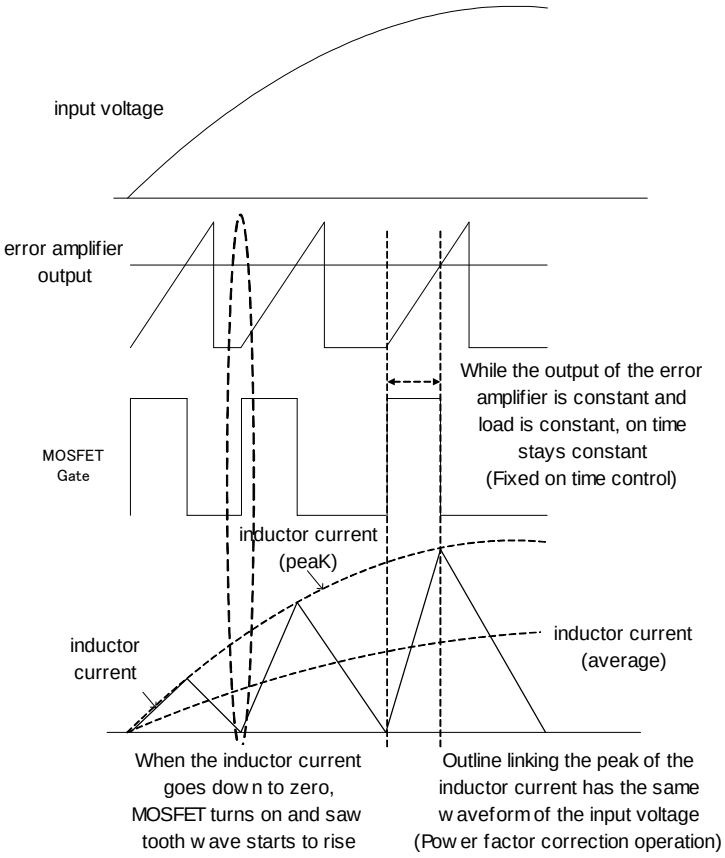


Fig.4 Fixed on time control

10. Description of each circuit block

(1) Error amplifier circuit

The error amplifier is to make the output voltage constant with feedback control. For this IC, a transconductance type is used for the error amplifier.
The non-inverting input terminal is connected to internal reference voltage of 2.5V (typ.).
The inverting input terminal is fed with output voltage of the power-factor correction converter, and normally use divided voltage with resistors. To the inverting input, internal constant current source of 1.8μA is connected for FB open detection function.
The output of the error amplifier (COMP) is connected to the PWM comparator and controls the on time of the OUT output.
The output voltage of PFC contains much of ripple of frequency 2 times AC power line (50 or 60Hz). When this ripple component becomes largely appears in the output of the error amplifier, the power-factor correction converter does not stably operate. In order to obtain the stable operation, connect capacitors and a resistor between terminal No.2 (COMP pin) and GND as shown in Fig.5.

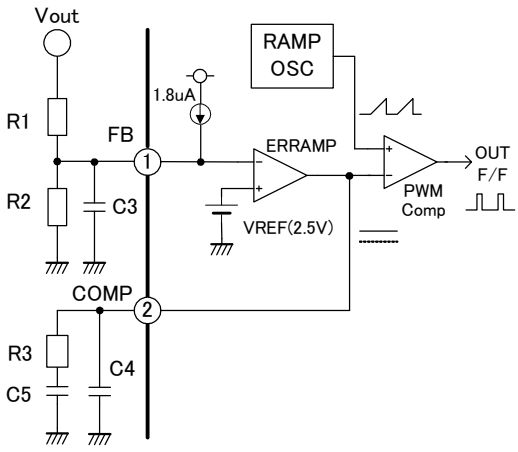


Fig.5 Error amplifier circuit

(2) Overvoltage protection circuit (OVP)

This circuit is to limit the voltage when the output voltage of the power-factor correction converter exceeds the set value.
When this IC starts up or load changes sharply, the output voltage of the converter may exceed the set value. In such a case, this protect circuit works to control the output voltage.
FA5601 has dynamic OVP function to narrow the on time when the FB pin voltage becomes above 2.5V, and static OVP function to stop the output when it becomes higher than 1.09 times the reference voltage.
Normally the voltage of the FB pin is 2.5V, approximately same as the reference voltage of the error amplifier. When the output voltage rises due to starting up or sharp load changes and the voltage of the FB pin becomes higher than 2.5V, the on time narrows by the dynamic OVP function. When the voltage further rises and exceeds the comparator reference voltage, output voltage of the comparator(OVP) inverts to stop the OUT pulse.(Fig. 6)
When the output voltage turns below 1.045 times the reference voltage, the OUT pulse resumes.

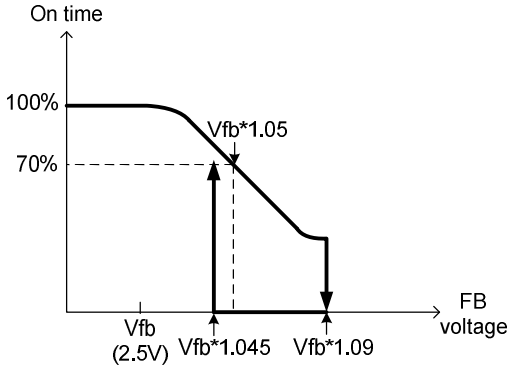


Fig.6 On time at overvoltage

(3) FB short/open-circuit detection circuit (Standby circuit)

In the PFC circuit of booster type, if feedback voltage is not properly provided to the FB pin due to short-circuit of R2 or open-circuit of R1, the error amplifier cannot control the constant voltage and the output voltage abnormally rises. In such a case, the overvoltage protection circuit also cannot operate because the detection of the output voltage is abnormal.
To avoid such situation, this IC is equipped with FB short-circuit detection circuit.
This circuit is composed of the reference voltage of 0.22V (typ.) and comparator (SP). When the input voltage of the FB pin becomes 0.22V or lower due to such trouble as short-circuit of R2 or open-circuit of R1, the output of the comparator (SP) inverts to stop the output of the IC and the IC stops operation resulting in standby state.
Once the voltage of the FB pin decreases to almost zero and the output of the IC stops, and then when the voltage of the FB pin returns to 0.22V or higher, the IC resumes from the standby state and the OUT pulse restarts.
When the connection between the FB pin and the node of voltage dividing resistors is open-circuit, the FB pin voltage is forcefully raised by the internal constant current source of 1.8μA connected to the FB pin. Since the error amplifier output (COMP) voltage decreases as the FB pin voltage rises, the output voltage decreases or OUT output is stopped.

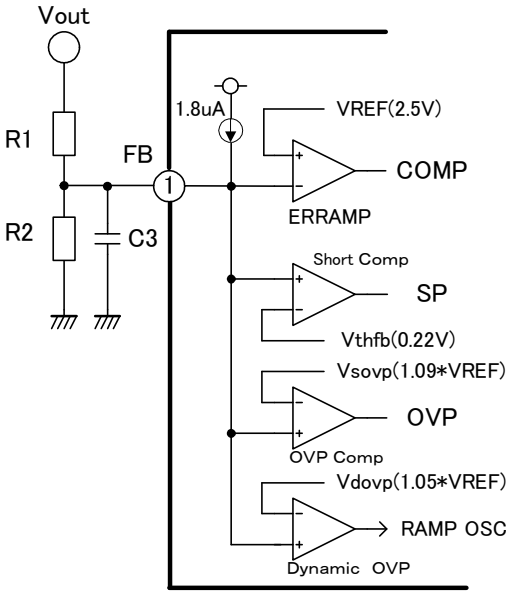


Fig.7 FB pin circuit

(4) Ramp oscillating circuit

The ramp oscillating circuit receives signal from the zero current detection circuit or restart circuit, and outputs the set signal of F/F for OUT output and saw tooth waveform signal for deciding the duty of the PWM comparator.

(4-1) Maximum frequency limiting
The switching frequency of PFC in the critical mode has characteristic to rise at light load.
FA5601 has the maximum frequency limiting function to improve the efficiency at light load and limits the switching frequency to Fmax (Hz). (Fig. 8)
The maximum frequency Fmax depends on the resistance connected between the RT pin and GND.
When the switching frequency is lower than Fmax, the zero level of the inductor current is detected and MOSFET is turned on to adjust turning on take place at the bottom of Vds waveform, as shown in Fig. 9.
In case of light load where the switching frequency is limited to Fmax, the zero level of the inductor current is detected and no turn-on occurs after the zero current detection delay Tzcd, but turn-on occurs at the cycle of 1/Fmax, as shown in Fig. 10.

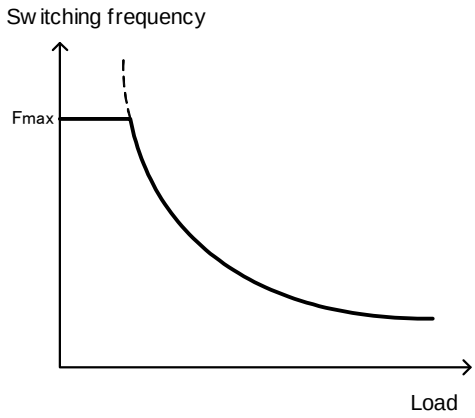


Fig.8 maximum frequency limiting

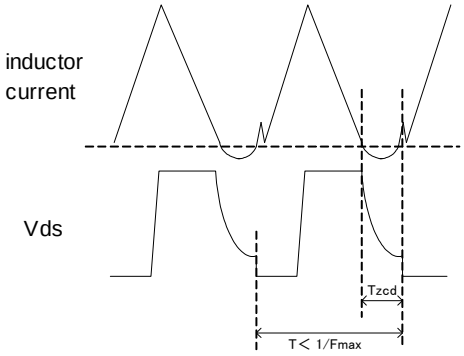


Fig.9 when the switching frequency is lower than the maximum frequency Fmax

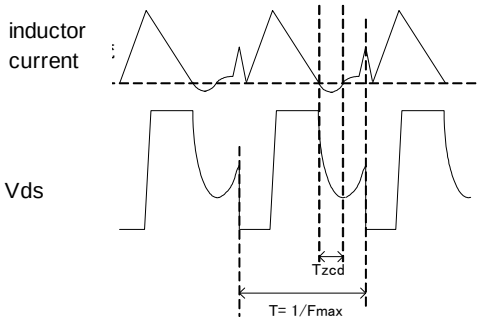


Fig.10 when the switching frequency is limited to the maximum frequency Fmax

(5) Zero current detection circuit

This IC performs the switching operation by self-oscillation in critical mode instead of the oscillator with the fixed frequency. The zero current detection circuit ZCD.comp detects that the inductor current becomes zero to perform the critical mode operation.
The voltage of the auxiliary winding (sub) installed on the inductor is input to the ZCD pin in the polarity as shown in Fig. 11. Positive voltage is generated in the auxiliary winding while MOSFET is off.
Subsequently when the inductor current becomes zero, the auxiliary winding voltage decreases rapidly. This voltage drop is detected by ZCD.comp and the ramp oscillating circuit (RAMP OSC) sends the setting signal to the R-S flip flop to turn on MOSFET and move to the next cycle.

The auxiliary winding voltage changes significantly depending on circuit and input voltage. To cope with this problem, a clamp circuit with the upper limit of 7.6V(typ.) and the lower limit of -1.0V(typ.) is provided.

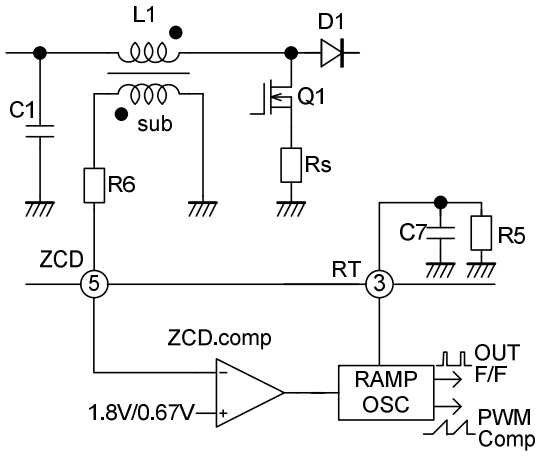


Fig.11 Zero current detection circuit

(6) Overcurrent detection protective circuit

The overcurrent detection protective circuit detects the inductor current and protects MOSFET by turning off the OUT output when it becomes higher than a set current level. For overcurrent detection, the voltage generated in the current sense resistance Rs, which is connected between the MOSFET source and the GND line, is input into the IS pin and compared by the overcurrent detection comparator.

When the IS pin voltage becomes 0.65V (typ) or more, it is output as overcurrent state.

When the overcurrent is detected, the F/F for OUT output is reset to make MOSFET turn off.

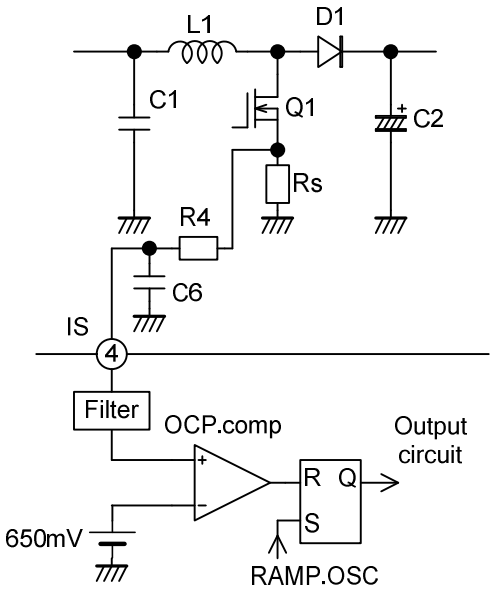


Fig.12 Overcurrent detection protective circuit

(7) Restart timer circuit

This IC utilizes self oscillation instead of the oscillator with fixed frequency, and in the steady operation, it turns on MOSFET with a signal from the zero current detector.

But in start up or light load condition, a trigger signal is required for starting up or stable operation.

This IC is provided with a restart timer, and when the output of IC continues turn off for 30μs(typ) or more, the trigger signal is automatically generated.

This signal can realize stable operation even when starting up or the load is light.

(8) Under Voltage Lock Out circuit (UVLO)

UVLO is equipped to prevent circuit malfunction when supply voltage drops.

When the supply voltage rises from zero, the operation starts at 13V (typ.) for FA5601.

When the supply voltage decreases after starting operation, operation stops at 9V (typ.) and the capacitor connected to the COMP pin is discharged by the discharging circuit within the COMP pin.

When UVLO is on and IC stops operation the OUT pin becomes Low and cuts off the output. The current consumption of the IC decreases to 80μA or less.

(9) Output circuit

The output circuit consists of a push-pull circuit, directly drives MOSFET. The peak current of the OUT output is 1.0A maximum for sink and 0.5A maximum for source.

11. Description of use for each pin

(1) Terminal No.1 (FB pin)

Functions
(i) Input of feedback signal of output voltage setting
(ii) Detect short-circuit of FB pin
(iii) Detect output overvoltage

Application
(i) Feedback signal input
- Wiring
Connect the node between voltage dividing resistors for setting output voltage.
- Operation
The output voltage Vout of PFC is controlled so that FB voltage matches the internal reference voltage (2.5V).
To detect FB pin open-circuit, pull-up current (Ipullup) is supplied to the FB pin. This current flows to GND via R2. For this reason, resistance R1, R2 should be set in consideration of this current when the output voltage (Vout) is set.

$$Vout = (VREF / R2 - Ipullup) \times R1 + VREF$$

VREF : Reference voltage =2.5V(typ)
Ipullup : FB pin pull-up current =1.8μA(typ)

To prevent malfunction due to noise, capacitor C3 of 100pF to 3300pF should be connected between the FB pin and GND.

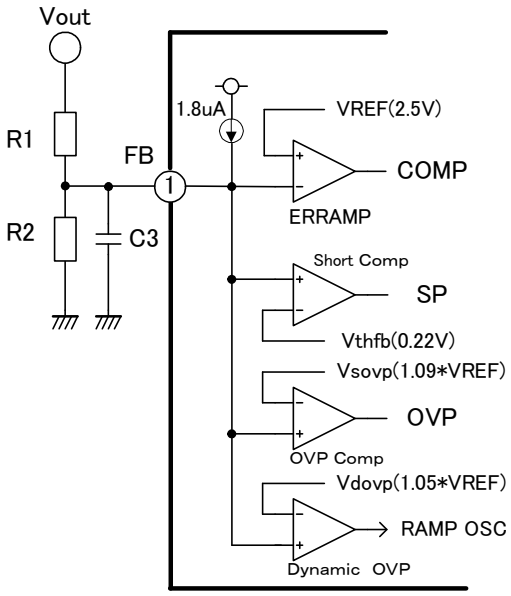


Fig.13 FB pin circuit

(ii) FB pin short-circuit detection
- Wiring
Same as for the (i) Feedback signal input
- Operation
When the input voltage of the FB pin becomes 0.22V or lower due to short-circuit of R2, the output of the comparator (SP) inverts to stop the output of the IC.

(iii) Output overvoltage detection
- Wiring
Same as for the (i) Feedback signal input
- Operation
Normally the voltage of the FB pin is 2.5V almost same as the reference voltage of the error amplifier. When the output voltage rises for some reason and the voltage of the FB pin reaches the comparator reference voltage (1.09*VREF), the output of the comparator (OVP) inverts to stop the OUT pulse. If the output voltage returns to the normal value, the OUT pulse resumes.

(2) Terminal No.2 (COMP pin)

Function
(i) Phase compensation of internal ERRAMP output
(ii) Soft start
(iii) ON/OFF operation from exterior

Application
(i) Phase compensation of internal ERRAMP output
- Wiring
Connect C, R between COMP pin and GND as shown in Fig. 14.
- Operation
Connecting C, R to the COMP pin suppress ripple component at 2 times the frequency of the AC line that appears in the FB output.

(Reference)
Example of application circuit : C4=0.1μF
C5=0.15μF
R3=68kΩ

The above is a reference example, and it should be decided by sufficiently verifying with actual application circuit.

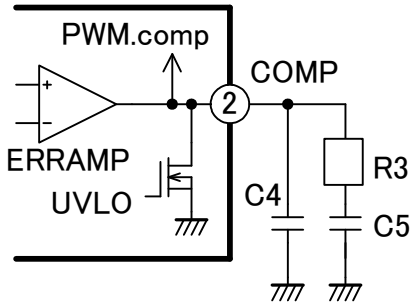


Fig.14 COMP pin circuit

(ii) Soft start
- Wiring
Connect C between COMP pin and GND as shown in Fig. 14.
- Operation
By connecting C to the COMP pin, the speed of the COMP pin voltage increase is slowed to restrict sudden widening of the ON time.
When the capacity of capacitor connected to the COMP pin is larger, the soft start time becomes longer. However, the phase compensation and transient response characteristics are changed at the same time, and so make adjustment while checking actual operation.

(iii) On/off operation from exterior
- Wiring
Connect the switch such as transistors between COMP pin and GND.
- Operation
By lowering the voltage of the COMP pin to Vthcomp or less, the output pulse from the IC is stopped. Example of connection is shown in Fig. 15.

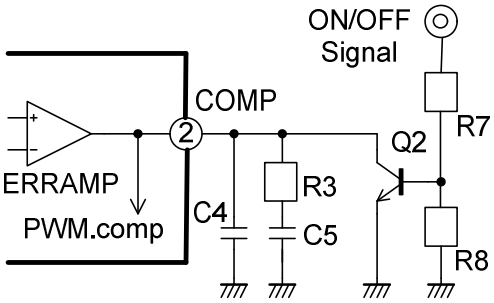


Fig.15 ON/OFF circuit

(3) Terminal No.3 (RT pin)

Functions
(i) Set maximum on time
(ii) Set maximum oscillation frequency

Application
(i) Set maximum on time
In the PFC circuit of booster type, on time Ton in each switching cycle with input and output conditions is theoretically expressed by the following formula.

$$Ton = \frac{2 \times Lp \times Po}{Vac^2 \times \eta}$$

Input Voltage (Vrms) : Vac
Inductor (H) : Lp
Maximum Output Power (W) : Po
Efficiency : η

The maximum on time Tonmax must be set equal to or more than the on time at minimum input voltage Vac(min) at which the on time is maximum. Set the maximum on time Tonmax by the following formula.

$$Ton\,max > \frac{2 \times Lp \times Po}{Vac(min)^2 \times \eta}$$

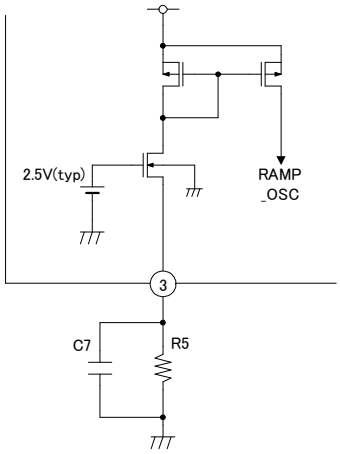


Fig.16 RT pin circuit

(ii) Set maximum oscillation frequency
To improve the efficiency at light load, FA5601 limits switching frequency at light load to Fmax(Hz). The maximum frequency Fmax depends on the resistance connected between RT pin and GND.

- Wiring
Connect R5 between RT pin and GND as shown in Fig. 16.
For the resistance dependency of the maximum on time and maximum oscillation frequency, see Chapter 8. Characteristic Curve.
The current sourced from the RT pin changes depending on the resistance connected. When R5 is relatively large, for example, 82kΩ, the current is about 10uA. When the current is relatively small, it is recommended to connect a capacitor of about 0.01μF in parallel to the resistor to stabilize the RT voltage, as shown in Fig. 16.
In addition, the oscillator slope is changed by the resistance value of RT. Therefore the on time characteristics of MOSFET to the COMP pin voltage is changed and so the circuit gain is changed.
Resistance value of RT is small → Circuit gain is small
Resistance value of RT is large → Circuit gain is large
Therefore operation stability and input and load regulations are changed. Make adjustment while checking actual operation.

(4) Terminal No.4 (IS pin)

Function

(i) Detect overcurrent through the MOSFET and turn off OUT output

Application

(i) Detect current value through the MOSFET

The maximum threshold voltage Vthis of the IS pin is 0.63V(min) to 0.67V(max).

The current detection resistance Rs is set so that necessary current can be supplied for this Vthis.

With maximum output Po(W) and minimum input voltage Vac(min), the maximum value of peak current (ILP(max)) through the inductor and MOSFET can be approximately expressed by the following formula.

$$I_{LP(\max)} = \frac{2 \times \sqrt{2} \times Po}{\eta \times Vac_{(\min)}}$$

Therefore, the value of Rs(Ω) is determined as follows.

$$Rs < \frac{Vthis}{I_{LP(\max)}} = \frac{0.63}{I_{LP(\max)}}$$

- Wiring

Connect the current detection resistor Rs between the source terminal of MOSFET and GND. The voltage across Rs is fed to the IC as the current/voltage conversion signal.

- Operation

(i) When the IS pin voltage becomes larger than 0.65V(typ), the comparator output signal inverts and turns off the OUT output.

- Additional explanation

When MOSFET turns on, the gate driving current of MOSFET and surge current due to discharging the parasitic capacitors run to the current detection resistance Rs. Large surge current may cause malfunction following disturbed input current waveform. Depending on the amperage of the surge current or timing, whisker-like pulse may be mixed in the turn-on portion of the OUT pulse of the IC. Normally, therefore, a CR filter is connected as shown in Fig.17. The cutoff frequency of this CR filter must be set sufficiently higher than the switching frequency so that it will not affect the normal operation.

It is recommended to set this cutoff frequency to about 1MHz to 2MHz.

$$\frac{1}{2 \times \pi \times C6 \times R4} \fallingdotseq 1 \sim 2[\mathrm{MHz}]$$

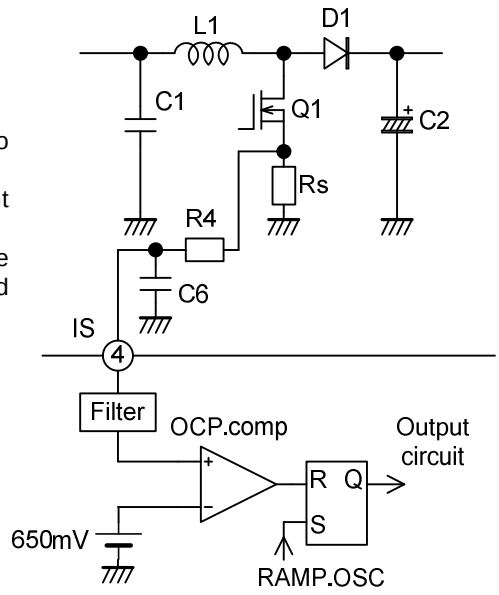


Fig.17 IS pin circuit

(5) Terminal No.5 (ZCD pin)

Function

(i) Detect zero current

Application

(i) Detect zero current

The auxiliary winding voltage of L1 is input into the ZCD pin to detect the timing for turning on MOSFET. To use the current, which is flowed into the ZCD pin, within the IC rating, usually the resistance R6 for current limitation is set between the ZCD pin and the auxiliary winding shown in Fig.18.

- Wiring

Connect the R6 between the ZCD pin and the auxiliary winding shown in Fig.18.

It is necessary to limit the current, which is flowed through the clamp circuit of ZCD pin, to 3mA or less in order to operate the IC normally as advised in the recommended conditions. The following formula must be satisfied.

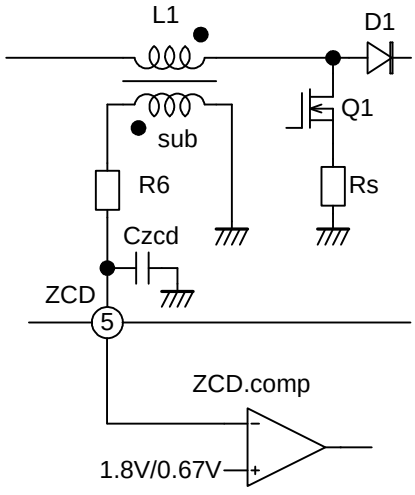
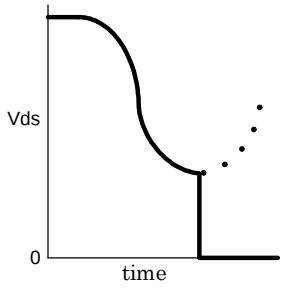


Fig.18 ZCD pin circuit

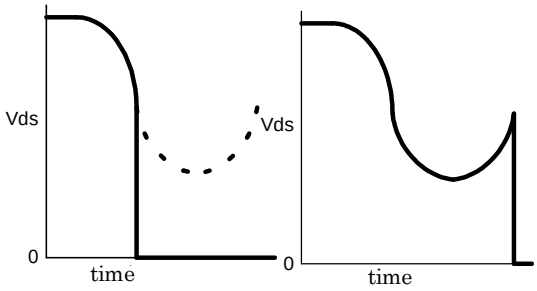
$$ON: R6 > \frac{-0.4 + \sqrt{2} \times Vac(\max) \times \frac{Ns}{Np}}{3 \times 10^{-3}}$$

$$OFF: R6 > \frac{Vo \times \frac{Ns}{Np} - 7.0}{3 \times 10^{-3}}$$

MOSFET (Q1) turns on after the current of inductor L1 becomes zero. Subsequently Vds between the drain and the source in MOSFET starts vibration just before the turn-on due to the resonance between L1 and the parasitic capacitor element.
Adjust R6 and C_{ZCD} so that MOSFET turns on in this resonance trough.
Generally R6 is 10kΩ to 100kΩ, and if adjustment cannot be made only by resistor, C_{ZCD} is added to make adjustment (usually the value becomes about 10pF to 100pF).
Then, the switching loss caused when MOSFET is turned on is kept minimal and the surge current generated at the time of turn-on is kept minimal.



(When R6 and Czcd values are correct)



(When R6 and Czcd value are not correct)

Fig.19 MOSFET waveform just before turn-on

(6) Terminal No.6 (GND pin)

Function

This voltage of GND pin is the reference for each portion of whole circuits.

(7) Terminal No.7 (OUTpin)

Function

This drives MOSFET.

Application

- Wiring

Connect it to the gate terminal of MOSFET through resistance.(Fig.20)

- Operation

During the period when turn on MOSFET, the output state is high, and the output voltage is almost VCC.
During the period when turn off MOSFET, the output state is low, and the output voltage is almost 0V.

- Additional explanation

The gate resistor is connected to limit the current of the OUT pin and prevent oscillation of the gate terminal voltage. The rating of the output current is 0.5A for source and 1A for sink.
Using the connections shown in Fig.21 and Fig.22, it is possible to independently set the gate driving current of turning on and off MOSFET.

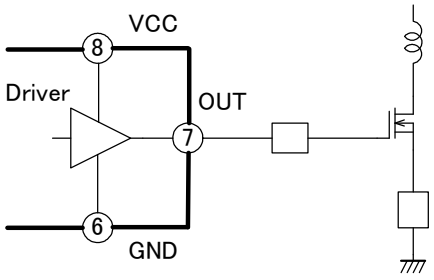


Fig.20 OUT pin circuit (1)

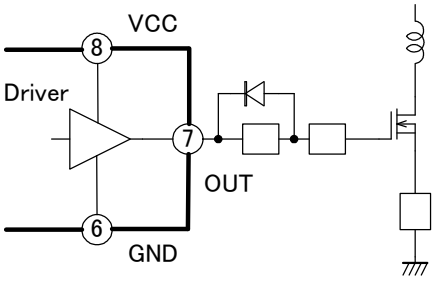


Fig.21 OUT pin circuit (2)

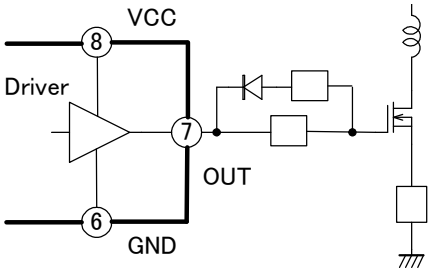


Fig.22 OUT pin circuit (3)

(8) Terminal No. 8 (VCC pin)

Function

(i) Supply the power of IC.

Application

(i) Supply the power of IC.

- Wiring

Connect the start up resistor R7 between VCC pin and Voltage line after rectifying from AC line, which supplies power before IC starts switching operation.

In general application, the power is provided from the auxiliary winding of the transformer through D2 during operation.

In some application, DC power supply can be connected.

- Operation

In the application without DC power supply to feed VCC pin, the current through start up resistor R7 charges the smoothing capacitor C8, and when VCC voltage rises to the on threshold voltage of UVLO, the IC starts operating. Before starting operation, it is necessary to supply current higher than 80μA(max), the startup current of the IC. During steady operation, the VCC is supplied from the auxiliary winding of the inductor. (Fig.23)

When the supply voltage rises from zero, the operation starts at 13V (typ.) for FA5601.

If the supply voltage decreases after the operation starts, the operation stops and capacitor connected to the COMP pin discharged at 9V(typ.) by UVLO. After IC stops operation due to UVLO, the OUT pin is Low state to cut off the output.

- Additional explanation

UVLO is preventive function to keep the circuit from malfunction when the supply voltage decreases.

With the start up resistor R7, it is necessary to supply current of 80μA or higher, the startup current, until start operating, and the following formula must be satisfied.

$$R7 < \frac{\sqrt{2} \times Vac(min) - Von(max)}{80 \times 10^{-6}}$$

Von(max) : ON threshold voltage of UVLO
FA5601 14V(max)

The value of R7 expressed with the formula is, however, at least necessary and minimum condition to start the IC, and actually it should be decided considering the starting up time required for each application circuit.

During the steady operation, Vcc is supplied from the auxiliary winding of the transformer. But there is some time delay until the auxiliary winding voltage sufficiently rises after the IC starts switching operation. To prevent Vcc from decreasing to the off threshold voltage of UVLO, it is necessary to decide the capacitance of the C8 connected to Vcc. Since this time delay differs depending on the circuit, it should be decided after checking with actual circuit.

It is also recommended to place the ceramic capacitor C9 (about 0.1μF) to remove switching noise.

- Startup time

When Vcc increases up to the ON threshold voltage of 13V and the IC starts operation, the COMP voltage increases. When the COMP voltage reaches 0.7V, OUT signal is output and operation is started.

The starting time Tstart can be estimated roughly by the following formula:

$$Tstart = \frac{C8 \cdot Von}{\frac{Vac(min) \cdot \sqrt{2}}{R7} - Istart}$$

Istart : startup current

This starting up time must be examined by measuring in actual circuit operation.

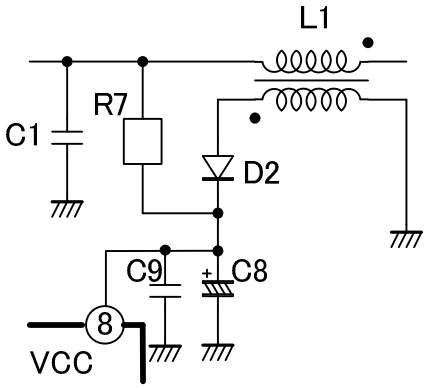


Fig.23 VCC pin circuit (1)

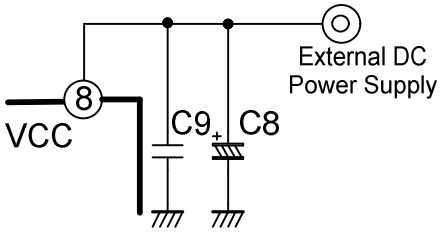


Fig.24 VCC pin circuit (2)

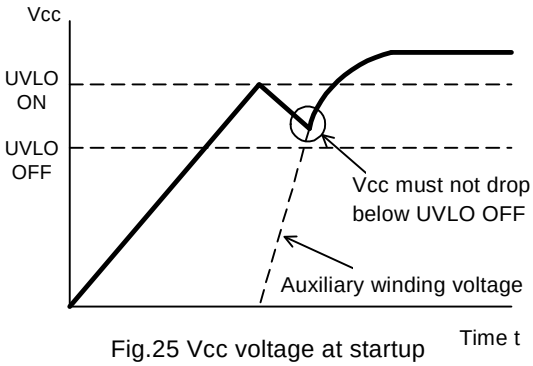


Fig.25 Vcc voltage at startup

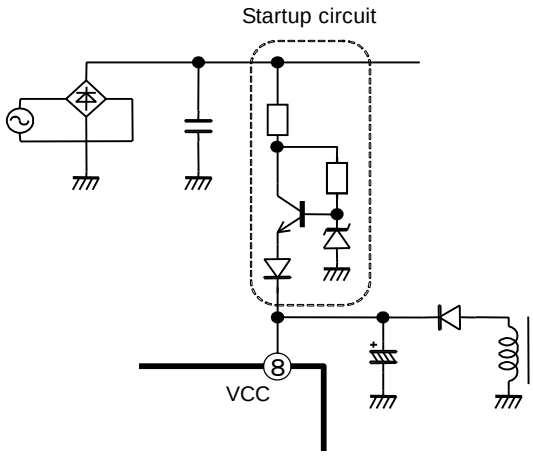


Fig.26 Startup circuit

Usually capacitor C8 connected to Vcc cannot be so small in capacity and so starting takes time when the starting resistance R7 is large. If the starting resistance R7 is small, the starting time is shortened but loss of starting resistance increases and the efficiency is decreased. As one of measures, it is advised to construct the starting circuit as shown in Fig.26 to shorten the starting time without reducing the efficiency.

(9) Minus voltage of each terminal

In some cases, the voltage oscillation of Vds just before MOSFET turns on is applied to the OUT pin through parasitic capacitors, etc. and minus voltage may be added to the OUT pin. If this minus voltage is large, the parasitic element inside the IC is activated, and the IC may malfunction.
If this minus voltage is expected to exceed -0.3V, Schottky barrier diode should be connected between the OUT pin and GND. With the forward voltage of the Schottky barrier diode, the minus voltage can be clamped.
For other terminals as well, care should be taken so that minus voltage will not be applied in the same way.

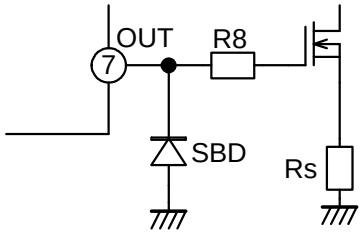


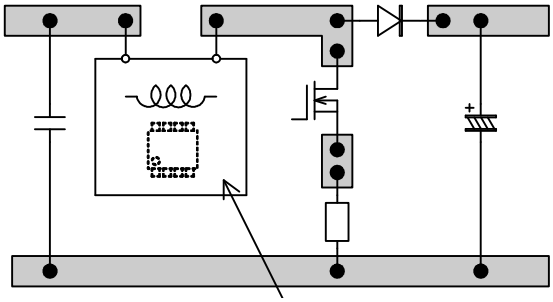
Fig.27 Protection circuit of OUT pin against the negative voltage

12. Advice for design

(1) Advice in pattern designing

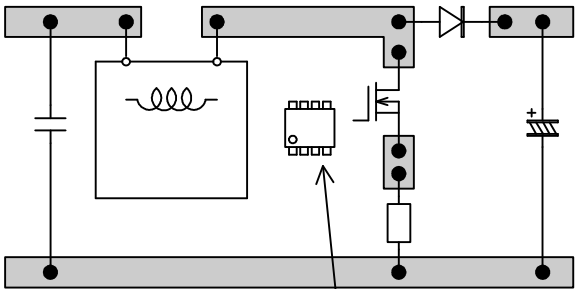
Main power parts such as MOSFET, inductor, and diode in the main switching circuit are operating with large voltage and current. For this reason, if the IC or wires of input signals are located close to these main power parts, malfunction may occur affected by noise generated there.

Special care should be taken to the following cases. (Bad examples)
- IC is placed under the main circuit parts such as inductor or just on the back side of the main circuit parts in case of a double-sided board. (Fig.28)
- IC is placed just beside the inductor, MOSFET or diode. (Fig.29)
- Signal wires are placed under the inductor or near MOSFET or diode. (Fig.30)



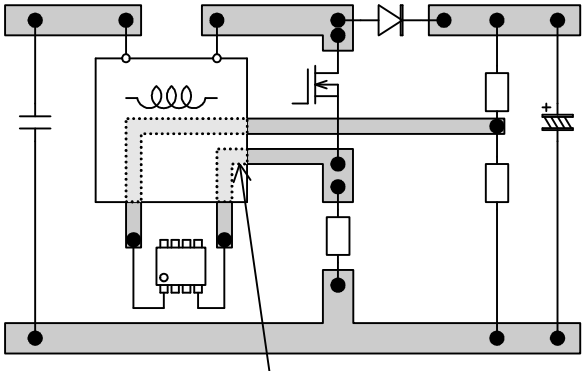
IC is placed under the inductor

Fig.28 Bad example (1)



IC is placed just beside the inductor, MOSFET

Fig.29 Bad example (2)



Signal wires are placed under the inductor or near MOSFET

Fig.30 Bad example (3)

(2) Example of GND wiring around IC

- Note

This wiring example is to make users understand the idea of GND wiring. The occurrence conditions of noise and malfunction are different depending on each application circuit, and it is not to guarantee that all application circuit will normally operate even if you use this wiring example (Fig. 31).

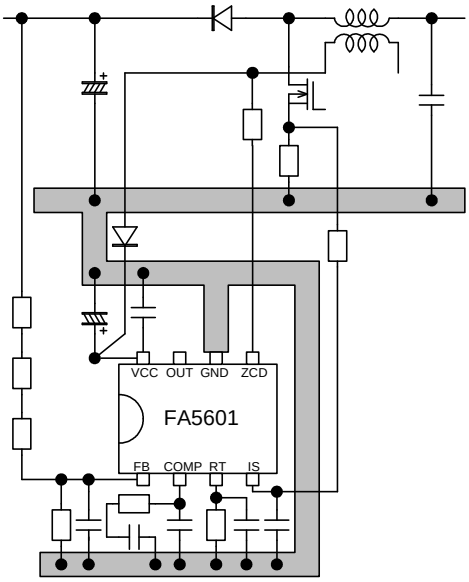


Fig.31 Good example of GND wiring around IC

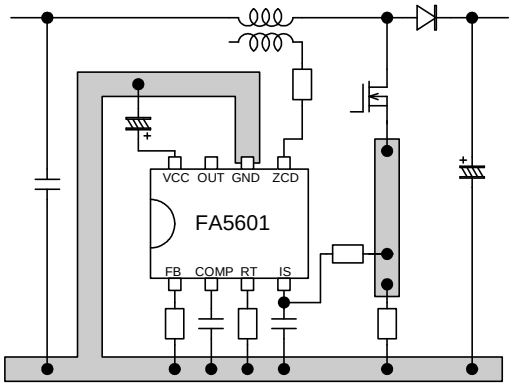
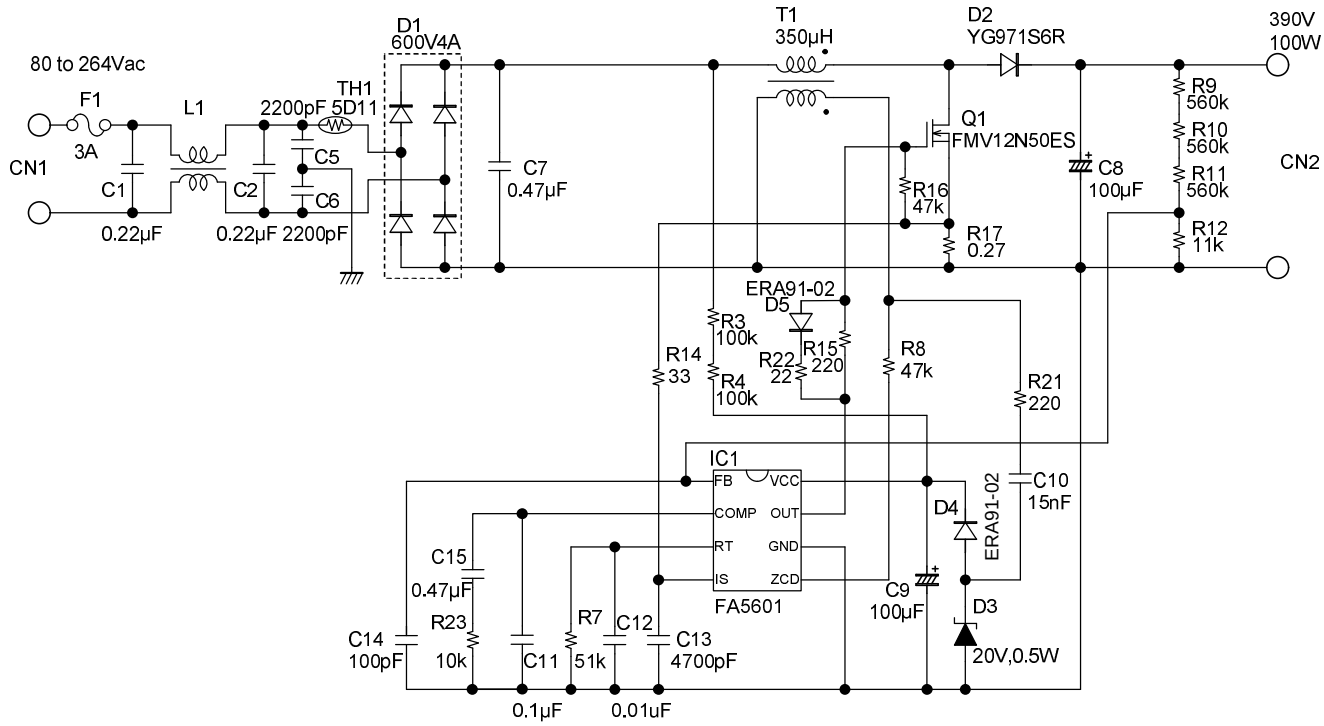


Fig.32 Bad example of GND wiring around IC

13. Example of application circuit

Fig.33 Example application circuit for non-isolated booster PFC



14. Example of application circuit for PFC flyback

Fig.34 Example application circuit for isolated PFC (constant voltage/constant current control)

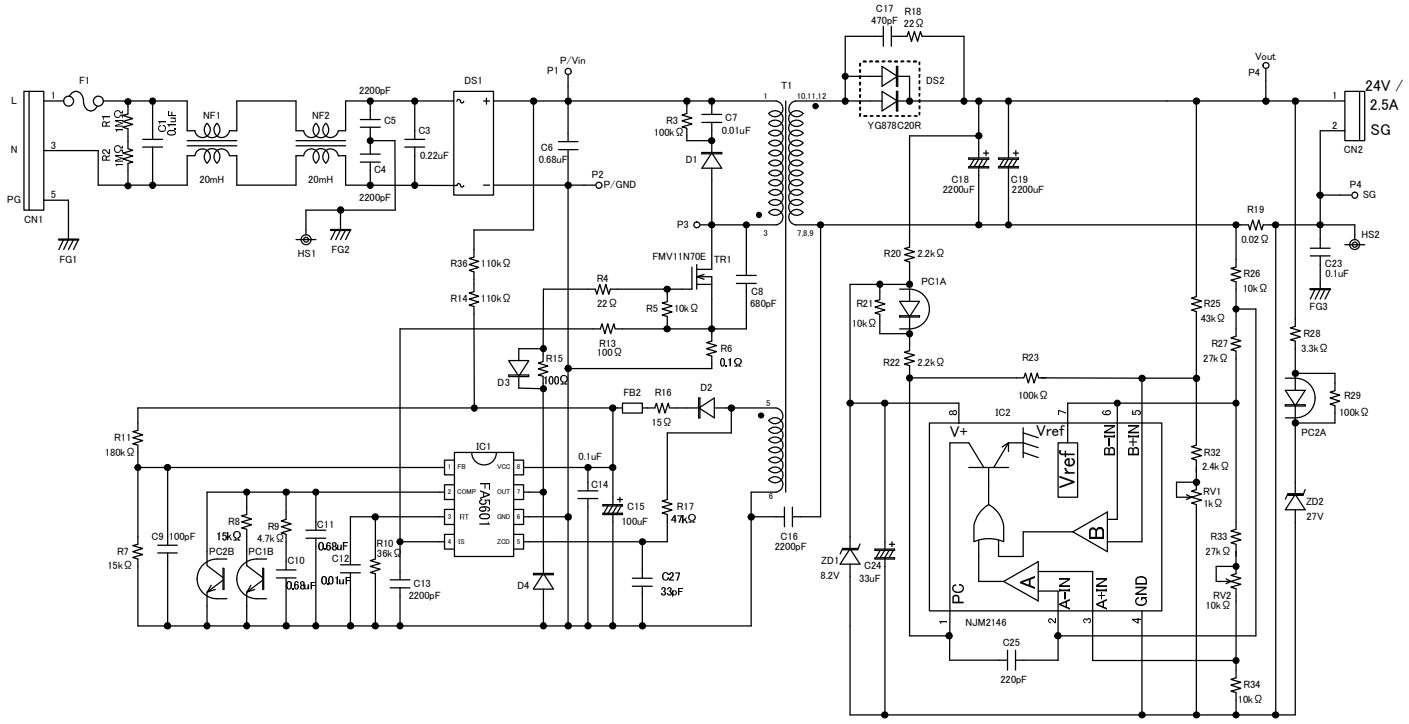
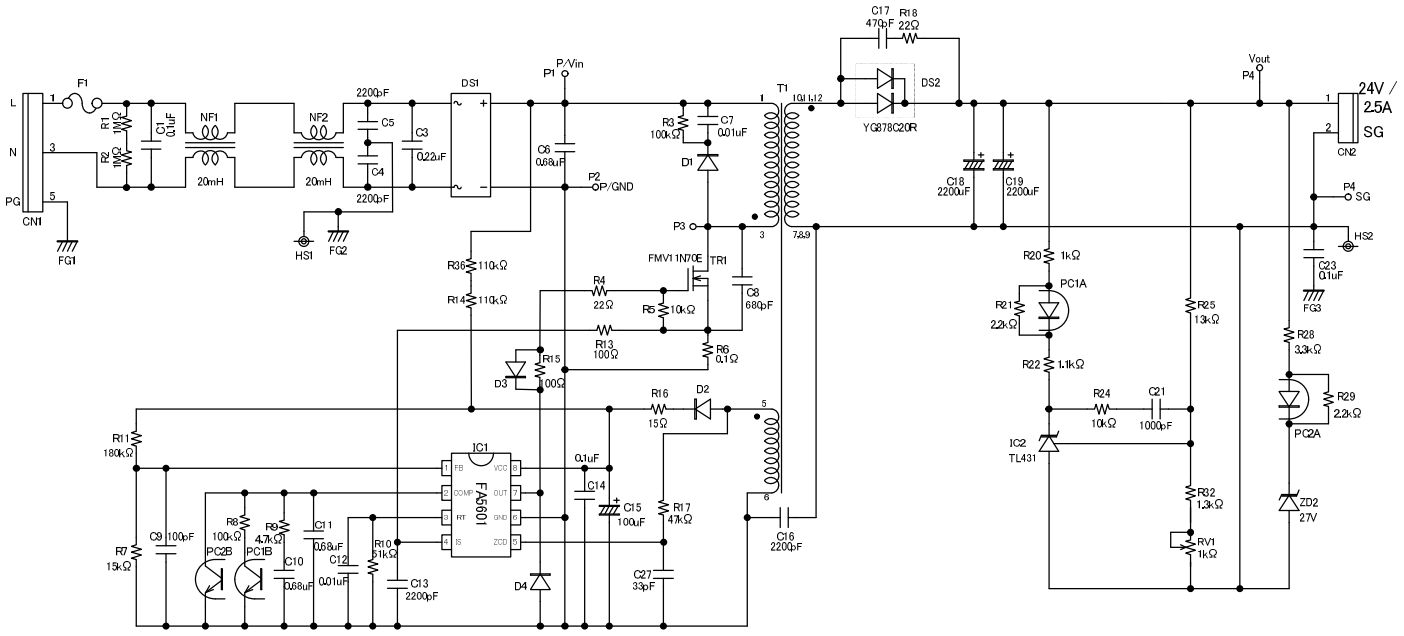


Fig.35 Example application circuit for isolated PFC (constant voltage control)



15. Advice for design of PFC flyback circuit

(1) Design of feedback circuit

Fig.36 shows an example circuit using a photo-coupler for secondary-side feedback in an isolated circuit configuration such as an application circuit.

[1] Voltage of 1.3V to 2.0V is input into the FB pin so that the error amplifier output (COMP) becomes high-level output during operation.

[2] In this example circuit, the COMP pin is used for both phase compensation and output feedback and so C and R are connected to the photo-coupler as shown in Fig.36. If resistance R4 which restricts the photo-coupler is too large, control cannot be performed during light load. Usually 15kΩ or less is advised.

When load is kept constant by phase the compensation capacitors C4, C5 and the resistance R3, adjust the COMP pin voltage to be almost flat (DC).

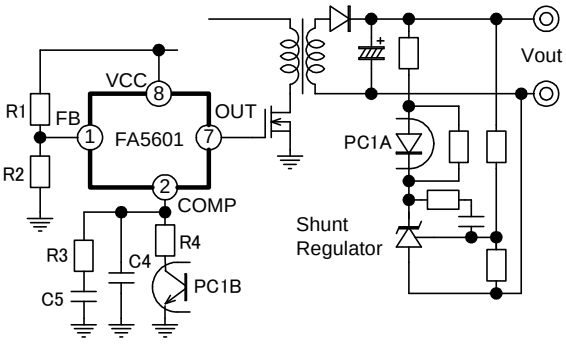


Fig.36 Example of feedback circuit

(2) Adjustment of turn-on timing

The ZCD pin is connected to the auxiliary winding installed on the transformer through the CR circuit of R_{ZCD} and C_{ZCD} (fig. 37).

Be careful of the polarity of the transformer auxiliary winding.

If voltage of the ZCD pin decreases to 670mV or less, MOSFET is turned on. The auxiliary winding voltage changes significantly in both positive and negative directions. To protect IC against this voltage, a clamp circuit is provided.

Just before turn-on, the MOSFET voltage oscillates due to the resonance between the transformer inductance and the resonant capacitor Cd. Adjust C_{ZCD} so that MOSFET turns on in the trough of this resonance (Fig. 38).

Generally R_{ZCD} is 10kΩ to 100kΩ and C_{ZCD} is about 10pF to 100pF.

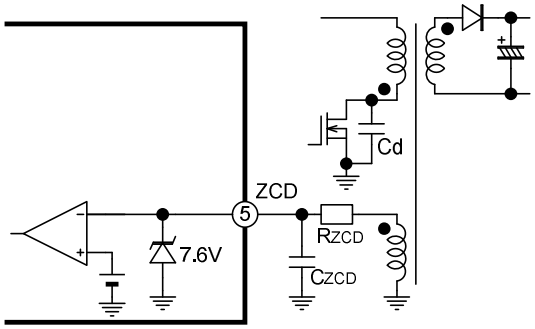


Fig.37 Example of ZCD pin circuit

(3) Starting operation

Example connection of the VCC pin is shown in Fig.39.

When Vcc increases to the ON threshold voltage of 13V due to the current by the starting resistance R7, the UVLO circuit is released and the IC starts operation.

When operation is started, the COMP pin voltage increases. When it reaches 0.7V, OUT signal is output and operation is started (Fig.40).

Vcc is supplied form the transformer auxiliary winding during steady operation. After the IC starts, however, there is slight time lag before the auxiliary winding voltage starts sufficiently. It is necessary to determine the proper capacity of the capacitor C8 connected to Vcc so that Vcc does not decrease to the UVLO off threshold voltage during this time lag.

Since this time lag changes depending on circuits, determine the capacity while checking actual operation.

It is advised to install a ceramic capacitor C9 (about 0.1μF) near the IC to remove switching noise.

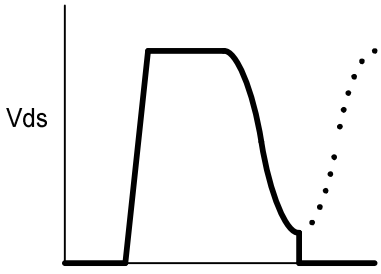


Fig.38 MOSFET Vds waveform

The IC starting time Tstart can be estimated roughly by the following formula.

$$Tstart = \frac{C8 \cdot Von}{\frac{Vac(min) \cdot \sqrt{2}}{R7} - Istart}$$

Istart : Startup current

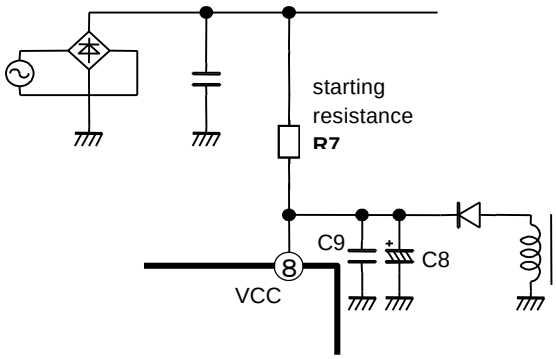


Fig.39 VCC pin circuit

Usually capacitor C8 connected to Vcc cannot be so small in capacity and so starting takes time when the starting resistance R7 is large.

If the starting resistance R7 is small, the starting time is shortened but loss of starting resistance increases and the efficiency is decreased.

As one of measures, it is advised to construct the starting circuit as shown in Fig.41 to shorten the starting time without reducing the efficiency.

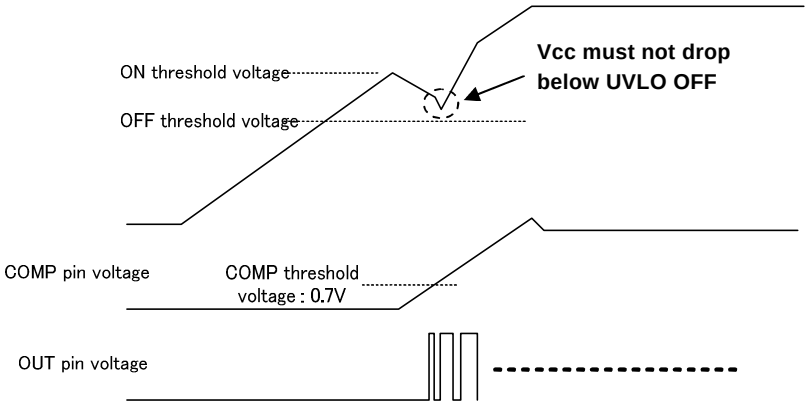


Fig.40 Vcc voltage at startup

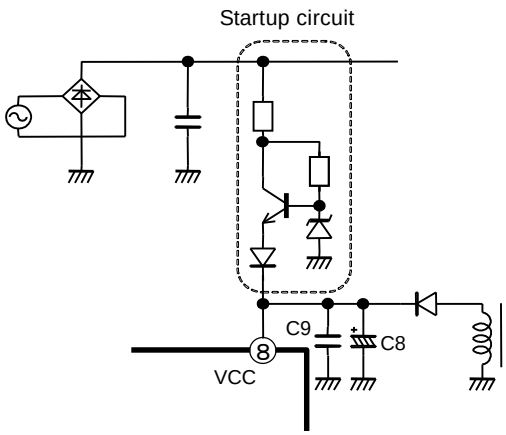


Fig.41 Startup circuit

16. Advice for use of PFC flyback circuit

(1) Precautions for designing patterns

Due to principal current, lightning surge test, AC input surge test and static electricity test, current may flow into the negative-side pattern and its surge voltage (noise) may cause malfunction of the control IC (unstable voltage, unstable waveform and latch stop). Therefore carefully study the following for design to avoid malfunction.

There are the following current pathways in the power source.

[1] Principal current, which flows from the electrolytic capacitor to the transformer primary winding, MOSFET and current detection resistor after rectification of AC power supply

[2] Rectified current, which flows from the transformer auxiliary winding to the electrolytic capacitor, and drive current, which flows from the electrolytic capacitor to the control IC and the MOSFET gate

[3] Control current of the control IC such as output feedback

[4] Filter current and surge current, which flow between the primary and secondary sides

- Separate the negative-side patterns [1] to [4] so that they are not interfered.
- The pathway where the primary current flows must be the shortest loop to keep the MOSFET surge voltage minimal.
- The electrolytic capacitor and the film capacitor between the VCC pin and GND must be installed immediately near the respective terminals and connected in the shortest distance.
- Place the filter capacitors connected to the FB pin, IS pin and ZCD pin immediately near the respective terminals and connect them in the shortest distance. Especially separate the negative-side pattern of FB pin from other patterns wherever possible.
- Do not place the high impedance control circuit and the patterns just below the transformer.

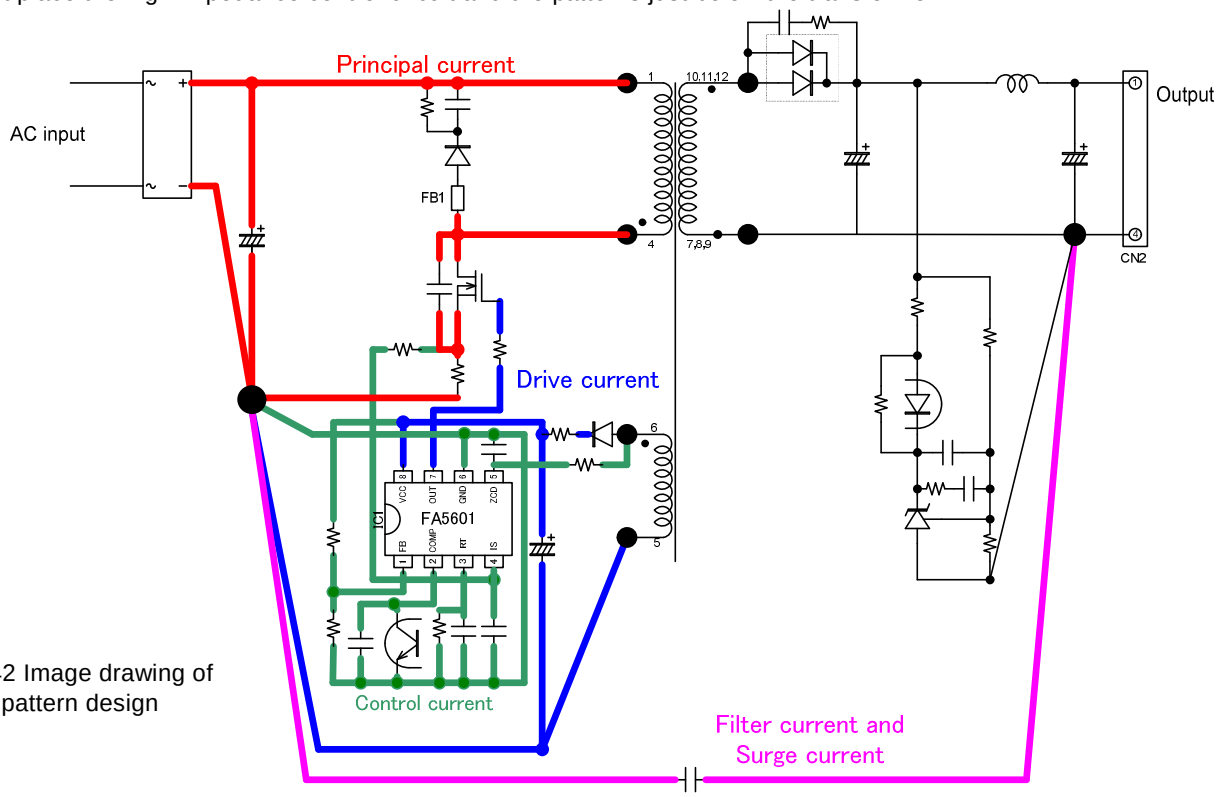


Fig.42 Image drawing of pattern design

17. Precautions in use regarding terminal noise

Condition	Pin	Malfunction in fear	Input regulations	Cautions in design
Input noise (within absolute maximum ratings)	FB	switching may stop when noise is over overvoltage protection level	input signal for feedback voltage of output voltage or the fixed voltage	connect condenser near terminal
		IC may become standby mode when noise is under short detection level (after standby mode cancellation become restart operation)		
		offset occurs in output voltage and output voltage rises or falls by a noise		
	COMP	on width may become not constant by load, output may change heavily	cancel noise	confirm sufficiently phase compensation constant
		switching may become when noise is over threshold voltage		
		switching may stop when noise is under threshold voltage		
	RT	on width may become not constant by load, output may change heavily	cancel noise	connect condenser near terminal
		restriction of maximum on time may not work when voltage is higher than terminal voltage (on width may change when voltage is higher than terminal voltage)		
		on width and restriction of maximum frequency may change when voltage is lower than terminal voltage		
	IS	switching may stop become when noise is over threshold voltage	cancel noise	connect condenser near terminal
	ZCD	turn-on occurs unintentional timing, MOSFET/Diode heat and switching noise may becomes bigger by a noise	cancel noise	connect condenser near terminal
		It may not turn on when the time over turn-on threshold is less than delay time	Although Inductor and MOSFET capacitance is resonant, input voltage more than threshold over delay time	
		it may become maximum frequency mode when noise frequency is faster than maximum frequency of setting	cancel noise	
	GND	reference voltage changes, IC may not behave normally	cancel noise	ground wiring should be a wide wiring
	OUT	the output may fall not to be able to drive MOSFET normally when signals more than the ability of the driver are input	cancel noise	-
	VCC	IC may stop when noise under UVLO is input	don't input noise under UVLO when operating	connect condenser near terminal
Input minus voltage (less than absolute maximum voltage)	FB	a parasitism element works, and the malfunction such as IC stop may occur	don't input minus voltage less than maximum absolute voltage	-
	COMP			
	RT			
	IS			
	ZCD			
	VCC			
	OUT	IC may be destroyed		
Input plus voltage (more than absolute maximum voltage)	FB	IC may be destroyed	don't input plus voltage more than maximum absolute voltage	-
	COMP			
	RT			
	IS			
	ZCD			
	OUT			
	VCC			