

## TLV809

### 3-Pin Supply Voltage Supervisor

#### 1 Features

- Precision Supply Voltage Monitor: 2.5 V, 3 V, 3.3 V, 5 V
- Power-On Reset Generator with a Fixed Delay Time of 200 ms
- Supply Current: 9  $\mu$ A (Typical)
- Temperature Range:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- 3-Pin SOT-23 Package
- Pin-for-Pin Compatible with the MAX809

#### 2 Applications

- DSPs, Microcontrollers, and Microprocessors
- Wireless Communication Systems
- Portable and Battery-Powered Equipment
- Programmable Controls
- Intelligent Instruments
- Industrial Equipment
- Notebook and Desktop Computers
- Automotive Systems

#### 3 Description

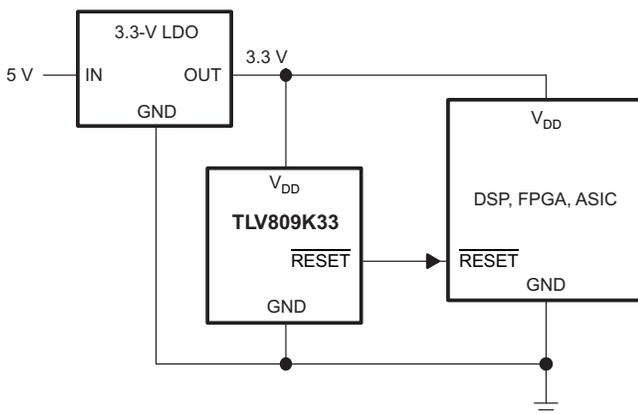
The TLV809 family of supervisory circuits provides circuit initialization and timing supervision, primarily for digital signal processors (DSPs) and processor-based systems.

During power-on,  $\overline{\text{RESET}}$  is asserted when the supply voltage ( $V_{\text{DD}}$ ) becomes greater than 1.1 V. Thereafter, the supervisory circuit monitors  $V_{\text{DD}}$  and keeps  $\overline{\text{RESET}}$  active as long as  $V_{\text{DD}}$  remains below the threshold voltage,  $V_{\text{IT}}$ . An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time ( $t_{\text{d(typ)}}$  = 200 ms) starts after  $V_{\text{DD}}$  rises above the threshold voltage,  $V_{\text{IT}}$ . When the supply voltage drops below the  $V_{\text{IT}}$  threshold voltage, the output becomes active (low) again. No external components are required. All devices in this family have a fixed sense-threshold voltage ( $V_{\text{IT}}$ ) set by an internal voltage divider.

The TLV803 has an active-low, push-pull RESET output. See the [TLV803](#) for an open-drain RESET output and the [TLV810](#) for a push-pull, active-high RESET output.

This product family is designed for supply voltages of 2.5 V, 3 V, 3.3 V, and 5 V. The circuits are available in a 3-pin SOT-23 package. The TLV809 devices are characterized for operation over a temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

Typical Application



Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV809	SOT-23 (3), DBV	2.90 mm x 1.60 mm
	SOT-23 (3), DBZ	2.92 mm x 1.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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## 4 Revision History

### Changes from Revision C (February 2012) to Revision D

**Page**

• Added <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Overview</i> section, <i>Feature Description</i> section, <i>Device Functional Modes</i> section, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	<b>1</b>
• Deleted pinout drawing from page 1 .....	<b>1</b>
• Changed <i>Description</i> section: added third paragraph and changed section wording for clarity .....	<b>1</b>
• Changed <i>Voltage Options</i> table: changed title, deleted duplicated data already in POA .....	<b>3</b>
• Deleted soldering temperature parameter from <i>Absolute Maximum Ratings</i> table .....	<b>3</b>
• Changed $I_{DD}$ parameter test conditions in <i>Electrical Characteristics</i> table .....	<b>4</b>

### Changes from Revision B (September 2010) to Revision C

**Page**

• Changed TLV809L30 DBZ ordering information column in Package/Ordering Information table .....	<b>3</b>
• Changed TLV809K33 DBZ ordering information column in Package/Ordering Information table .....	<b>3</b>
• Changed first TLV809I50 DBZ ordering information entry in Package/Ordering Information table .....	<b>3</b>

### Changes from Revision A (July 2010) to Revision B

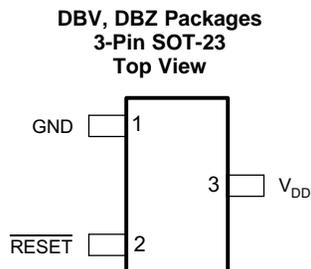
**Page**

• Updated document format to current standards .....	<b>1</b>
• Added DBZ package to pinout figure .....	<b>1</b>
• Added DBZ package to <i>Package/Ordering Information</i> table .....	<b>3</b>
• Added <i>Thermal Information</i> table .....	<b>3</b>
• Changed <a href="#">Figure 3</a> .....	<b>6</b>

## 5 Voltage Options

PRODUCT	THRESHOLD VOLTAGE
TLV809J25	2.25 V
TLV809L30	2.64 V
TLV809K33	2.93 V
TLV809I50	4.55 V

## 6 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	GND	—	Ground pin. This pin must be connected to ground with a low-impedance connection.
2	$\overline{\text{RESET}}$	O	$\overline{\text{RESET}}$ pin. $\overline{\text{RESET}}$ is an active low signal, asserting when $V_{\text{DD}}$ is below the threshold voltage. When $V_{\text{DD}}$ rises above $V_{\text{IT}}$ , there is a delay time ( $t_d$ ) until $\overline{\text{RESET}}$ deasserts. $\overline{\text{RESET}}$ is a push-pull output stage.
3	$V_{\text{DD}}$	I	Supply voltage pin. A 0.1- $\mu\text{F}$ ceramic capacitor from this pin to ground is recommended to improve stability of the threshold voltage.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{\text{DD}}$	Supply voltage <sup>(2)</sup>		7	V
	All other pins <sup>(2)</sup>	-0.3	7	
$I_{\text{OL}}$	Maximum low output current		5	mA
$I_{\text{OH}}$	Maximum high output current		-5	mA
$I_{\text{IK}}$	Input clamp current ( $V_{\text{I}} < 0$ or $V_{\text{I}} > V_{\text{DD}}$ )		$\pm 20$	mA
$I_{\text{OK}}$	Output clamp current ( $V_{\text{O}} < 0$ or $V_{\text{O}} > V_{\text{DD}}$ )		$\pm 20$	mA
$T_{\text{A}}$	Operating free-air temperature	-40	85	$^{\circ}\text{C}$
$T_{\text{stg}}$	Storage temperature	-65	150	$^{\circ}\text{C}$

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND. For reliable operation, do not operate the device at 7 V for more than  $t = 1000\text{h}$  continuously.

## 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

at specified temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>DD</sub>	Supply voltage	2		6	V
C <sub>IN</sub>	V <sub>DD</sub> bypass capacitor		0.1		μF
T <sub>A</sub>	Operating free-air temperature range	–40		85	°C

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TLV809		UNIT
		DBV (SOT-23)	DBZ (SOT-23)	
		3 PINS	3 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	242.1	286.9	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	213.0	105.6	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	123.4	124.4	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	45.7	25.8	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	130.9	107.9	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

at T<sub>A</sub> = –40°C to +85°C (unless otherwise noted); typical values are at T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V <sub>OH</sub>	High-level output voltage	V <sub>DD</sub> = 2.5 V to 6 V, I <sub>OH</sub> = –500 μA	V <sub>DD</sub> – 0.2			V	
		V <sub>DD</sub> = 3.3 V, I <sub>OH</sub> = –2 mA	V <sub>DD</sub> – 0.4				
		V <sub>DD</sub> = 6 V, I <sub>OH</sub> = –4 mA	V <sub>DD</sub> – 0.4				
V <sub>OL</sub>	Low-level output voltage	V <sub>DD</sub> = 2 V to 6 V, I <sub>OH</sub> = 500 μA	0.2			V	
		V <sub>DD</sub> = 3.3 V, I <sub>OH</sub> = 2 mA	0.4				
		V <sub>DD</sub> = 6 V, I <sub>OH</sub> = 4 mA	0.4				
Power-up reset voltage <sup>(1)</sup>		V <sub>DD</sub> ≥ 1.1 V, I <sub>OL</sub> = 50 μA	0.2			V	
V <sub>IT-</sub>	Negative-going input threshold voltage <sup>(2)</sup>	T <sub>A</sub> = –40°C to +85°C	TLV809J25	2.20	2.25	2.30	V
			TLV809L30	2.58	2.64	2.70	
			TLV809K33	2.87	2.93	2.99	
			TLV809I50	4.45	4.55	4.65	
V <sub>hys</sub>	Hysteresis		TLV809J25	30		mV	
			TLV809L30	35			
			TLV809K33	40			
			TLV809I50	60			
I <sub>DD</sub>	Supply current	V <sub>DD</sub> = 2 V, RESET is unconnected	9		12	μA	
		V <sub>DD</sub> = 6 V, RESET is unconnected	20		25		
C <sub>I</sub>	Input capacitance	V <sub>I</sub> = 0 V to V <sub>DD</sub>	5			pF	

(1) The lowest supply voltage at which  $\overline{\text{RESET}}$  becomes active.  $t_r, v_{DD} \geq 15 \text{ ms/V}$ .

(2) To ensure best stability of the threshold voltage, place a bypass capacitor (0.1-μF ceramic) near the supply pins.

## 7.6 Timing Requirements

at  $T_A = 25^\circ\text{C}$ ,  $R_L = 1\text{ M}\Omega$ , and  $C_L = 50\text{ pF}$

		MIN	NOM	MAX	UNIT
$t_w$	Pulse duration at $V_{DD}$	$V_{DD} = V_{IT-} + 0.2\text{ V}$ , $V_{DD} = V_{IT-} - 0.2\text{ V}$		3	$\mu\text{s}$

## 7.7 Switching Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $R_L = 1\text{ M}\Omega$ , and  $C_L = 50\text{ pF}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_d$	Delay time	$V_{DD} \geq V_{IT-} + 0.2\text{ V}$ ; see Figure 1	120	200	280	ms
$t_{PHL}$	Propagation (delay) time, high-to-low-level output	$V_{DD}$ to $\overline{\text{RESET}}$ delay $V_{IL} = V_{IT-} - 0.2\text{ V}$ , $V_{IH} = V_{IT-} + 0.2\text{ V}$		1		$\mu\text{s}$

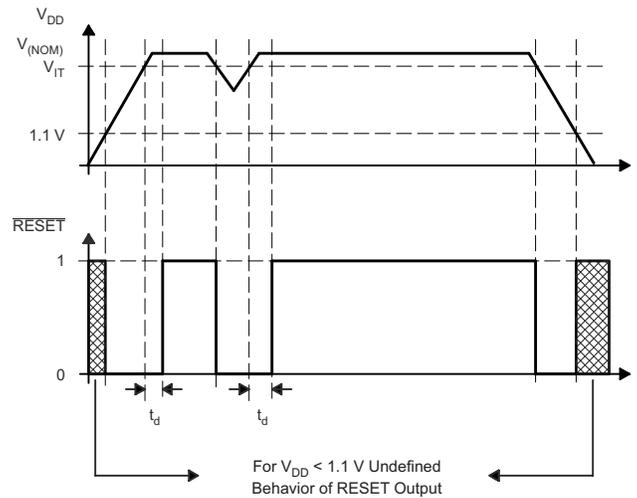
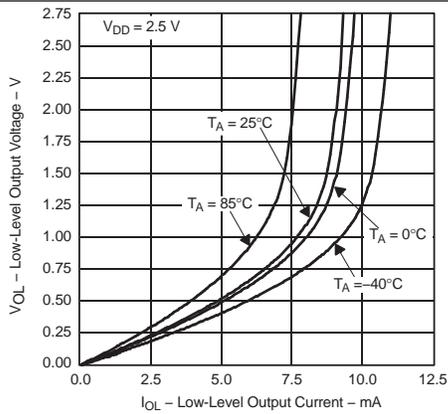
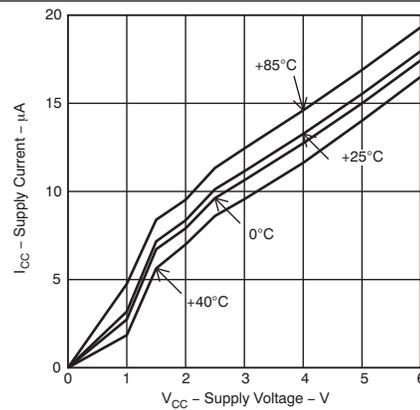


Figure 1. Timing Diagram

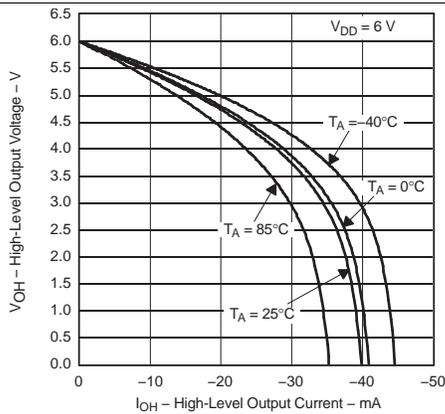
## 7.8 Typical Characteristics



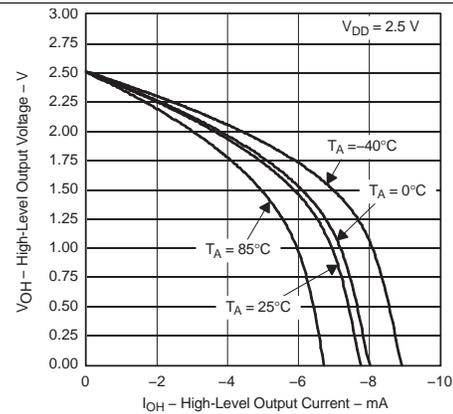
**Figure 2. Low-Level Output Voltage vs Low-Level Output Current**



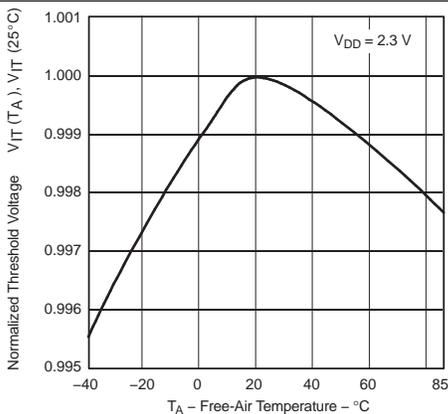
**Figure 3. Supply Current vs Supply Voltage**



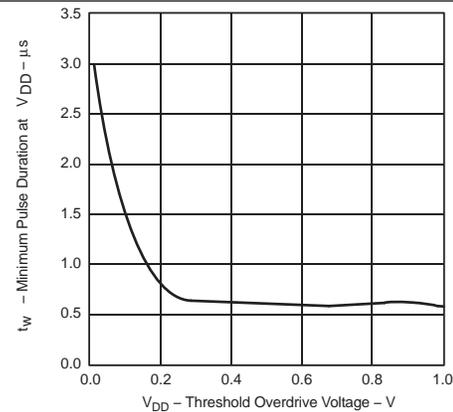
**Figure 4. High-Level Output Voltage vs High-Level Output Current**



**Figure 5. High-Level Output Voltage vs High-Level Output Current**



**Figure 6. Normalized Input Threshold Voltage vs Free-Air Temperature at V<sub>DD</sub>**



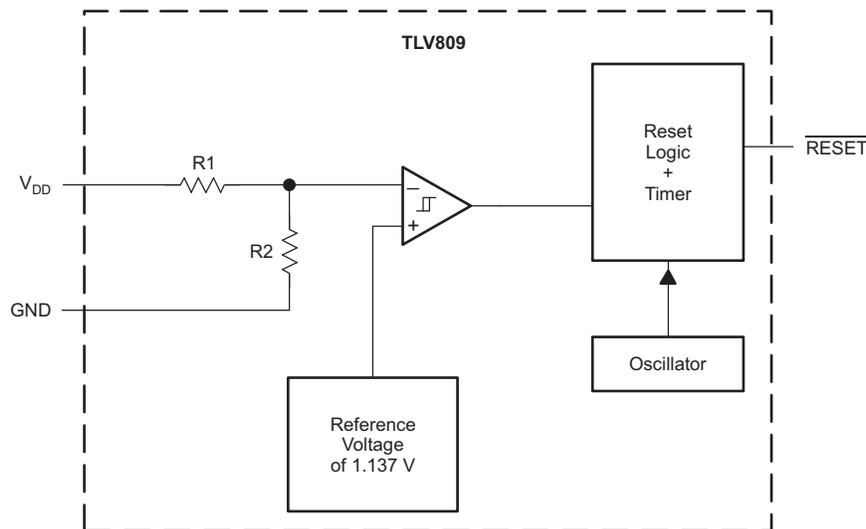
**Figure 7. Minimum Pulse Duration at V<sub>DD</sub> vs V<sub>DD</sub> Threshold Overdrive Voltage**

## 8 Detailed Description

### 8.1 Overview

The TLV809 is a 3-pin voltage detector with fixed detection thresholds, an active-low push-pull  $\overline{\text{RESET}}$  output, and an internal timer to delay the  $\overline{\text{RESET}}$  signal when  $V_{\text{DD}}$  rises above the threshold voltage.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Supply Voltage Monitoring

The device actively monitors its supply voltage to ensure that the power supply is above a certain voltage threshold.

The device offers various fixed threshold options that are approximately 10% below several standard supply voltages (2.5 V, 3.0 V, 3.3 V, 5.0 V).

#### 8.3.2 $\overline{\text{RESET}}$ Output

The device has a  $\overline{\text{RESET}}$  output to indicate the status of the input power supply.

$\overline{\text{RESET}}$  is an active low signal, asserting when  $V_{\text{DD}}$  is below the threshold voltage. When  $V_{\text{DD}}$  rises above  $V_{\text{IT}}$ , there is a delay time ( $t_d$ ) until  $\overline{\text{RESET}}$  deasserts.

$\overline{\text{RESET}}$  is a push-pull output stage.

### 8.4 Device Functional Modes

When the input supply voltage is in its recommended operating range (2 V to 6 V), the device is in a normal operational mode. In normal operational mode the device monitors  $V_{\text{DD}}$  for undervoltage detection.

When the input supply is below its recommended operating range, the device is in shutdown mode and therefore tries to assert  $\overline{\text{RESET}}$ .

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

#### 9.1.1 $V_{DD}$ Transient Rejection

The device has built-in rejection of fast transients on the  $V_{DD}$  pin. The rejection of transients depends on both the duration and the amplitude of the transient. The amplitude of the transient is measured from the bottom of the transient to the negative threshold voltage of the device, as shown in Figure 8.

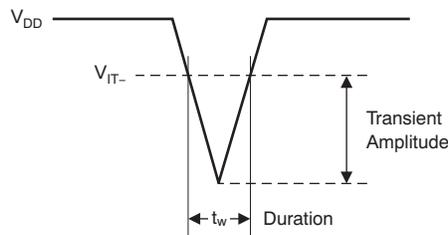


Figure 8. Voltage Transient Measurement

The device does not respond to transients that are fast duration and low amplitude or long duration and small amplitude. Figure 7 illustrates the relationship between the transient amplitude and duration needed to trigger a reset. Any combination of duration and amplitude above the curve generates a reset signal.

#### 9.1.2 Reset During Power-Up and Power-Down

The device output is valid when  $V_{DD}$  is greater than 1.1 V. When  $V_{DD}$  is less than 1.1 V, the output transistor turns off and becomes high impedance. The voltage on the  $\overline{\text{RESET}}$  pin rises to the voltage level connected to the pullup resistor. Figure 9 shows a typical waveform for power-up.

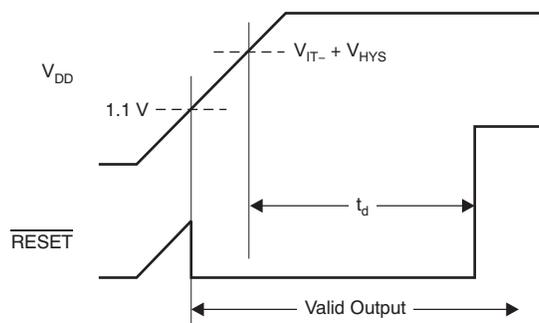


Figure 9. Power-Up Response

## 9.2 Typical Application

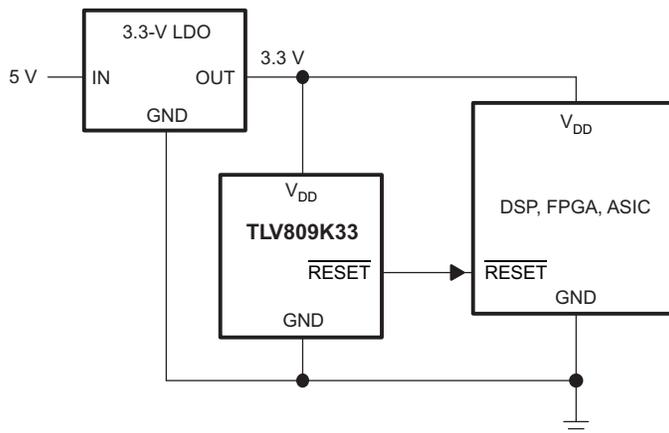


Figure 10. Monitoring a 3.3-V Supply

### 9.2.1 Design Requirements

The device must ensure that the supply voltage does not drop more than 15% below 3.3 V. If the supply voltage falls below 3.3 V – 15%, then the load must be disabled.

### 9.2.2 Detailed Design Procedure

The TLV809K33 is selected to ensure that V<sub>DD</sub> is greater than 2.87 V when the load is enabled.

### 9.2.3 Application Curve

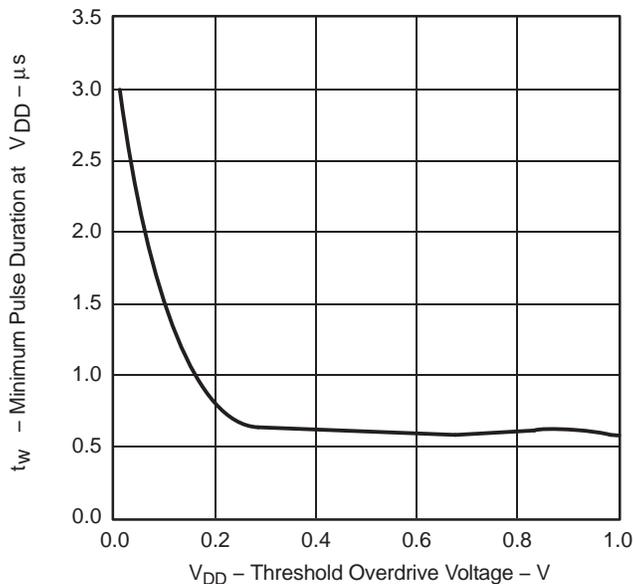


Figure 11. Minimum Pulse Duration at V<sub>DD</sub> vs V<sub>DD</sub> Threshold Overdrive Voltage

## 10 Power Supply Recommendations

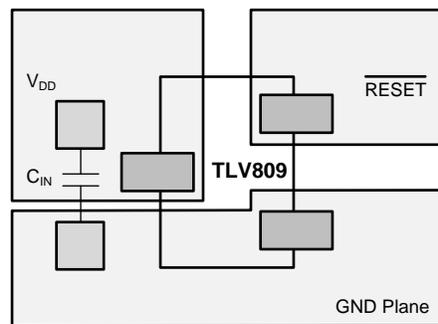
Power the device with a low-impedance supply. A 0.1- $\mu$ F bypass capacitor from  $V_{DD}$  to ground is recommended.

## 11 Layout

### 11.1 Layout Guidelines

Place the device near the load for the input power supply, with a low-impedance connection to the power supply pins of the load to sense the supply voltage.

### 11.2 Layout Example



**Figure 12. Example Layout**

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

TLV803 Data Sheet, [SBVS157](#)

TLV810 Data Sheet, [SBVS158](#)

### 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.3 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV809I50DBVR	ACTIVE	SOT-23	DBV	3	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VTBI	<a href="#">Samples</a>
TLV809I50DBVT	ACTIVE	SOT-23	DBV	3	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VTBI	<a href="#">Samples</a>
TLV809I50DBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BCMV	<a href="#">Samples</a>
TLV809I50DBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BCMV	<a href="#">Samples</a>
TLV809J25DBVR	ACTIVE	SOT-23	DBV	3	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VTCI	<a href="#">Samples</a>
TLV809J25DBVT	ACTIVE	SOT-23	DBV	3	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VTCI	<a href="#">Samples</a>
TLV809J25DBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BCMT	<a href="#">Samples</a>
TLV809J25DBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BCMT	<a href="#">Samples</a>
TLV809K33DBVR	ACTIVE	SOT-23	DBV	3	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VTRI	<a href="#">Samples</a>
TLV809K33DBVT	ACTIVE	SOT-23	DBV	3	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VTRI	<a href="#">Samples</a>
TLV809K33DBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BCMX	<a href="#">Samples</a>
TLV809K33DBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BCMX	<a href="#">Samples</a>
TLV809L30DBVR	ACTIVE	SOT-23	DBV	3	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VTXI	<a href="#">Samples</a>
TLV809L30DBVT	ACTIVE	SOT-23	DBV	3	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VTXI	<a href="#">Samples</a>
TLV809L30DBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BCMZ	<a href="#">Samples</a>
TLV809L30DBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BCMZ	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:  
**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

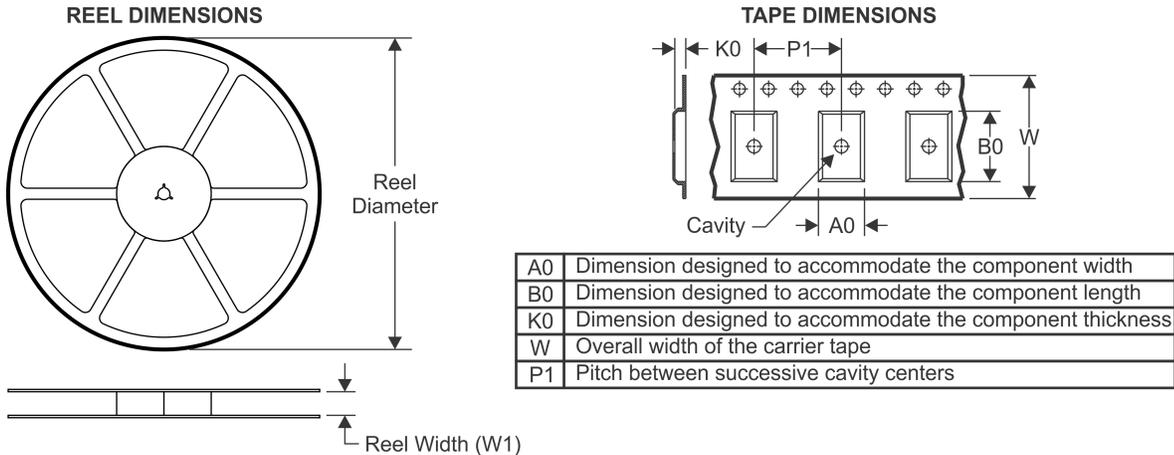
<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

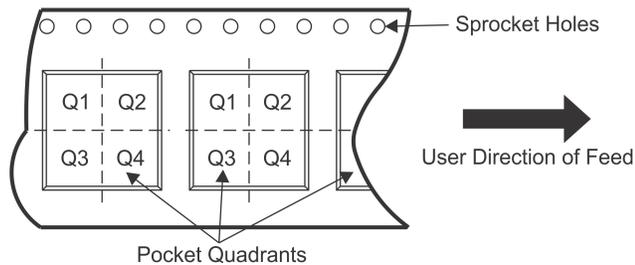
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## TAPE AND REEL INFORMATION

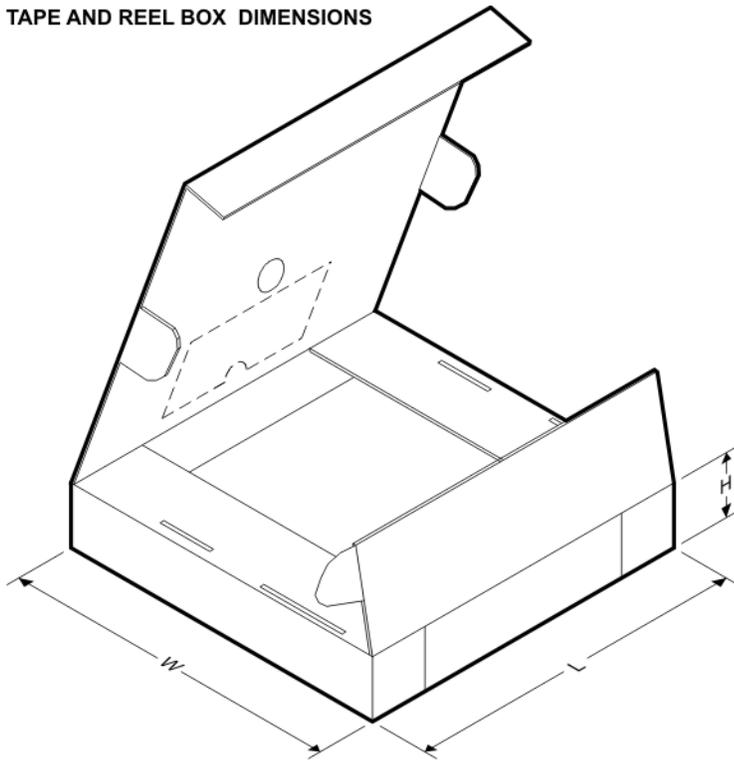


### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV809I50DBVR	SOT-23	DBV	3	3000	180.0	9.0	3.3	3.2	1.47	4.0	8.0	Q3
TLV809I50DBVT	SOT-23	DBV	3	250	180.0	9.0	3.3	3.2	1.47	4.0	8.0	Q3
TLV809I50DBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV809I50DBZT	SOT-23	DBZ	3	250	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV809J25DBVR	SOT-23	DBV	3	3000	180.0	9.0	3.3	3.2	1.47	4.0	8.0	Q3
TLV809J25DBVT	SOT-23	DBV	3	250	180.0	9.0	3.3	3.2	1.47	4.0	8.0	Q3
TLV809J25DBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV809J25DBZT	SOT-23	DBZ	3	250	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV809K33DBVR	SOT-23	DBV	3	3000	178.0	9.0	3.3	3.2	1.47	4.0	8.0	Q3
TLV809K33DBVT	SOT-23	DBV	3	250	178.0	8.4	3.3	3.2	1.47	4.0	8.0	Q3
TLV809K33DBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV809K33DBZT	SOT-23	DBZ	3	250	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV809L30DBVR	SOT-23	DBV	3	3000	180.0	9.0	3.3	3.2	1.47	4.0	8.0	Q3
TLV809L30DBVT	SOT-23	DBV	3	250	180.0	9.0	3.3	3.2	1.47	4.0	8.0	Q3
TLV809L30DBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV809L30DBZT	SOT-23	DBZ	3	250	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

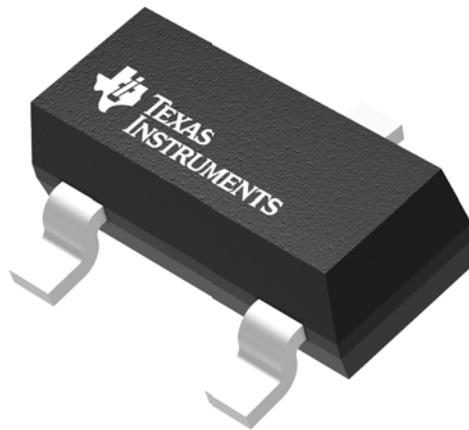
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV809I50DBVR	SOT-23	DBV	3	3000	182.0	182.0	20.0
TLV809I50DBVT	SOT-23	DBV	3	250	182.0	182.0	20.0
TLV809I50DBZR	SOT-23	DBZ	3	3000	203.0	203.0	35.0
TLV809I50DBZT	SOT-23	DBZ	3	250	203.0	203.0	35.0
TLV809J25DBVR	SOT-23	DBV	3	3000	182.0	182.0	20.0
TLV809J25DBVT	SOT-23	DBV	3	250	182.0	182.0	20.0
TLV809J25DBZR	SOT-23	DBZ	3	3000	203.0	203.0	35.0
TLV809J25DBZT	SOT-23	DBZ	3	250	203.0	203.0	35.0
TLV809K33DBVR	SOT-23	DBV	3	3000	180.0	180.0	18.0
TLV809K33DBVT	SOT-23	DBV	3	250	180.0	180.0	18.0
TLV809K33DBZR	SOT-23	DBZ	3	3000	203.0	203.0	35.0
TLV809K33DBZT	SOT-23	DBZ	3	250	203.0	203.0	35.0
TLV809L30DBVR	SOT-23	DBV	3	3000	182.0	182.0	20.0
TLV809L30DBVT	SOT-23	DBV	3	250	182.0	182.0	20.0
TLV809L30DBZR	SOT-23	DBZ	3	3000	203.0	203.0	35.0
TLV809L30DBZT	SOT-23	DBZ	3	250	203.0	203.0	35.0

## GENERIC PACKAGE VIEW

**DBZ 3**

**SOT-23 - 1.12 mm max height**

SMALL OUTLINE TRANSISTOR



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4203227/C

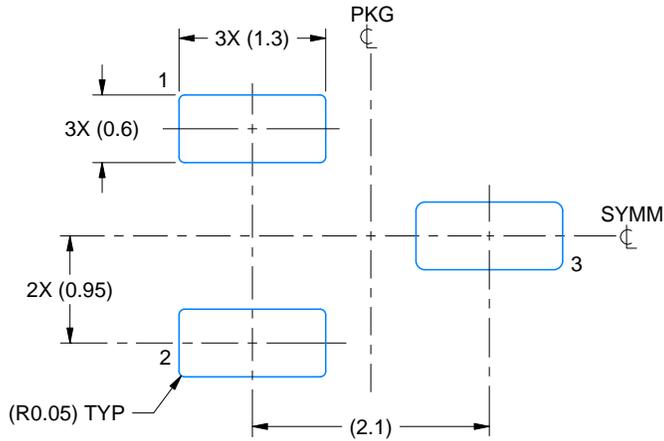


# EXAMPLE BOARD LAYOUT

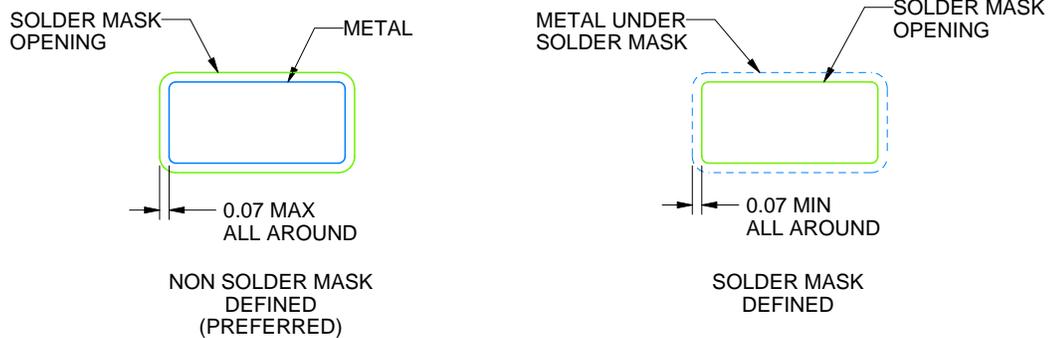
DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
SCALE:15X



SOLDER MASK DETAILS

4214838/C 04/2017

NOTES: (continued)

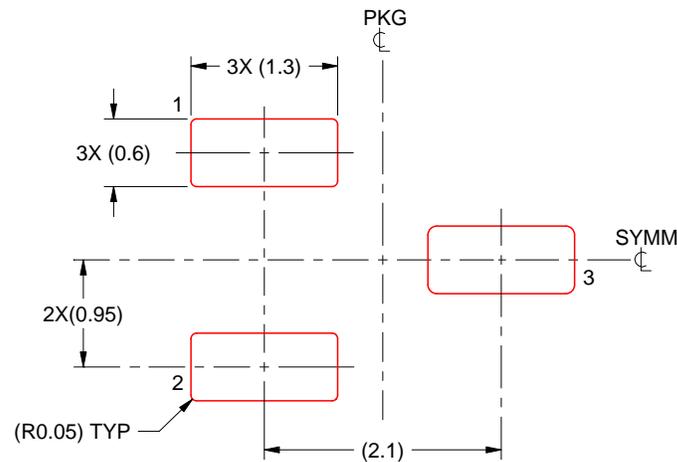
- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:15X

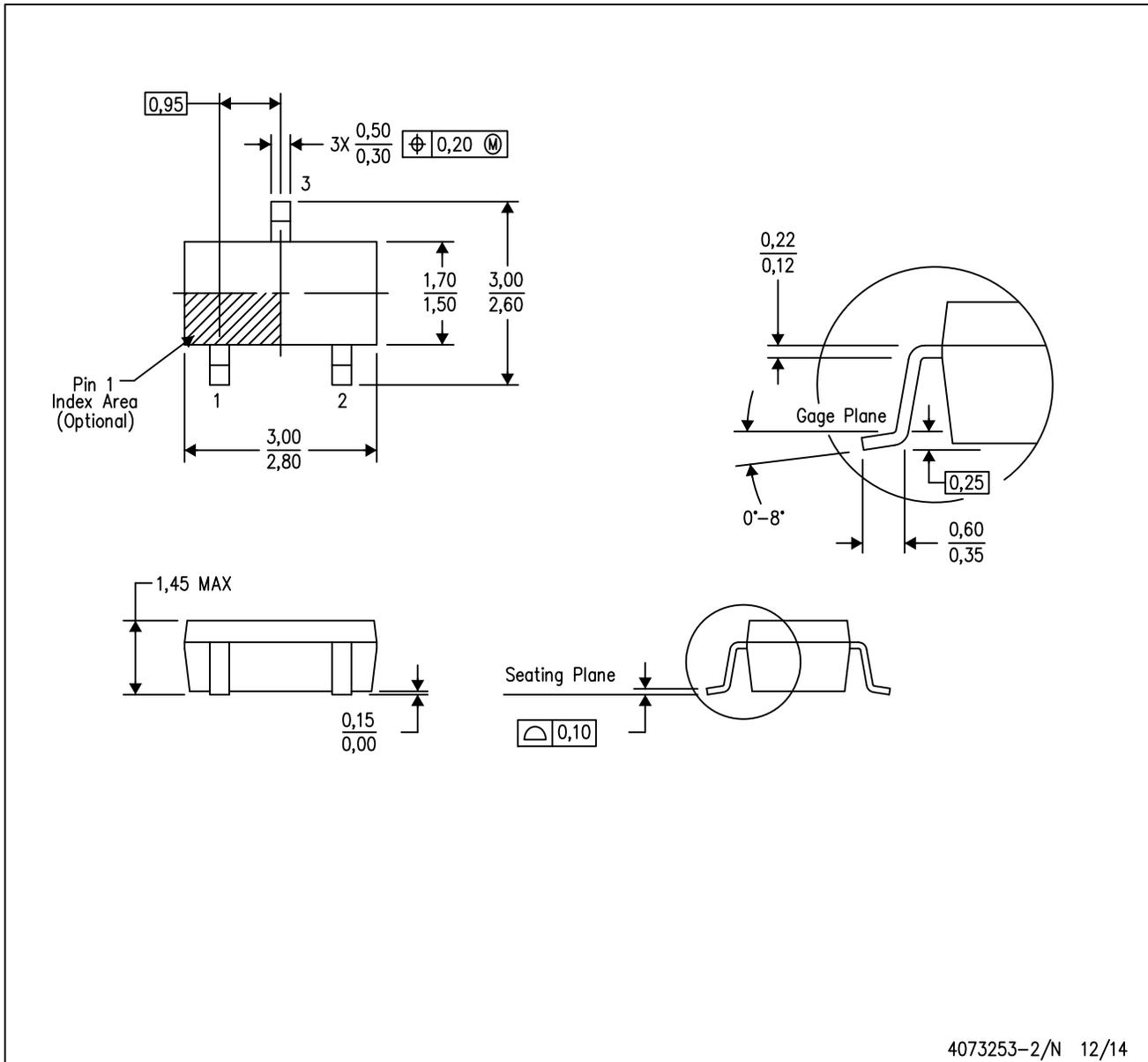
4214838/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

DBV (R-PDSO-G3)

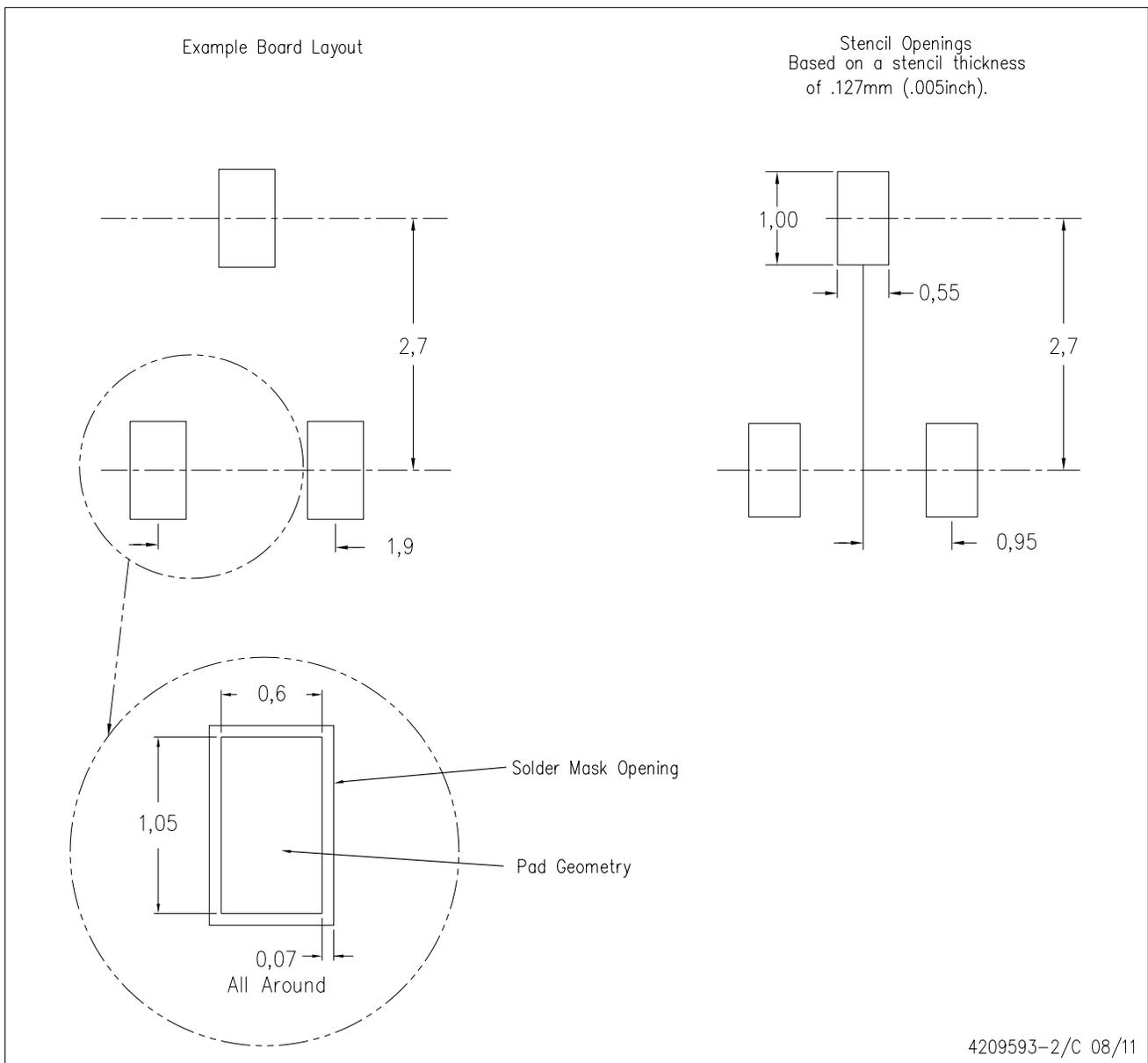
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

DBV (R-PDSO-G3)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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