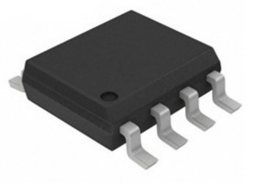
Low Offset Operational Amplifier

PRODUCT DESCRIPTION

The OP07 is a low offset voltage operational amplifier, which uses wafer-level trim to eliminate offset and further reduces offset voltage through external circuit. It also has ultra-low bias current (only 4nA) and high open-loop gain (minimum 200V/mV, 106dB). All of these characteristics make the OP07 suitable to be used as a high-gain instrumentation amplifier.

The OP07 has ±13V wide input voltage range, 106dB common-mode rejection ratio (CMRR) and high input impedance. These features make the amplifier high-precise when amplifying signals. Excellent linearity and precision are guaranteed even at high closed-loop gain. The parameters, such as time stability of offset and gain, rate of change with temperature are also excellent. After removal of external offset, the precision and stability of the OP07 make itself become the industry standard for instrument applications.



SOP8

DIP8

FEATURES

- Low Offset Voltage Drift: 1.3µV/°C (Max)
- Time Stability of Offset Voltage: 1.5µV/Month (Max)
- Low Noise: 0.6µVp-p (Max)
- Wide Input Voltage Range: ±14V (Typ)
- Wide Power Supply: ±3V to ±18V

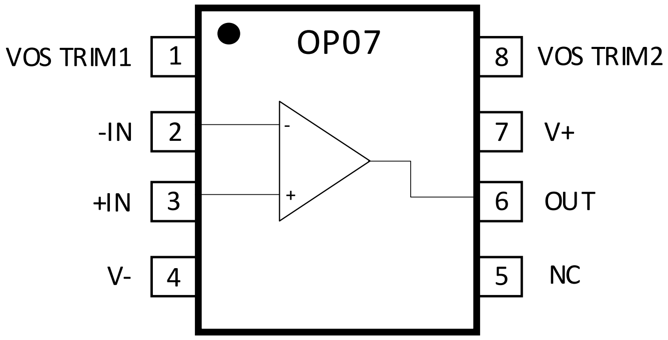
APPLICATIONS

- Wireless Base Station Control Circuit
- Optical Fiber Network Control Circuit
- Instrumentation Amplifier
- Sensor and Controller
  - Thermocouple
  - Thermal Resistance Detection
  - Strain Bridge
  - Parallel Current Detection
- Precision Filter

PRODUCT SPECIFICATION

Part Number	Package	Marking
OP07	SOP8	OP07
OP07D	DIP8	OP07D

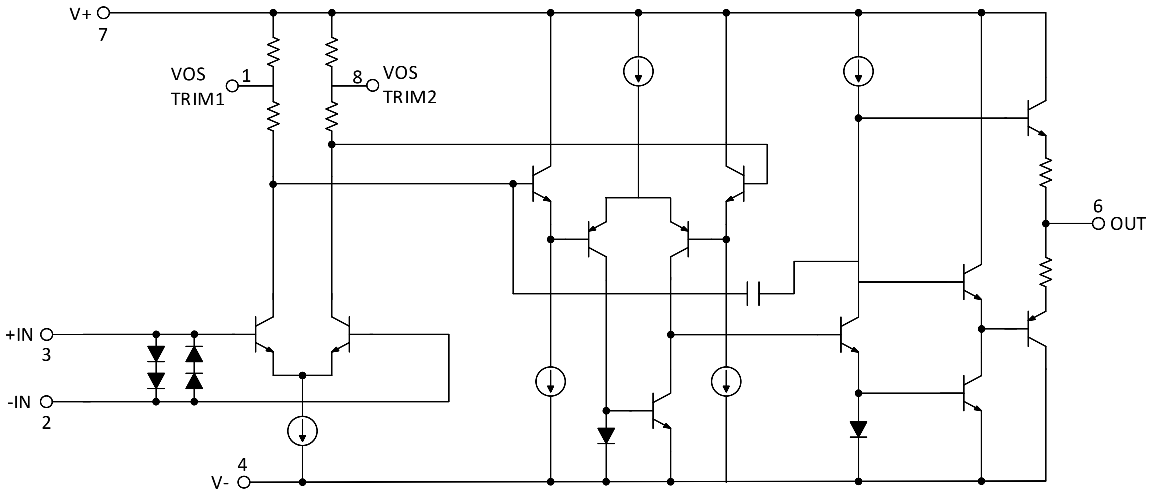
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
1	VOS TRIM1	IO	Offset Voltage Trim 1
2	-IN	I	Negative Input
3	+IN	I	Positive Input
4	V-	-	Negative Power Supply
5	NC	-	Not Connection
6	OUT	O	Output
7	V+	-	Positive Power Supply
8	VOS TRIM2	IO	Offset Voltage Trim 2

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn’t represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Ratings	Unit
Power Supply	V_S	±22	V
Input Voltage [1]	V_{IN}	±22	V
Differential Input Voltage	V_{IN}	±30	V
Storage Temperature Range	T_A	-65 ~ +125	°C
Operating Temperature Range	T_{stg}	-40 ~ +85	°C
Junction Temperature	T_J	150	°C
Lead Temperature		300	°C

Note 1: When power supply is less than ±22V, the absolute maximum value of input voltage is equal to power supply.

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, V_S=±15V.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
		Input Characteristics				
Input Offset Voltage	V_{OS}	T_A=25°C, Grade A			25	μV
		T_A=25°C, Grade B			75	
		T_A=25°C, Grade C			150	
Offset Voltage Long-term Stability	V_{OS}/Time			0.3	1.5	μV/Month
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta_T$	-0°C ≤ T_A ≤ +70°C		0.3	1.3	μV/°C
Input Bias Current	I_B			22		nA
Input Offset Current	I_{OS}			7		nA
Input Difference-mode Resistance	R_{IN}		15	50		MΩ
Input Common-mode Resistance	R_{INCM}			160		GΩ
Input Voltage Range	ICMR		±13	±14		V
		-0°C ≤ T_A ≤ +70°C	±13	±13.5		
Common-mode Rejection Ratio	CMRR	V_{CM}=±13V	106	123		dB
		-0°C ≤ T_A ≤ +70°C	103	123		
Large Signal Gain	A_{VO}	R_L≥2kΩ, V_O=±10V	106	114		dB
		R_L≥500Ω, V_O=±10V	103	112		
		-0°C ≤ T_A ≤ +70°C , R_L≥2kΩ, V_O=±10V	105	113		
		Output Characteristics				
Output Voltage Magnitude	V_O	R_L≥10kΩ	±12.5	±13.0		V
		R_L≥2kΩ	±12.0	±12.8		
		R_L≥1kΩ	±10.5	±12.0		
		-0°C ≤ T_A ≤ +70°C, R_L≥2kΩ	±12.0	±12.6		
Output Short-circuit Current	I_{SC}			21		mA
		Power Supply				
Power Supply Rejection Ratio	PSRR	V_S=±3V to ±18V	94	106		dB
		-0°C ≤ T_A ≤ +70°C	90	103		
Quiescent Power Dissipation	P_Q	V_S=±15V, No Load		80	120	mW
		V_S=±3V, No Load		5.5	8	

Parameters	Symbol	Condition	Min	Typ	Max	Unit
Dynamic Characteristics						
Gain Bandwidth Product	GBP	A_V=1	1	1.3		MHZ
Slew Rate	SR	R_L≥2kΩ	0.1	0.3		V/μs
Offset Voltage Adjustment Range		R_P=20kΩ		±3.6		mV
Noise Characteristics						
Voltage Noise	e_np-p	0.1Hz to 10Hz		0.35	0.6	μVp-p
Voltage Noise Density	e_n	f_o=10Hz		10.3	18.0	$nV/\sqrt{Hz}$
		f_o=100Hz		10.0	13.0	
		f_o=1kHz		9.6	11.0	
Current Noise	I_np-p			14	30	pA_{p-p}
Current Noise Density	I_n	f_o=10Hz		0.32	0.80	$pA/\sqrt{Hz}$
		f_o=100Hz		0.14	0.23	
		f_o=1kHz		0.12	0.17	

TYPICAL CHARACTERISTICS CURVE

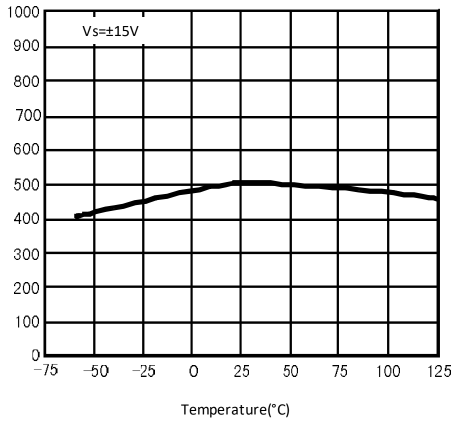


Figure 1. Open-loop Gain VS. Temperature

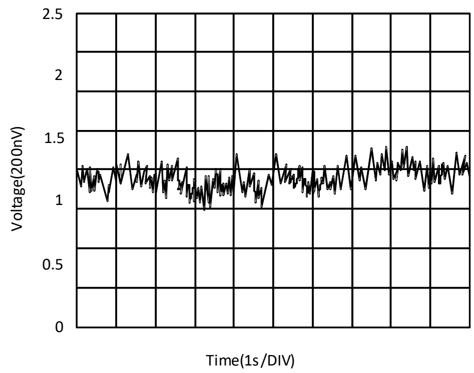


Figure 2. Low-frequency Noise

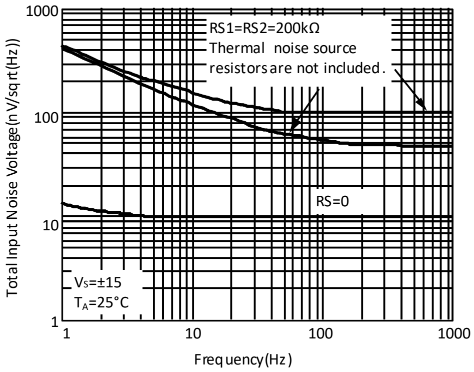


Figure 3. Total Input Noise Voltage VS. Frequency

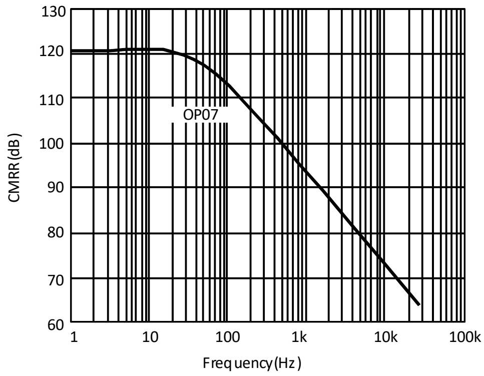


Figure 4. CMRR VS. Frequency

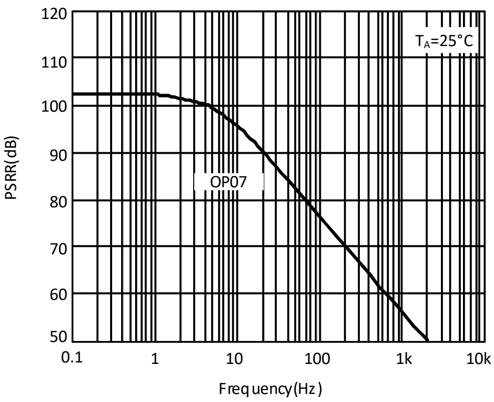


Figure 5. PSRR VS. Frequency

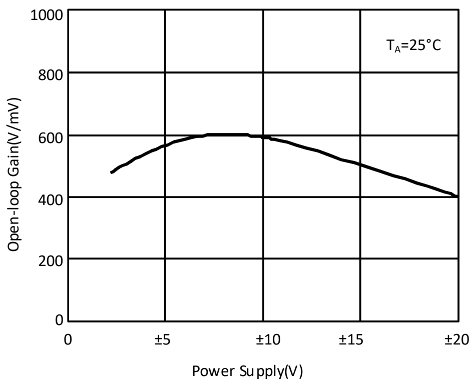


Figure 6. Open-loop Gain VS. Power Supply

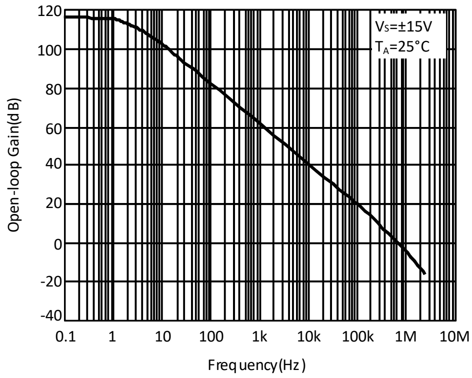


Figure 7. Open-loop Gain Frequency Response

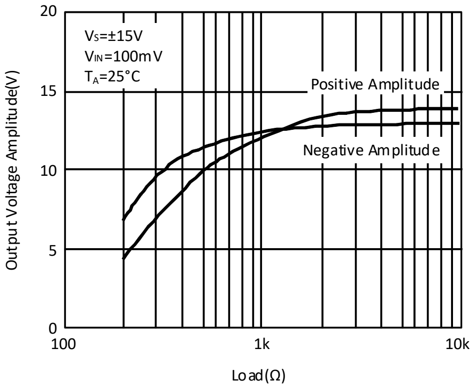


Figure 8. Output Voltage Amplitude VS. Load

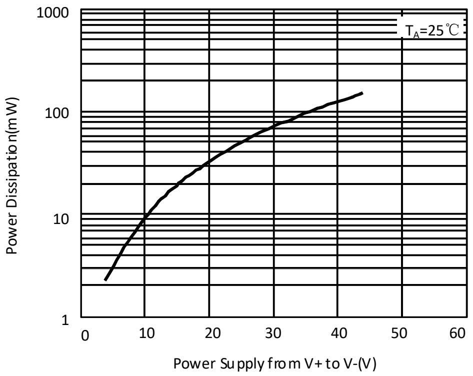


Figure 9. Power Dissipation VS. Power Supply

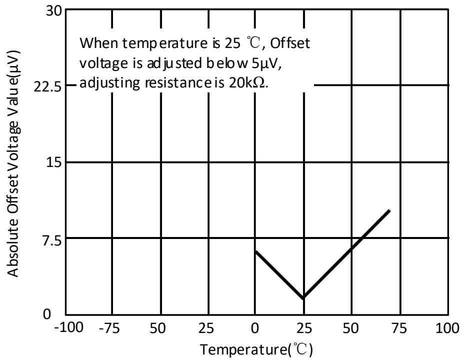


Figure 10. Trimmed Offset Voltage VS. Temperature

TYPICAL APPLICATION

In case of 500pF load capacitance and ±10V amplitude, the OP07 can provide stable operating characteristics. And large load capacitance needs to be decoupled by 50Ω resistance.

The stray difference-temperature voltage generated by different metals in touch with the input terminals can deteriorate the drift performance. Therefore, the best operating environment is to keep the two inputs contact at the same temperature. It is better to approach the package temperature.

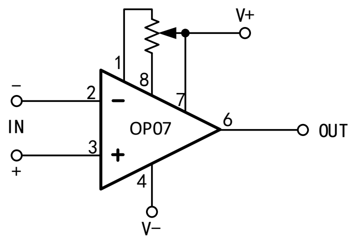


Figure 11. Optical Offset Elimination Circuit

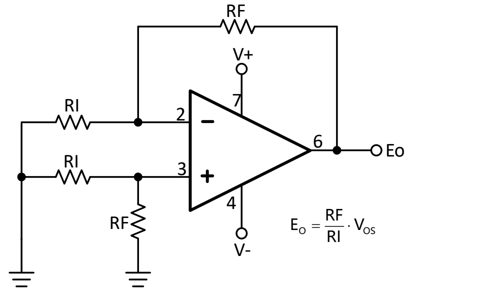


Figure 12. Typical Offset Voltage Measurement Circuit

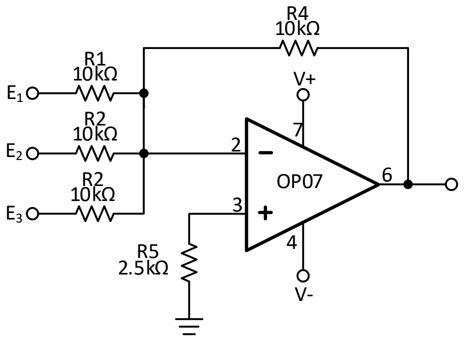


Figure 13. Precise Summing Circuit

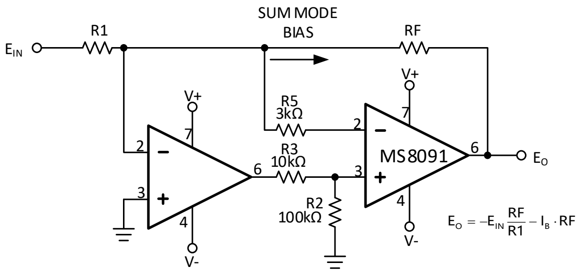


Figure 14. High-speed, Low Offset Compound Amplifier

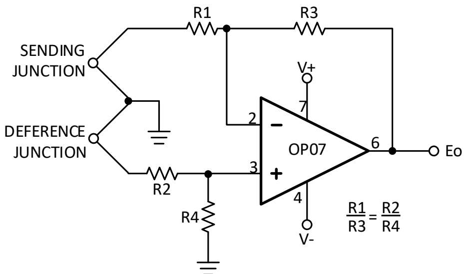


Figure 15. High-Stable Thermocouple Amplifier

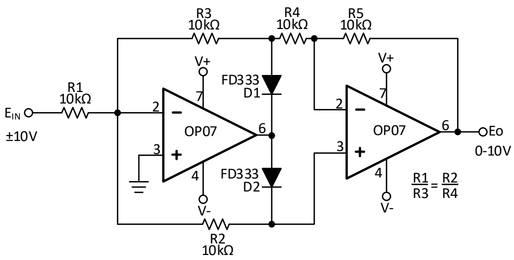


Figure 16. Precise Absolute Value Circuit

PACKAGE OUTLINE DIMENSIONS

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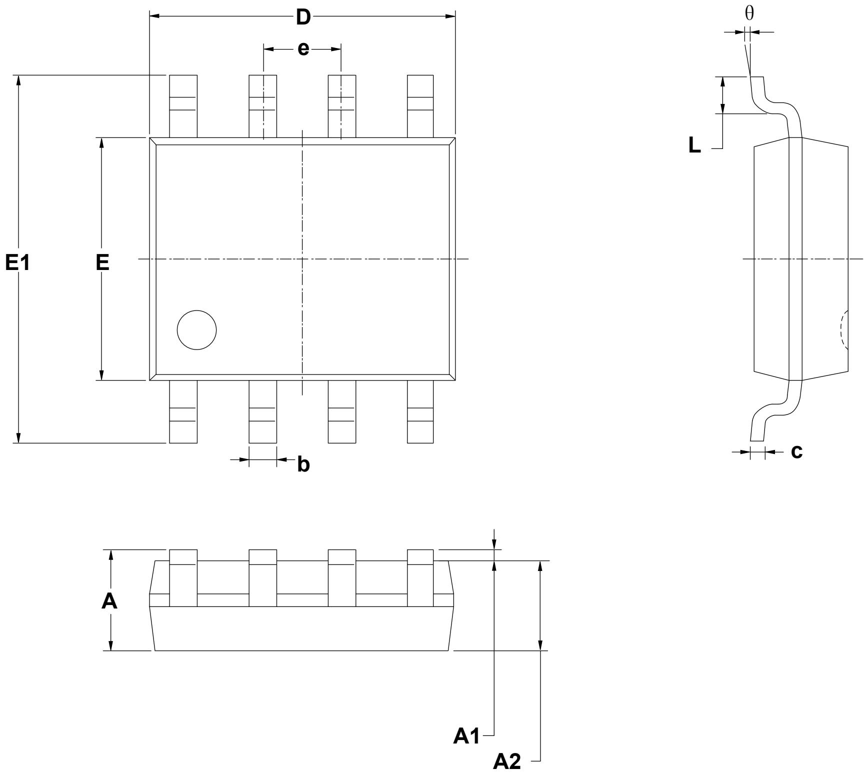
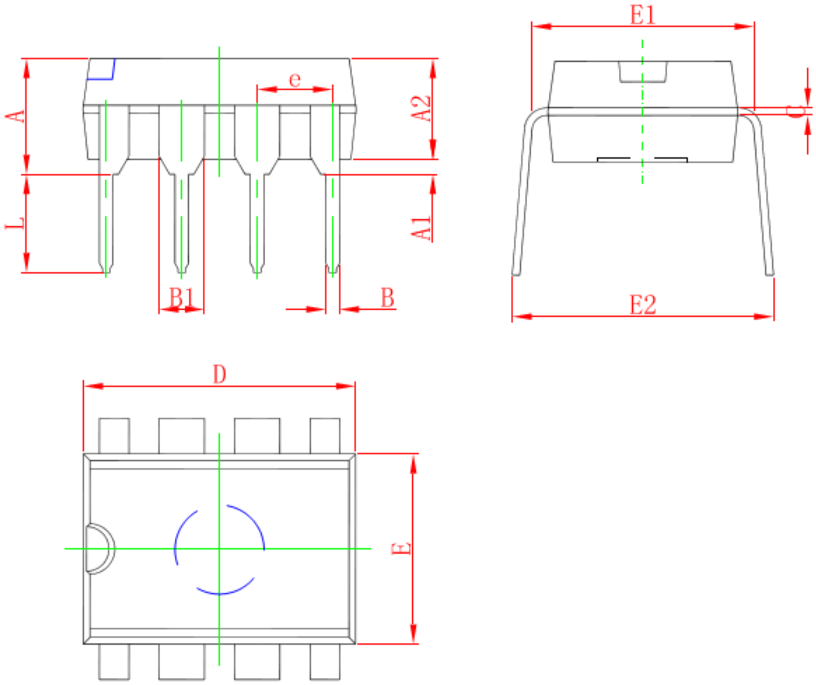


Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0 º	8 º	0 º	8 º

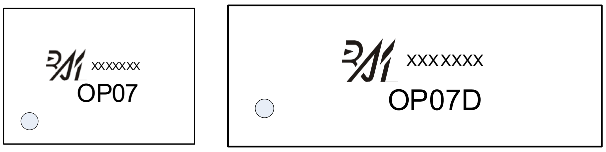
DIP8



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524(BSC)		0.060(BSC)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540(BSC)		0.100(BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

MARKING and PACKAGING SPECIFICATION

1. Marking Drawing Description



Product Name: OP07, OP07D

Product Code: XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
OP07	SOP8	2500	1	2500	8	20000

Device	Package	Piece/Tube	Tube/Box	Piece/Box	Box/Carton	Piece/Carton
OP07D	DIP8	50	40	2000	10	20000

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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1、The operator shall ground through the anti-static wristband.

2、The equipment shell must be grounded.

3、The tools used in the assembly process must be grounded.

4、Must use conductor packaging or anti-static materials packaging or transportation.

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