

CA-IS308x 5kV_{RMS} Isolated Half/Full-Duplex RS-485/RS-422 Transceivers

1. Features

- **High-Performance and Compliant with RS-485 EIA/TIA-485 Standard**
 - 500kbps, 10Mbps or 20Mbps data rate optional
 - 1/8 unit load enables up to 256 nodes on the bus
 - 2.375V to 5.5V logic side supply voltage and 3 V to 5.5 V bus side supply voltage
 - Bus common mode supply rage
 - CA-IS3080/86: -15V to +15V
 - CA-IS3082/88: -7V to +12V
 - CMTI: ±150kV/μs (typical)
 - Output current limited and thermal shutdown protection on driver side
 - Open、short circuit protection and bus failure protection
 - Wide operating temperature range: -40°C to 125°C
 - Wide-body SOIC16-WB(W) Package
 - High lifetime: >40 years
- **Safety Regulatory Approvals**
 - VDE 0884-11 and DIN EN & IEC 62368-1 VDE reinforced isolation (pending)
 - UL according to UL1577: 5kV_{RMS} per minute
 - 5kV_{RMS} reinforced insulation certifications IEC 62368-1 and IEC 61010-1 Approvals
 - 5kV_{RMS} reinforced insulation certifications EN 62368-1 and EN 61010-1 Approvals
 - 5kV_{RMS} reinforced insulation certifications GB 4943.1-2011 and GB 8898-2011 CQC Approvals

2. Applications

- Industrial Automation Equipment
- Grid infrastructure
- Solar inverter
- Motor drivers
- HVAC

3. General Description

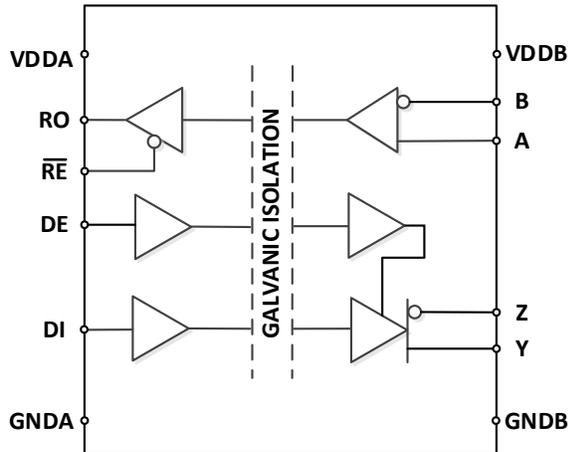
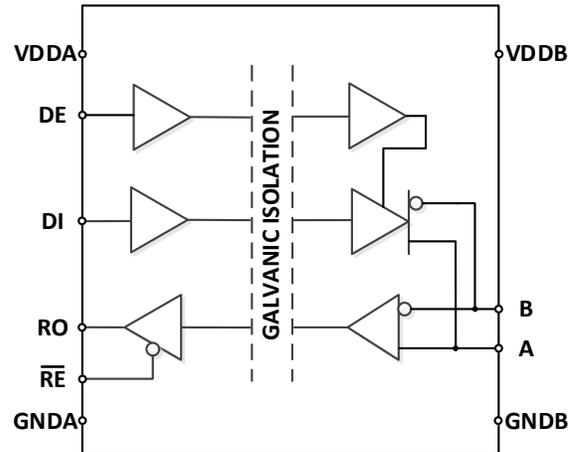
The CA-IS308x family of devices is a galvanically-isolated RS-485/RS-422 transceiver that has superior isolation and RS485 performance to meet the needs of the industrial applications. All devices of this family have the logic input and output buffers separated by a silicon oxide (SiO₂) insulation barrier that provides galvanic isolation, features up to 5000V_{RMS} (60s) of galvanic isolation and ±150kV/μs typical CMTI. Isolation improves communication by breaking ground loops and reduces noise where there are large differences in ground potential between ports.

The CA-IS308x family of devices supports multiple nodes communications on bus line, and max data rate up to 20Mbps, allowing up to 256 transceivers (loads) on a common bus. Maintaining multidrop operation and increasing the maximum data rate offers a more robust system design for reliable communication. For the CA-IS308x family of devices, The CA-IS3080 and CA-IS3086 full-duplex transceivers are designed for bidirectional data communications on multipoint bus transmission lines simultaneously. The CA-IS3082 and CS-IS3088 provide half-duplex transceivers, the driver and receiver enable pins let any node at any given moment be configured in either transmit or receive mode which decreases cable requirements.

The CA-IS308x series devices are available in wide-body SOIC16 package which is the industry standard isolated RS-485/RS-422 package, and operate over -40°C to +125°C temperature range.

Device information

Part #	Package	Package size (NOM)
CA-IS3080	SOIC16-WB(W)	10.30 mm × 7.50 mm
CA-IS3082		
CA-IS3086		
CA-IS3088		

CA-IS3080/CA-IS3086 full-duplex block diagram

CA-IS3082/CA-IS3088 half-duplex block diagram


4. Ordering Information

Table. 4-1 Ordering Information

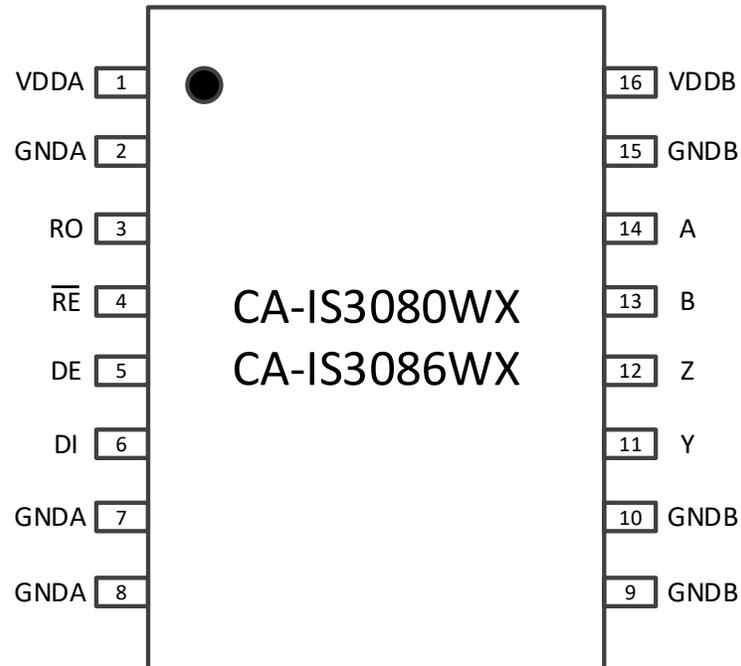
Model	V _{DDA} (V)	V _{DDB} (V)	Full/half-duplex	Transmission speed (Mbps)	Rated voltage (V)	Package
CA-IS3080WX	2.375~5.5	3.0~5.5	Full-duplex	0.5	5000	SOIC16-WB
CA-IS3086WX	2.375~5.5	3.0~5.5	Full-duplex	10	5000	SOIC16-WB
CA-IS3082WX	2.375~5.5	3.0~5.5	Half-duplex	0.5	5000	SOIC16-WB
CA-IS3082WNX	2.375~5.5	3.0~5.5	Half-duplex	0.5	5000	SOIC16-WB
CA-IS3088WX	2.375~5.5	3.0~5.5	Half-duplex	20	5000	SOIC16-WB

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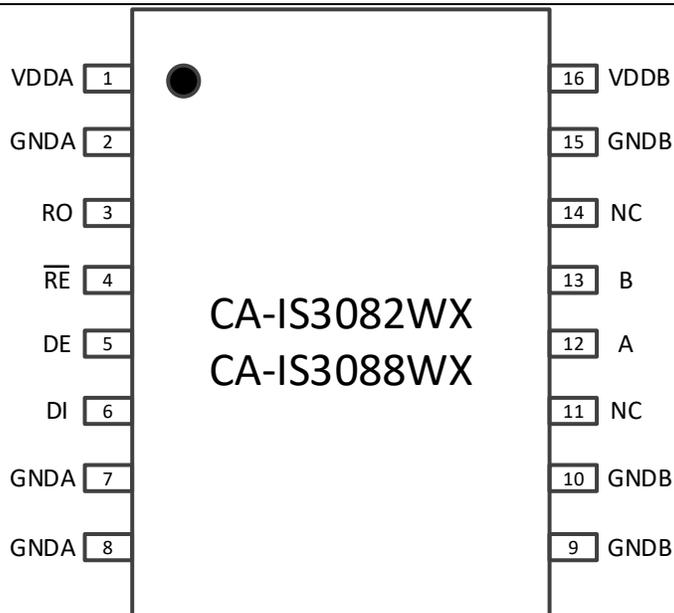
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5. Revision History

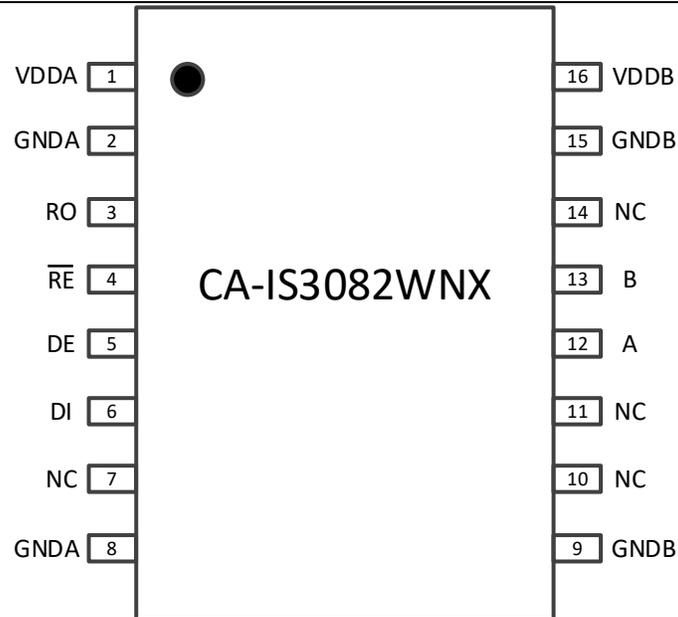
Revision Number	Description	Page Changed
Version 1.00	N/A	N/A
Version 1.01	The driver output changed to high-impedance state under thermal shutdown.	11
Version 1.02	Updated VIORM value to 1414V, VIOWM value to 1000V, VIOTM value to 1414V. Updated CA-IS3082W/WX/WNX and CA-IS3088W/WX all parameters of EC table. Add new part number CA-IS3082WNX.	8 10,12 2,6,23
Version 1.03	Deleted CA-IS3080W、CA-IS3082W、CA-IS3086W and CA-IS3088W information, Add CA-IS3080WX and CA-IS3086WX Part number and information. Add CA-IS3080/86WX VDDB operating range 3.0V~5.5V. Add CA-IS3080/86WX bus common mode operating voltage -15V to +15V.	2 1 1
Version 1.04	Updated CA-IS308x' EC table.	10~13
Version 1.05	Updated Maximum data rate up to 20Mbps of CA-IS3088WX.	1
Version 1.06	Updated POD.	22
Version 1.07	Update enable time of CA-IS3088WX driver Update Propagation delay time of CA-IS3088WX receiver	12 13

6. Pin Configuration and Description

Figure. 6-1 CA-IS3080WX and CA-IS3086WX Top View
Tab. 6-1 CA-IS3080WX and CA-IS3086WX Pin Description

Pin name	Pin number	Type	Description
VDDA	1	Power supply	Logic-Side Power Input. Bypass VDDA to GNDA with both 0.1 μ F and 1 μ F capacitors as close to the device as possible.
GNDA	2, 7, 8	Ground	Logic-Side Ground. GNDA is the ground reference for digital signals.
RO	3	Digital I/O	Receiver Data Output. Drive \overline{RE} low to enable RX. With \overline{RE} low, RO is high when $(V_A - V_B) > -20\text{mV}$ and is low when $(V_A - V_B) < -200\text{mV}$.
\overline{RE}	4	Digital I/O	Receiver Output Enable. Driver \overline{RE} low or connect to GNDA to enable RX. Drive \overline{RE} high to disable RX.
DE	5	Digital I/O	Driver Output Enable. Drive DE high to enable bus driver outputs. Drive DE low or connect to GNDA to disable bus driver outputs. DE has an internal weak pull-down to GNDA.
DI	6	Digital I/O	Driver Input. With DE high, a logic low on DI forces the noninverting output (Y) low and the inverting output (Z) high; a logic high on DI forces the noninverting output high and the inverting output low.
GNDB	9, 10, 15	Ground	Cable Side Ground. GNDB is the ground reference for the RS-485/RS-422 bus signals.
Y	11	Bus I/O	Non-inverting RS-485/RS-422 driver output .
Z	12	Bus I/O	Inverting RS-485/RS-422 driver output.
B	13	Bus I/O	Inverting RS-485/RS-422 receiver input.
A	14	Bus I/O	Non-inverting RS-485/RS-422 receiver input.
VDDB	16	Power supply	Cable Side Power Input. Bypass VDDB to GNDB with both 0.1 μ F and 1 μ F capacitors as close to the device as possible.


Figure. 6-2 CA-IS3082WX and CA-IS3088WX Top View
Tab. 6-2 CA-IS3082WX and CA-IS3088WX Pin Description

Pin name	Pin number	Type	Description
VDDA	1	Power supply	Logic-Side Power Input. Bypass VDDA to GNDA with both 0.1μF and 1μF capacitors as close to the device as possible.
GNDA	2, 7, 8	Ground	Logic-Side Ground. GNDA is the ground reference for digital signals.
RO	3	Digital I/O	Receiver Data Output. Drive \overline{RE} low to enable RX. With \overline{RE} low, RO is high when $(V_A - V_B) > -20mV$ and is low when $(V_A - V_B) < -200mV$.
\overline{RE}	4	Digital I/O	Receiver Output Enable. Driver \overline{RE} low or connect to GNDA to enable RX. Drive \overline{RE} high to disable RX.
DE	5	Digital I/O	Driver Output Enable. Drive DE high to enable bus driver outputs. Drive DE low or connect to GNDA to disable bus driver outputs. DE has an internal weak pull-down to GNDA.
DI	6	Digital I/O	Driver Input. With DE high, a logic low on DI forces the noninverting output (A) low and the inverting output (B) high; a logic high on DI forces the non-inverting output high and the inverting output low.
GNDB	9, 10, 15	Ground	Cable Side Ground. GNDB is the ground reference for the RS-485/RS-422 bus signals.
NC	11, 14	-	No internal connection
A	12	Bus I/O	Non-inverting RS-485/RS-422 receiver input and driver output.
B	13	Bus I/O	Inverting RS-485/RS-422 receiver input and driver output.
VDDB	16	Power supply	Cable Side Power Input. Bypass VDDB to GNDB with both 0.1μF and 1μF capacitor as close to the device as possible.


Figure. 6-3 CA-IS3082WNX Top View
Tab. 6-3 CA-IS3082WNX Pin Description

Pin name	Pin number	Type	Description
VDDA	1	Power supply	Logic-Side Power Input. Bypass VDDA to GNDA with both 0.1 μ F and 1 μ F capacitors as close to the device as possible.
GNDA	2, 7, 8	Ground	Logic-Side Ground. GNDA is the ground reference for digital signals.
RO	3	Digital I/O	Receiver Data Output. Drive \overline{RE} low to enable RX. With \overline{RE} low, RO is high when $(V_A - V_B) > -20\text{mV}$ and is low when $(V_A - V_B) < -200\text{mV}$.
\overline{RE}	4	Digital I/O	Receiver Output Enable. Drive \overline{RE} low or connect to GNDA to enable RX. Drive \overline{RE} high to disable RX.
DE	5	Digital I/O	Driver Output Enable. Drive DE high to enable bus driver outputs. Drive DE low or connect to GNDA to disable bus driver outputs. DE has an internal weak pull-down to GNDA.
DI	6	Digital I/O	Driver Input. With DE high, a logic low on DI forces the noninverting output (A) low and the inverting output (B) high; a logic high on DI forces the non-inverting output high and the inverting output low.
GNDB	9, 10, 15	Ground	Cable Side Ground. GNDB is the ground reference for the RS-485/RS-422 bus signals.
NC	7, 10, 11, 14	-	No internal connection
A	12	Bus I/O	Non-inverting RS-485/RS-422 receiver input and driver output.
B	13	Bus I/O	Inverting RS-485/RS-422 receiver input and driver output.
Vddb	16	Power supply	Cable Side Power Input. Bypass Vddb to GNDB with both 0.1 μ F and 1 μ F capacitor as close to the device as possible.

7. Specifications

7.1. Absolute Maximum Ratings¹

Parameters		Minimum value	Maximum value	Unit	
V _{DDA} , V _{DDB}	Power supply voltage ²	-0.5	6.0	V	
V _{IO}	Logic voltage (A, B, Y, Z)	CA-IS3080/86	-30	30	V
		CA-IS3082/88	-8	13	
V _{IO}	Logic voltage (DI, DE, \overline{RE} , RO)	-0.5	V _{DDA} +0.5 ³	V	
I _O	Output current on RO	-20	20	mA	
T _J	Junction temperature		150	°C	
T _{STG}	Storage temperature range	-65	150	°C	

Notes:

- The stresses listed under “Absolute Maximum Ratings” are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.
- All voltage values except differential I/O bus voltages are with respect to the local ground (GNDA or GNDB) and are peak voltage values.
- Maximum voltage must not be exceed 6V.

7.2. ESD Ratings

		Value	Unit
V _{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	Bus pin to GNDA	±4000
		Bus pin to GNDB	±8000
		All other pins	±4000
	Charged device model (CDM), per JEDEC Specification JESD22-C101, all pins	±2000	V

7.3. Recommended Operating Conditions

Parameters		Minimum value	Typical value	Maximum value	Unit
V _{DDA}	Power supply voltage on side A	2.375	3.3 or 5V	5.5	V
V _{DDB}	Power supply voltage on side B	3	3.3 or 5V	5.5	V
V _{OC}	Common mode voltage at bus pins: A, B, (CA-IS3082/88)	-7		12	V
V _{OC}	Common mode voltage at bus pins: A, B, Y and Z (CA-IS3080/86)	-15		15	V
V _{ID}	Differential input voltage V _{AB}	CA-IS3080/86		12	V
		CA-IS3082/88	-15	15	
R _L	Differential load resistance	54			Ω
V _{IH}	Input high voltage (DI, DE to GNDA)	2.0		V _{DDA} +0.3	V
V _{IL}	Input low voltage (DI, DE to GNDA)	-0.3		0.8	V
V _{IH}	Input high voltage (\overline{RE} to GNDA)	0.7xV _{DDA}		V _{DDA} +0.3	V
V _{IL}	Input low voltage (\overline{RE} to GNDA)	-0.3		0.3xV _{DDA}	V
DR	Data rate	CA-IS3080WX		0.5	Mbps
		CA-IS3082WX			
		CA-IS3082WNX			
		CA-IS3086WX		10	
		CA-IS3088WX		20	
T _A	Environmental temperature	-40		125	°C

7.4. Thermal Information

Thermal Metric		CA-IS308x	Unit
R _{θJA}	Junction-to-ambient thermal resistance	83.4	°C/W

7.5. Insulation Specifications

Parameters		Test conditions	Specifications	Unit
			W	
CLR	External Clearance ¹	Shortest terminal-to-terminal distance through air	8	mm
CPG	External Creepage ¹	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	32	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	V
	Material group	According to IEC 60664-1	I	
	IEC 60664-1 over-voltage category	Rated mains voltage ≤ 300 V _{RMS}	I-IV	
		Rated mains voltage ≤ 400 V _{RMS}	I-IV	
		Rated mains voltage ≤ 600 V _{RMS}	I-III	
DIN V VDE V 0884-11:2017-01²				
V _{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1414	V _{PK}
V _{IOWM}	Maximum operating isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test	1000	V _{RMS}
		DC voltage	1414	V _{DC}
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} , t=60 s (qualification); V _{TEST} = 1.2 × V _{IOTM} , t=1 s (100% product test)	7070	V _{PK}
V _{IOSM}	Maximum surge isolation voltage ²	Test method per IEC 60065, 1.2/50μs waveform, V _{TEST} = 1.6 × V _{IOSM} (production test)	6250	V _{PK}
Q _{pd}	Apparent charge ³	Method a, after input/output safety tests subgroup 2/3, V _{ini} = V _{IOTM} , t _{ini} = 60s; V _{pd(m)} = 1.2 × V _{IORM} , t _m = 10s	≤5	pC
		Method a, after environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60s; V _{pd(m)} = 1.6 × V _{IORM} , t _m = 10s	≤5	
		Method b1, at routine test (100% production test) and preconditioning (sample test) V _{ini} = 1.2 × V _{IOTM} , t _{ini} = 1s; V _{pd(m)} = 1.875 × V _{IORM} , t _m = 1s	≤5	
C _{IO}	Barrier capacitance, input to output ⁴	V _{IO} = 0.4 × sin (2πft), f = 1 MHz	~0.5	pF
R _{IO}	Isolation resistance , input to output ⁴	V _{IO} = 500 V, T _A = 25°C	>10 ¹²	Ω
		V _{IO} = 500 V, 100°C ≤ T _A ≤ 125°C	>10 ¹¹	
		V _{IO} = 500 V at T _S = 150°C	>10 ⁹	
	Pollution degree		2	
UL 1577				
V _{ISO}	Maximum isolation voltage	V _{TEST} = V _{ISO} , t = 60 s (certified) V _{TEST} = 1.2 × V _{ISO} , t = 1 s (100% production test)	5000	V _{RMS}
Notes:				
1. This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits. 2. Devices are immersed in oil during surge characterization. 3. The characterization charge is discharging charge (pd) caused by partial discharge. 4. Capacitance and resistance are measured with all pins on field-side and logic-side tied together.				

7.6. Safety-Related Certifications

VDE (pending)	UL	CQC	TUV
Certified according to DIN V VDE V 0884-11:2017-01	Certified according to UL 1577 Component Recognition Program	Certified according to GB4943.1-2011 and GB 8898-2011	Certified according to EN/IEC 61010-1:2010 (3rd Ed) and EN/IEC 62368-1:2014+A11:2017
	SOP16-W: 5000 V _{RMS}	Reinforced insulation 600 V _{RMS} Maximum working voltage (Altitude ≤ 5000 m)	5000 V _{RMS} reinforced insulation per EN/IEC 61010-1:2010 (3rd Ed) and EN/IEC 62368-1:2014+A11:2017, working voltage is up to 600 V _{RMS}
	Certificate number: E511334	Certificate number: CQC20001257126	CB certificate number: JPTUV-112094; DE 2-028138 AK certificate number: AK 50476734 0001; AK 50476735 0001

7.7. Electrical Characteristics
7.7.1. Driver

 All typical specs are at $V_{DDA} = 3.3V$, $V_{DDB} = 5V$, $T_A = 25^\circ C$, Min/Max specs are over recommended operating conditions unless otherwise specified.

CA-IS3082WX, CA-IS3088WX, CA-IS3082WNX:

Parameters		Test conditions	Minimum value	TYP	Maximum value	Unit
$ V_{OD1} $	Driver differential-output voltage	$V_{DDB} = 5V$	2.7	4.6	5.5	V
$ V_{OD2} $	Driver differential-output voltage	$R_L = 54\Omega$, see Figure 8-1	1.5	3.6		V
$\Delta V_{OD1} $	Change in differential output voltage between two states		-0.2		0.2	
V_{OC}	Common-mode output voltage		1	$V_{DDB}/2$	3	
ΔV_{OC}	change in steady-state common-mode output voltage between two states		-0.2		0.2	
I_{IH}, I_{IL}	Input current(DI, DE)	$V_{DI}, V_{DE} = 0V$ or V_{DDA}	-20		20	μA
I_{OS}	Short-circuit output current	$DE = V_{DDA}, V_A$ or $V_B = -7V$	-150		150	mA
		$DE = V_{DDA}, V_A$ or $V_B = 12V$				
CMTI	Common mode transient immunity	$V_{CM} = 1500V$; see Figure 8-8	100	150		kV/ μS
C_i	Input capacitance	$V_I = V_{DDA}/2 + 0.4 \times \sin(2\pi ft)$, $f = 1\text{ MHz}$, $V_{DDA} = 5\text{ V}$		4		pF

CA-IS3080WX, CA-IS3086WX:

Parameters		Test conditions	Minimum value	TYP	Maximum value	Unit
$ V_{OD1} $	Driver differential-output voltage	$V_{DDB} = 5V$	2.7	5	5.5	V
$ V_{OD2} $	Driver differential-output voltage	$R_L = 54\Omega$, see Figure 8-1	1.5	3.7		V
$\Delta V_{OD1} $	Change in differential output voltage between two states		-0.2		0.2	
V_{OC}	Common-mode output voltage		1	$V_{DDB}/2$	3	
ΔV_{OC}	change in steady-state common-mode output voltage between two states		-0.2		0.2	
I_{IH}, I_{IL}	Input current(DI, DE)	$V_{DI}, V_{DE} = 0V$ or V_{DDA}	-20		20	μA
I_{OS}	Short-circuit output current	$DE = V_{DDA}, V_Y = -7V, V_Z = 12V$	-250		250	mA
		$DE = V_{DDA}, V_Y = 12V, V_Z = -7V$				
CMTI	Common mode transient immunity	$V_{CM} = 1500V$; see Figure 8-8	100	150		kV/ μS
C_i	Input capacitance	$V_I = V_{DDA}/2 + 0.4 \times \sin(2\pi ft)$, $f = 1\text{ MHz}$, $V_{DDA} = 5\text{ V}$		4		pF

7.7.2. Receiver

 All typical specs are at $V_{DDA} = 3.3V$, $V_{DDB} = 5V$, $T_A = 25^\circ C$, Min/Max specs are over recommended operating conditions unless otherwise specified.

CA-IS3082WX, CA-IS3088WX, CA-IS3082WNX:

Parameters		Test conditions	Minimum value	Typical value	Maximum value	Unit
V_{OH}	Output voltage high level	$I_{OH} = -4mA$;	$V_{DDA}-0.4$	4.8		V
V_{OL}	Output voltage low level	$I_{OL} = 4mA$;		0.2	0.4	V
$V_{IT+(IN)}$	Positive-going input threshold voltage			-110	-50	mV
$V_{IT-(IN)}$	Negative-going input threshold voltage		-200	-140		mV
$V_{I(HYS)}$	Receiver input hysteresis			30		mV
I_I	Bus input current	V_A or $V_B = 12V$, other logic input pins are connected to 0V		75	125	μA
		V_A or $V_B = 12V$, powered down, other logic input pins are connected to 0V		80	125	
		V_A or $V_B = -7V$, other logic input pins are connected to 0V	-100	-40		
		V_A or $V_B = -7V$, powered down, other logic input pins are connected to 0V	-100	-40		
R_{ID}	Differential input resistance	Measured between A and B	96			K Ω
I_{IH}	Input current on the \overline{RE} pin	$V_{RE} = HIGH$	-20		20	μA
I_{IL}	Input current on the \overline{RE} pin	$V_{RE} = LOW$	-20		20	μA
C_D	Differential input capacitance	Input signal is $f = 1.5MHz$, $V_{pp} = 1V$ sinusoidal signals; measured between A and B		12		pF
C_I	Single-ended input capacitance	$V_I = 0.4 \times \sin(2\pi ft)$, $f = 1MHz$		18		pF

CA-IS3080WX, CA-IS3086WX:

Parameters		Test conditions	Minimum value	Typical value	Maximum value	Unit
V_{OH}	Output voltage high level	$I_{OH} = -4mA$;	$V_{DDA}-0.4$	4.8		V
V_{OL}	Output voltage low level	$I_{OL} = 4mA$;		0.2	0.4	V
$V_{IT+(IN)}$	Positive-going input threshold voltage			-100	-20	mV
$V_{IT-(IN)}$	Negative-going input threshold voltage		-200	-130		mV
$V_{I(HYS)}$	Receiver input hysteresis			30		mV
I_I	Bus input current	V_A or $V_B = 12V$, other logic input pins are connected to 0V		75	125	μA
		V_A or $V_B = 12V$, powered down, other logic input pins are connected to 0V		75	125	
		V_A or $V_B = -7V$, other logic input pins are connected to 0V	-100	-43		
		V_A or $V_B = -7V$, powered down, other logic input pins are connected to 0V	-100	-43		
R_{ID}	Differential input resistance	Measured between A and B	96			K Ω
I_{IH}	Input current on the \overline{RE} pin	$V_{RE} = HIGH$	-20		20	μA
I_{IL}	Input current on the \overline{RE} pin	$V_{RE} = LOW$	-20		20	μA
C_D	Differential input capacitance	Input signal is $f = 1.5MHz$, $V_{pp} = 1V$ sinusoidal signals; measured between A and B		17		pF
C_I	Single-ended input capacitance	$V_I = 0.4 \times \sin(2\pi ft)$, $f = 1MHz$		17		pF

7.8. Supply Current

All typical specs are at $V_{DDA} = 3.3V$, $V_{DDB} = 5V$, $T_A = 25^\circ C$, Min/Max specs are over recommended operating conditions unless otherwise specified.

Parameters		Test conditions		Minimum value	Typical value	Maximum value	Unit
I_{CCA}	Logic side supply current	$\overline{RE} = 0V$ or V_{DDA} , $DE = 0V$ or V_{DDA}	$V_{DDA} = 3.3V$			7.6	mA
			$V_{DDA} = 5V$			8	mA
I_{CCB}	Bus side supply current	$\overline{RE} = 0V$ or V_{DDA} , $DE = 0V$, No bus load				6.8	mA

7.9. Switching Characteristics

7.9.1. Driver

All typical specs are at $V_{DDA} = 3.3V$, $V_{DDB} = 5V$, $T_A = 25^\circ C$, Min/Max specs are over recommended operating conditions unless otherwise specified.

CA-IS3082WX, CA-IS3082WNX:

Parameters		Test conditions		Minimum	Typical	Maximum	Unit
t_{PLH} , t_{PHL}	Driver Propagation Delay	See Figure 8-2 and Figure 8-3			100	250	ns
t_{PWD}	Driver output skew $ t_{PLH} - t_{PHL} $			5	20	ns	
t_r	Differential output rise time			150	500	ns	
t_f	Differential output fall time			150	500	ns	
t_{PZH} , t_{PZL}	Driver enable time	See Figure 8-7			300	800	ns
t_{PHZ} , t_{PLZ}	Driver disable time			20	50	ns	

CA-IS3088WX:

Parameters		Test conditions		Minimum	Typical	Maximum	Unit
t_{PLH} , t_{PHL}	Driver Propagation Delay	See Figure 8-2 and Figure 8-3			20	50	ns
t_{PWD}	Driver output skew $ t_{PLH} - t_{PHL} $			3	12.5	ns	
t_r	Differential output rise time			5	12	ns	
t_f	Differential output fall time			5	12	ns	
t_{PZH} , t_{PZL}	Driver enable time	See Figure 8-7			15	35	ns
t_{PHZ} , t_{PLZ}	Driver disable time			15	35	ns	

CA-IS3080WX:

Parameters		Test conditions		Minimum	Typical	Maximum	Unit
t_{PLH} , t_{PHL}	Driver Propagation Delay	See Figure 8-2 and Figure 8-3			300	620	ns
t_{PWD}	Driver output skew $ t_{PLH} - t_{PHL} $			5	30	ns	
t_r	Differential output rise time			360	680	ns	
t_f	Differential output fall time			360	680	ns	
t_{PZH} , t_{PZL}	Driver enable time	See Figure 8-7			110	650	ns
t_{PHZ} , t_{PLZ}	Driver disable time			20	250	ns	

CA-IS3086WX:

Parameters		Test conditions		Minimum	Typical	Maximum	Unit
t_{PLH} , t_{PHL}	Driver Propagation Delay	See Figure 8-2 and Figure 8-3			16	48	ns
t_{PWD}	Driver output skew $ t_{PLH} - t_{PHL} $			3	12.5	ns	
t_r	Differential output rise time			3	10	ns	
t_f	Differential output fall time			3	10	ns	
t_{PZH} , t_{PZL}	Driver enable time	See Figure 8-7			30	90	ns
t_{PHZ} , t_{PLZ}	Driver disable time			25	50	ns	

7.9.2. Receiver

 All typical specs are at $V_{DDA} = 3.3V$, $V_{DDB} = 5V$, $T_A = 25^\circ C$, Min/Max specs are over recommended operating conditions unless otherwise specified.

CA-IS3082WX, CA-IS3082WNX:

Parameters	Test conditions	Minimum	Typical	Maximum	Unit
t_{PLH} , t_{PHL} Driver Propagation Delay	See Figure 8-4 and Figure 8-5		50	100	ns
t_{PWD} Driver output skew $ t_{PLH} - t_{PHL} $				12	ns
t_r Differential output rise time			2.5	4	ns
t_f Differential output fall time			2.5	4	ns
t_{PHZ} , t_{PLZ} Driver enable time	See Figure 8-6		12	25	ns
t_{PZH} , t_{PZL} Driver disable time, DE = 0V			12	25	ns

CA-IS3088WX:

Parameters	Test conditions	Minimum	Typical	Maximum	Unit
t_{PLH} , t_{PHL} Driver Propagation Delay	See Figure 8-4 and Figure 8-5		50	100	ns
t_{PWD} Driver output skew $ t_{PLH} - t_{PHL} $				8	ns
t_r Differential output rise time			2.5	4	ns
t_f Differential output fall time			2.5	4	ns
t_{PHZ} , t_{PLZ} Driver enable time	See Figure 8-6		12	25	ns
t_{PZH} , t_{PZL} Driver disable time, DE = 0V			12	25	ns

CA-IS3080WX:

Parameters	Test conditions	Minimum	Typical	Maximum	Unit	
t_{PLH} , t_{PHL} Driver Propagation Delay	See Figure 8-4 and Figure 8-5		30	120	ns	
t_{PWD} Driver output skew $ t_{PLH} - t_{PHL} $				7	25	ns
t_r Differential output rise time			2.5	4	ns	
t_f Differential output fall time			2.5	4	ns	
t_{PHZ} , t_{PLZ} Driver enable time	See Figure 8-6		20	40	ns	
t_{PZH} , t_{PZL} Driver disable time, DE = 0V			20	40	ns	

CA-IS3086WX:

Parameters	Test conditions	Minimum	Typical	Maximum	Unit	
t_{PLH} , t_{PHL} Driver Propagation Delay	See Figure 8-4 and Figure 8-5		30	120	ns	
t_{PWD} Driver output skew $ t_{PLH} - t_{PHL} $				7	25	ns
t_r Differential output rise time			2.5	4	ns	
t_f Differential output fall time			2.5	4	ns	
t_{PHZ} , t_{PLZ} Driver enable time	See Figure 8-6		20	40	ns	
t_{PZH} , t_{PZL} Driver disable time, DE = 0V			20	40	ns	

8. Parameter Measurement Information

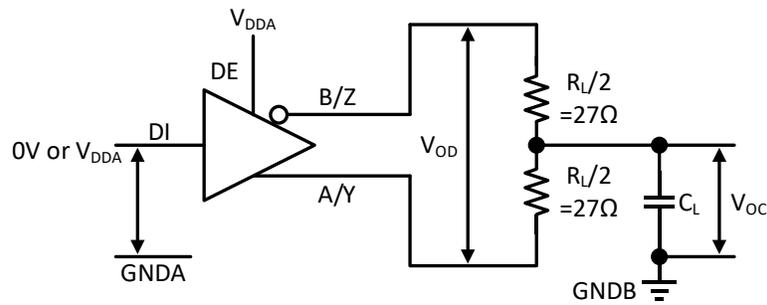


Figure 8-1 Driver DC test circuit

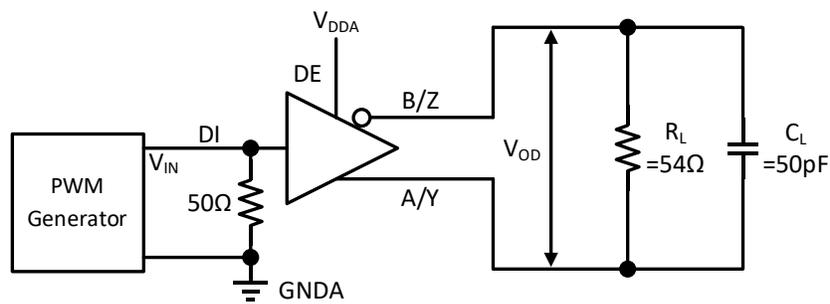


Figure 8-2 Driver propagation delays test circuit

- Note:
1. The input pulse is supplied by a generator with characteristics: PRR \leq 125 kHz, 50% duty cycle; rise time $t_r \leq$ 6 ns, fall time $t_f \leq$ 6 ns; $Z_0 = 50 \Omega$.
 2. Load capacitance CL includes external circuit (instrumentation and fixture etc.) capacitance

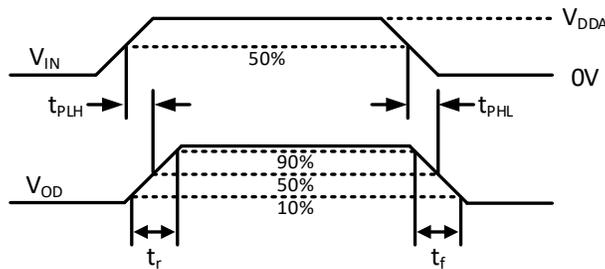


Figure 8-3 Driver propagation delays and rising/falling time

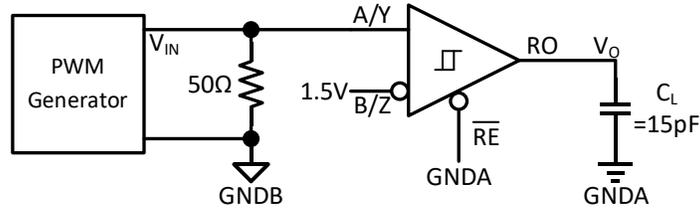


Figure 8-4 Receiver propagation delays test circuit

- Note:
1. The input pulse is supplied by a generator with characteristics: PRR \leq 125 kHz, 50% duty cycle; rise time $t_r \leq$ 6 ns, fall time $t_f \leq$ 6 ns; $Z_0 = 50 \Omega$.
 2. Load capacitance C_L includes external circuit (instrumentation and fixture etc.) capacitance

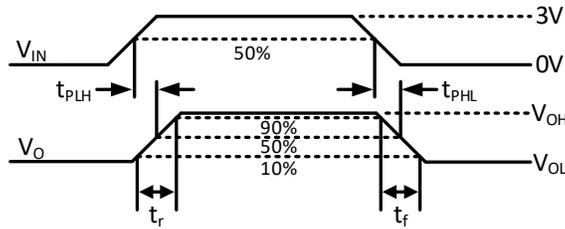


Figure 8-5 Receiver propagation delays and rising/falling time

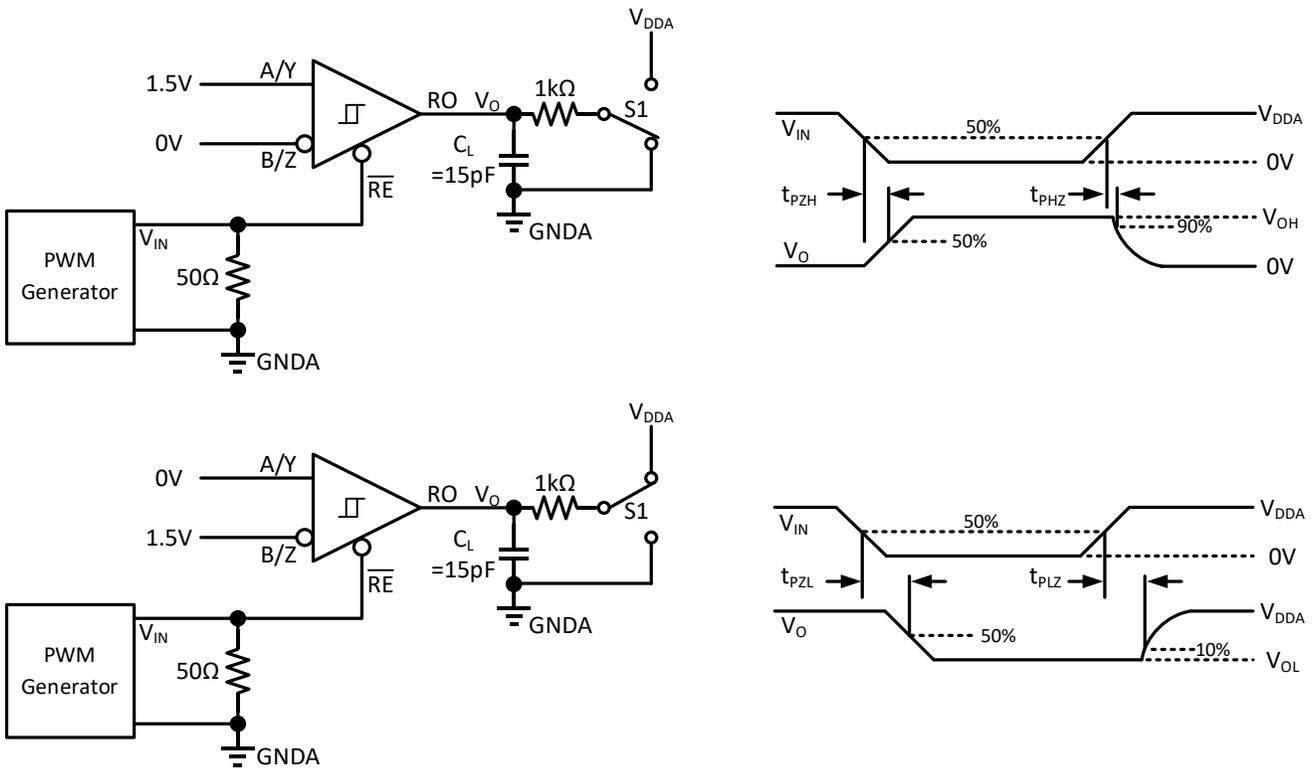


Figure 8-6 Receiver enable and disable timing

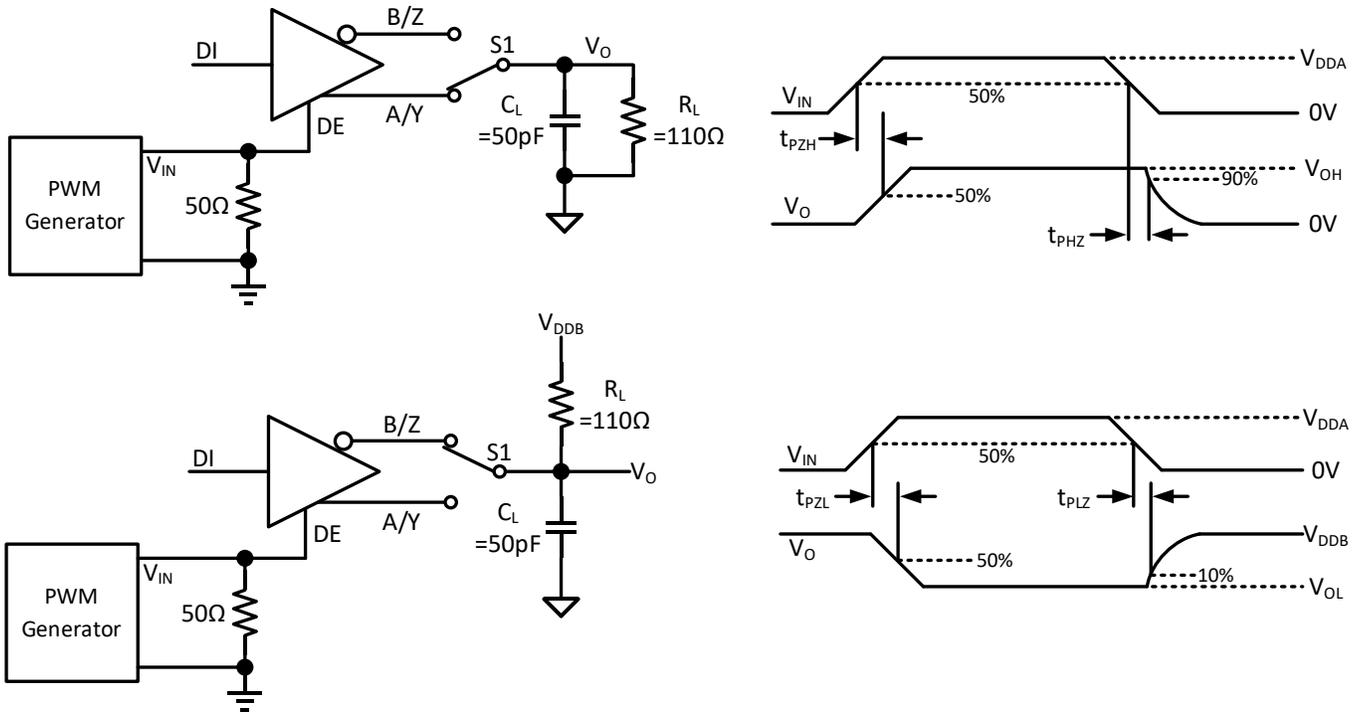


Figure 8-7 Driver enable and disable timing

Note:

1. The input pulse is supplied by a generator with characteristics: PRR \leq 125 kHz, 50% duty cycle; rise time $t_r \leq$ 6 ns, fall time $t_f \leq$ 6 ns; $Z_0 = 50 \Omega$.
2. Load capacitance C_L includes external circuit (instrumentation and fixture etc.) capacitance

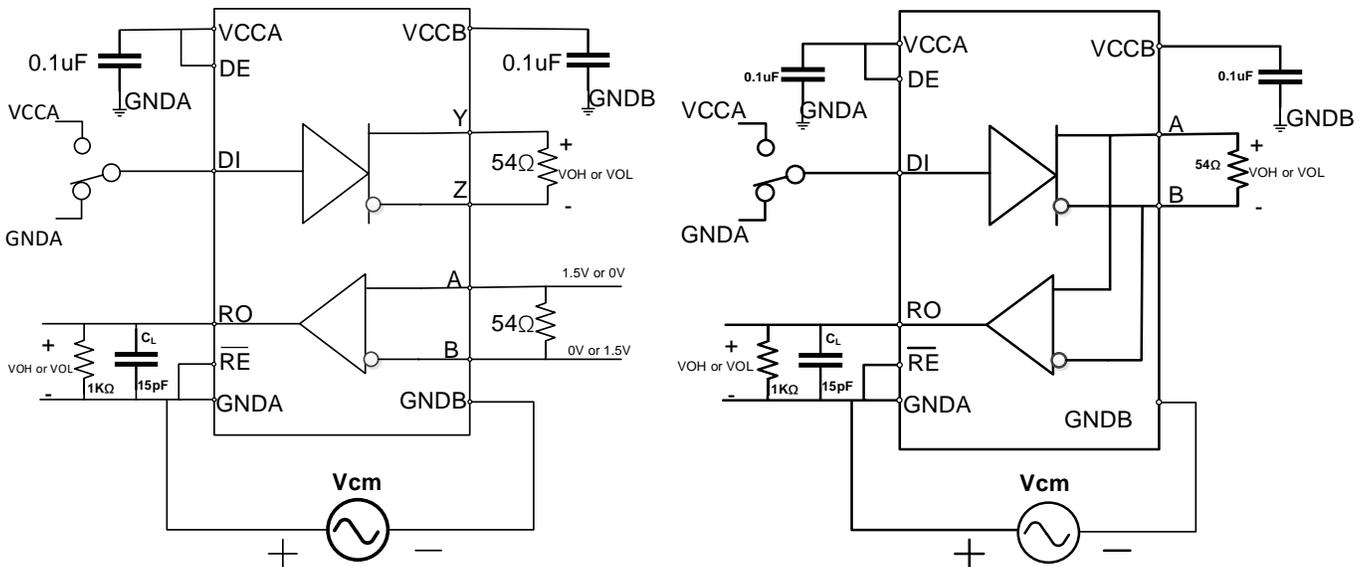


Figure 8-8 Common Mode Transient Immunity (CMTI) test for the full-duplex (left) and half-duplex (right)

9. Detailed Description

The CA-IS308x isolated RS485/RS422 transceivers provide up to $5kV_{RMS}$ of galvanic isolation between the cable side (bus-side) of the transceiver and the controller side (logic-side). These devices feature up to $150\text{ kV}/\mu\text{s}$ common mode transient immunity, allow up to 20Mbps (CA-IS3088)、10Mbps (CA-IS3086) or 0.5Mbps (CA-IS3080/82) communication across an isolation barrier. Robust isolation coupled with extended ESD protection and increased speeds enables efficient communication in noisy environments, making them ideal for communication between logic-side and bus-side in a wide range of applications, such as motor drives, PLC communication modules, telecom rectifiers, elevators, HVACs etc. applications. Two mechanisms against excessive power dissipation caused by faults or bus contention. The first, a current limit on the output stage, provides immediate protection against short circuits over the entire common-mode voltage range. The second, a thermal shutdown circuit, forces the driver outputs into a high-impedance state. The CA-IS3080WX and CA-IS3086WX provide full-duplex transceivers, while CA-IS3082WX, CA-IS3082WNX, and CA-IS3088WX provide half-duplex transceivers for RS-485 communication.

9.1. Logic Input

The CA-IS308x devices include three logic inputs on the logic side: receiver enable, driver enable and driver digital input. The transmitter enable pin DE has an internal weak pull-down to GNDA; while the digital input DI and receiver enable \overline{RE} pins have an internal pull-up to V_{DDA} . All devices use $1.5M\Omega$ pull-up or pull-down resistor for the logic inputs, see Figure 9 for the inputs equivalent circuit of the CA-IS308x series.

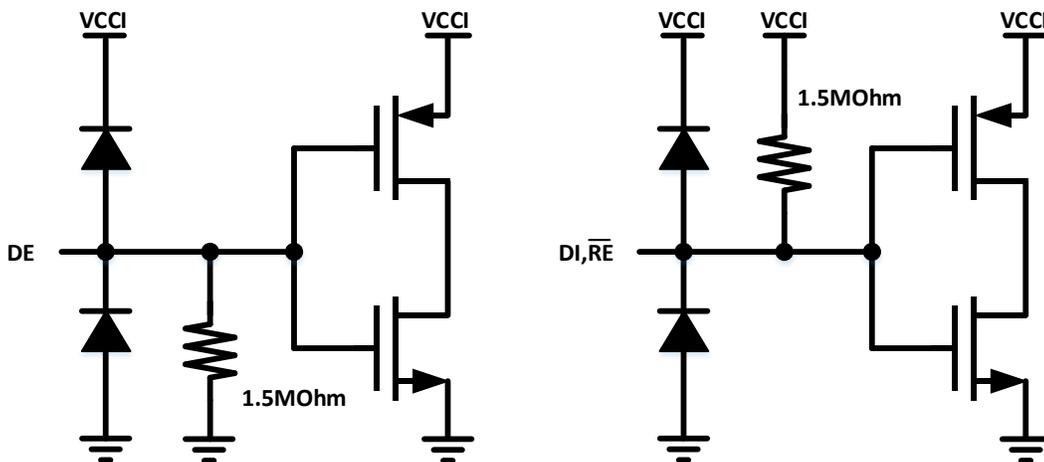


Figure 9-1 Logic input equivalent circuit

9.2. Receiver

The receiver reads the differential input from the bus line (Y/A and Z/B) and transfers this data as a single-ended, logic-level output RO to the controller. Driver the enable input \overline{RE} low to enable the receiver. Driver \overline{RE} logic high to disable the receiver. The truth table of receiver of CA-IS308x is shown below *Table 9-1*.

In case the receiver has been enabled, if the differential input voltage $V_{ID} = V_A - V_B$ is higher than or equal to the threshold voltage $V_{TH+(IN)}$, the RO pin output high level. Conversely, if the differential input voltage $V_{ID} = V_A - V_B$ is lower than the threshold voltage $V_{TH-(IN)}$, the RO pin output high level. if the differential input voltage V_{ID} is between $V_{TH-(IN)}$ and $V_{TH+(IN)}$, the RO pin output Indeterminate level.

In case the receiver has been disabled, the RO pin output high impedance. The receiver will disable when the \overline{RE} pin is floating why the internal \overline{RE} pin is weak pull-up to V_{DDA} .

Fail-safe feature is used to keep the receiver's output in a defined state when the receiver is not connected to the cable, the cable has an open or the cable has a short.

Table 9-1 CA-IS308x Receiver Truth Table

VDDA	VDDB	DIFFERENTIAL INPUT	ENABLE	OUTPUT
		$(V_A - V_B)$	(\overline{RE})	(RO)
Powered up	Powered up	$V_{TH+(IN)} \leq V_A - V_B$	L	H
Powered up	Powered up	$V_{TH-(IN)} < V_A - V_B < V_{TH+(IN)}$	L	Indeterminate
Powered up	Powered up	$V_A - V_B \leq V_{TH-(IN)}$	L	L
Powered up	Powered up	X	H	Hi-Z
Powered up	Powered up	X	open	Hi-Z
Powered up	Powered up	Open/Short/Idle	L	H
Powered down	Powered up	X	X	Hi-Z
Powered up	Powered down	X	L	H

Notes:

1. X = don't care; H = high level; L = low level; Hi-Z = high impedance.
2. \overline{RE} has an internal weak pull-up to V_{DDA} .

9.3. Driver

The transmitter converts a single-ended input signal (DI) from the local controller to differential outputs for the bus lines Y/A and Z/B. The truth table for the transmitter is provided in *Table 9-2*. The driver outputs and receiver inputs are protected from $\pm 8\text{kV}$ electrostatic discharge (ESD) to GNDB on the cable side, as specified by the Human Body Model (HBM). The driver outputs also feature current limiting protection and thermal shutdown. The DE pin of driver has an internal weak pull-down to GNDA, the driver is inhibited when the DE pin is floating. The DI pin of driver has an internal weak pull-up for CA-IS308x, When the driver DE pin is enabled, if the DI is floating, the driver output high level.

Table 9-2 CA-IS308x Transmitter Truth Table

VDDA	VDDB	INPUT	ENABLE INPUT	OUTPUTS	
		(DI)	(DE)	Y / A	Z / B
Powered up	Powered up	H	H	H	L
Powered up	Powered up	L	H	L	H
Powered up	Powered up	X	L	Hi-Z	Hi-Z
Powered up	Powered up	X	OPEN	Hi-Z	Hi-Z
Powered up	Powered up	OPEN	H	H	L
Powered down	Powered up	X	X	Hi-Z	Hi-Z
Powered up	Powered down	X	X	Hi-Z	Hi-Z
Powered down	Powered down	X	X	Hi-Z	Hi-Z

Notes:

1. X = don't care; H = high level; L = low level; Hi-Z = high impedance.
2. DE has an internal weak pull-down to V_{DDA} , DI has an internal weak pull-up to V_{DDA} .

9.4. Protection Functions

9.4.1. Signal Isolation

The CA-IS308x devices integrated digital galvanic isolators using Chipanalog's capacitive isolation technology based on the ON-OFF keying (OOK) modulation scheme, allow data transmission between the controller side and cable side of the transceiver with different power domains.

9.4.2. Thermal Shutdown

If the junction temperature of the CA-IS308x device exceeds the thermal shutdown threshold $T_{J(\text{shutdown})}$ (160°C, typ.), the driver outputs go high-impedance state. The shutdown condition is cleared when the junction temperature drops to normal operation temperature range of the device.

9.4.3. Current-Limit

The CA-IS308x protect the transmitter output stage against a short-circuit to a positive or negative voltage over the common mode voltage range of -7V to +12V(CA-IS3082/88) and -15V to +15V(CA-IS3080/86) by limiting the driver current. However, this will cause large supply current and dissipation. Thermal shutdown further protects the devices from excessive temperatures that may result from a short circuit. The transmitter returns to normal operation once the short is removed.

10. Applications Information

CA-IS308x family consists of half-duplex and full-duplex RS-485 transceivers commonly used for asynchronous data transmissions. For half-duplex devices, the driver and receiver enable pins allow for the configuration of different operating modes to avoid conflicts of bus line. Full-duplex implementation requires two signal pairs (four wires), and allows each node to transmit data on one pair while simultaneously receiving data on the other pair. When the number of nodes is greater than 2, user carefully need to control the enable function of driver to avoid conflicts of bus line also.

10.1. Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. As seen in the following typical network application circuit, *Figure 10-1* show typical network application circuits for the full-duplex RS422 transceivers. The driver of Master be able to send data to multiple slaves, which can receive data from slaves at the same time. *Figure 10-2* show typical network application circuits for the half-duplex RS485 transceivers. Contrast to full-duplex transceivers, which can reduce a pair of cables.

The maximum recommended data rate in the RS-485/RS422 network is 10Mbps, which can be achieved at a maximum cable length of 40ft (12m). The absolute maximum distance is 4000ft (1.2km) of cable, at which point, data rate is limited to 100kbps. These were the specifications made in the original standard, new RS-485 transceivers and cables are pushing the limit of RS-485 far beyond its original definitions. However, the maximum data rate is still limited by the bus loading, number of nodes, cable length etc. factors. For RS485 network design, margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum data rate, number of nodes often lower. To minimize reflections, terminate the line at both ends with a termination resistor (120Ω in the typical application circuits), whose value matches the characteristic impedance (Z_0) of the cable, and keep stub lengths off the main line as short as possible. The termination resistors should always be placed at the far ends of the cable. As a general rule moreover, termination resistors should be placed at both far ends of the cable. This method, known as parallel termination, generally allows for higher data rates over longer cable length.

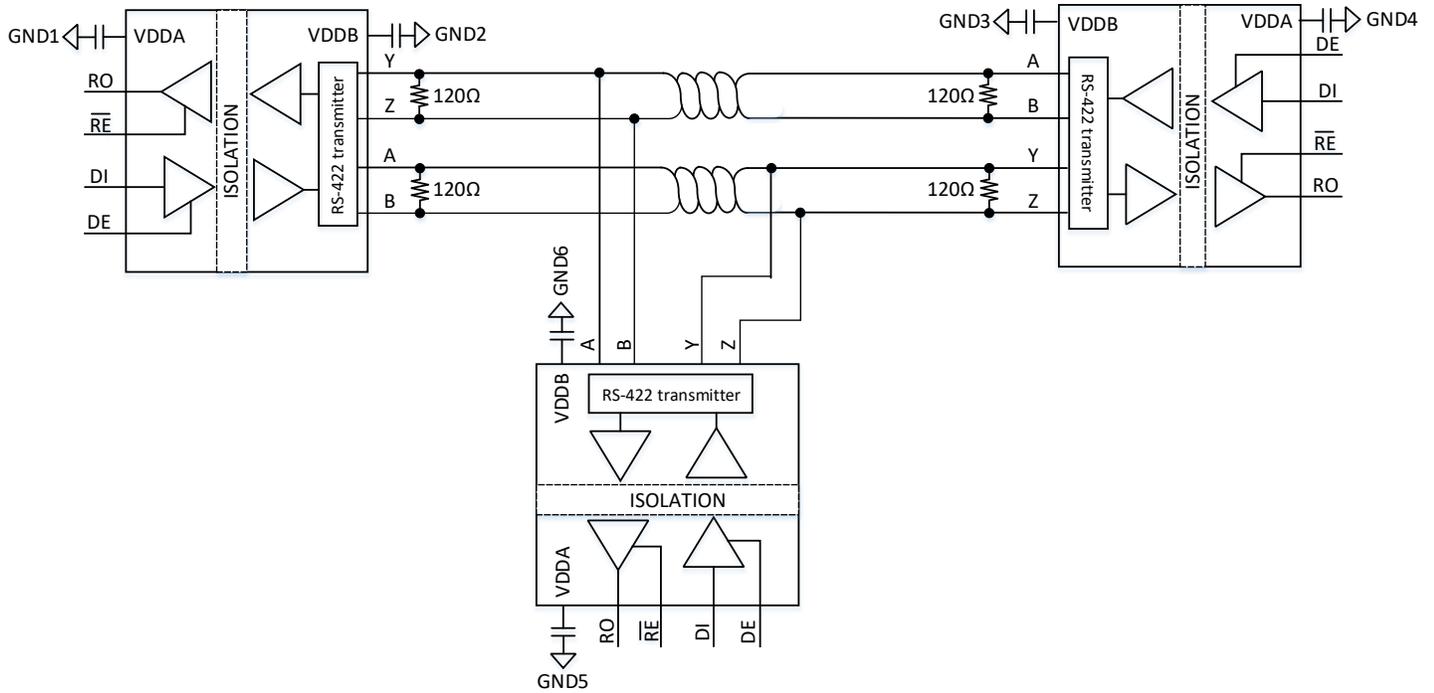


Figure 10-1 Typical isolated full-duplex RS422 application circuit

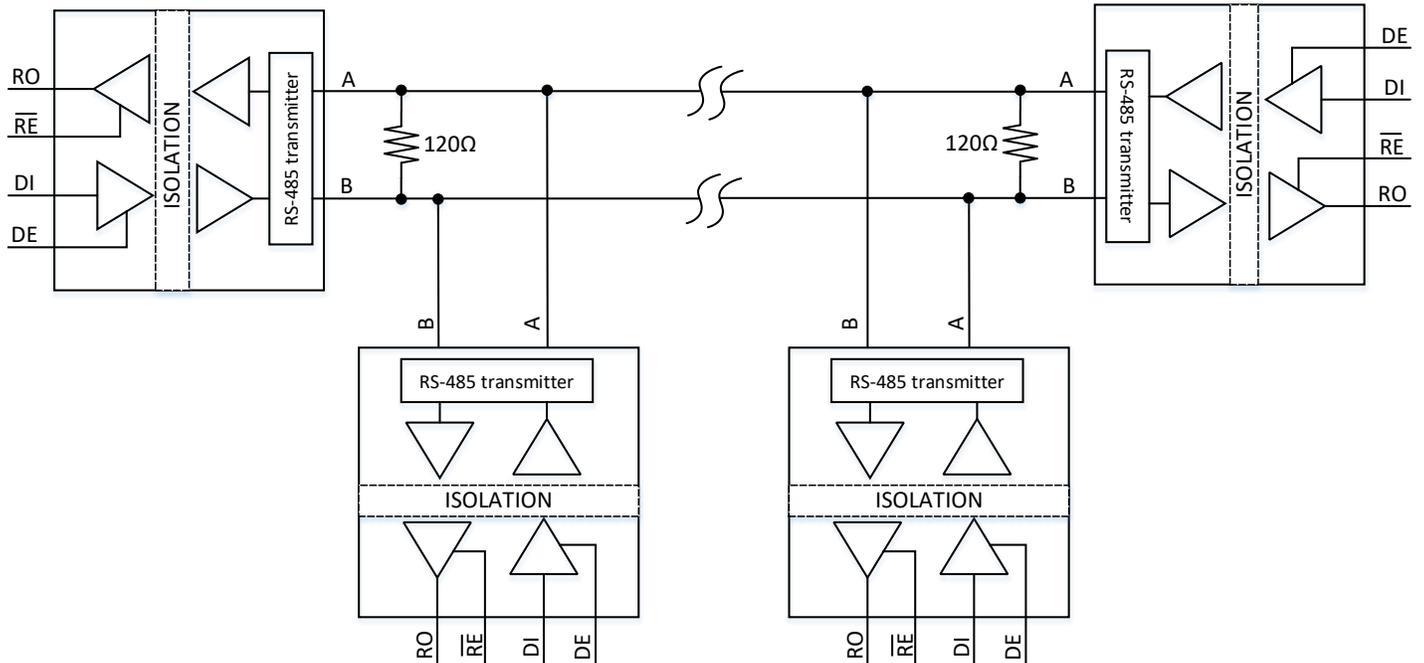


Figure 10-2 Typical isolated half-duplex RS485 application circuit

10.2. 256 transceivers on the bus

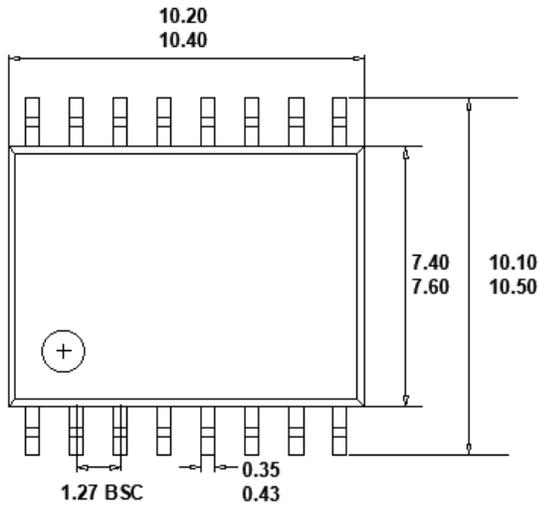
The maximum number of transceivers and receivers allowed depends on how much each device loads down the system. All devices connected to an RS-485 network should be characterized in regard to multiples or fractions of unit loads. The maximum number of unit loads allowed one twisted pair, assuming a properly terminated cable with a characteristic impedance of 120Ω or more, is 32 (375Ω). The CA-IS308x transceivers have a 1/8-unit load ($96k\Omega$) receiver, which allows up to 256 transceivers, connected in parallel, on one communication line.

10.3. PCB Layout

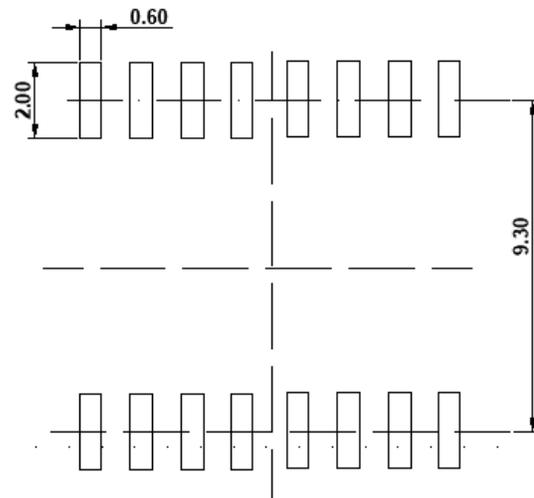
It is recommended to design an isolation channel underneath the isolator that is free from ground and signal planes. Any galvanic or metallic connection between the cable side and logic side will defeat the isolation. To make sure device operation is reliable at all data rates and supply voltages, the decoupling capacitors between VDDA and GNDA and between VDDB and GNDB are recommended. The capacitors should be located as close as possible to the IC to minimize inductance.

11. Package Information

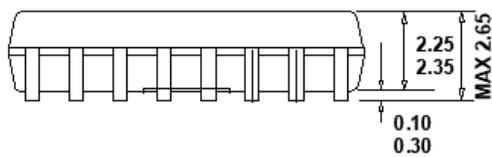
The following diagrams illustrate the dimension diagram of CA-IS308x series digital isolators packaged in SOIC16-WB wide package and the suggested pad dimension diagram, wherein dimensions are in millimeters.



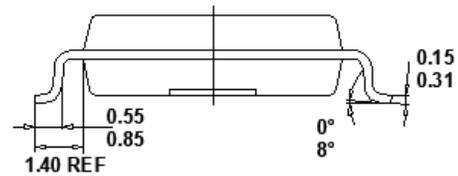
TOP VIEW



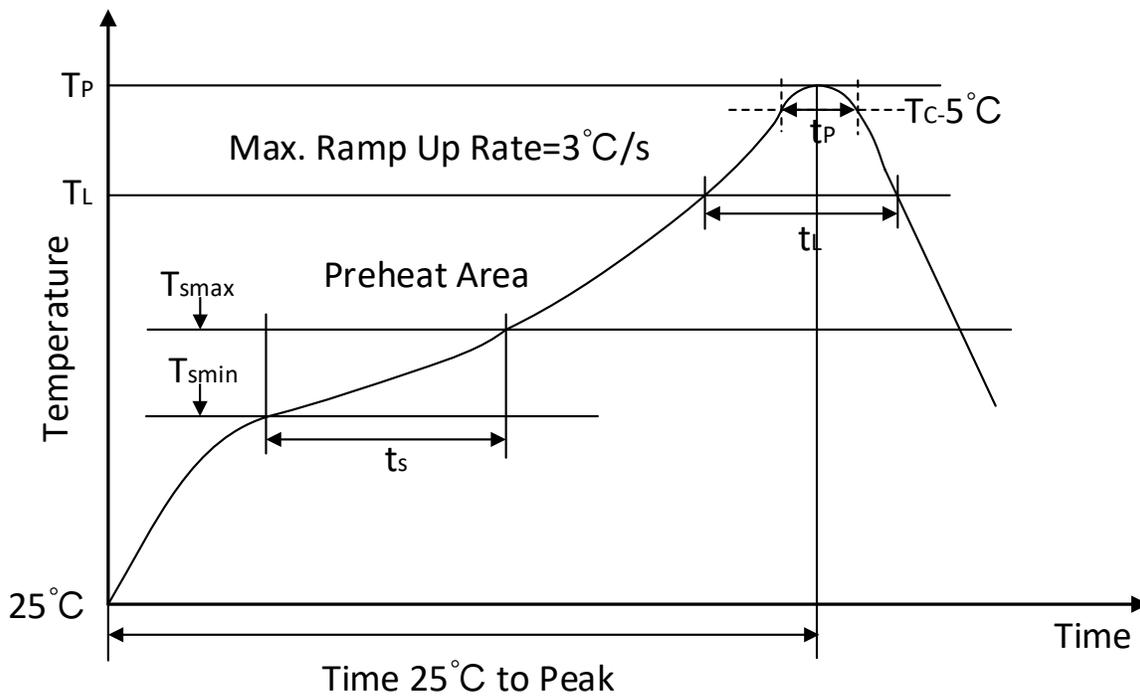
RECOMMENDED LAND PATTERN



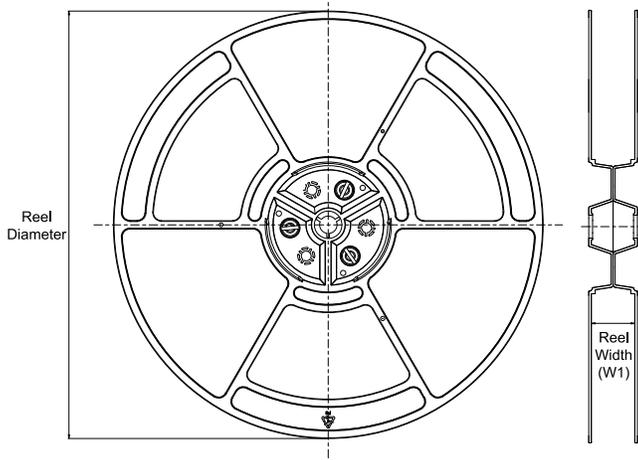
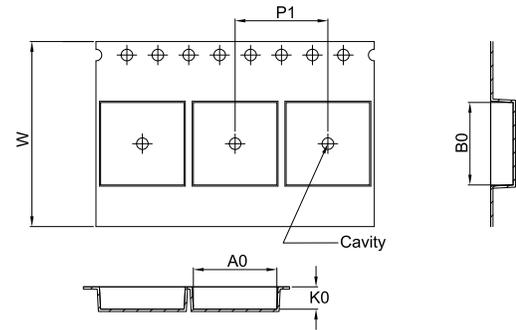
FRONT VIEW



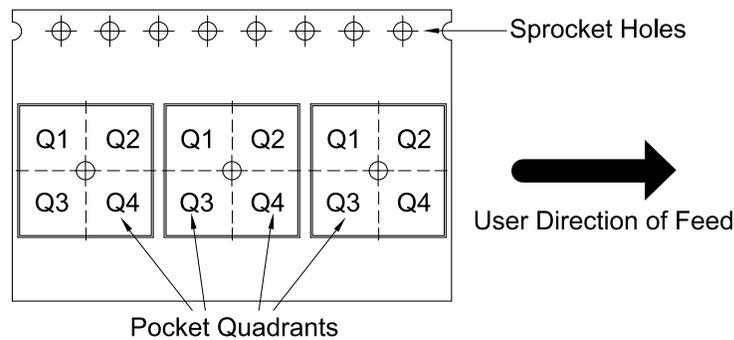
LEFT SIDE VIEW

12. Soldering Temperature (reflow) Profile

Figure. 12-1 Soldering Temperature (reflow) Profile
Table. 12-1 Soldering Temperature Parameter

Profile Feature	Pb-Free Assembly
Average ramp-up rate(217 °C to Peak)	3°C/second max
Time of Preheat temp(from 150 °C to 200 °C)	60-120 second
Time to be maintained above 217 °C	60-150 second
Peak temperature	260 +5/-0 °C
Time within 5 °C of actual peak temp	30 second
Ramp-down rate	6 °C/second max.
Time from 25 °C to peak temp	8 minutes max

13. Tape and Reel Information
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3080WX	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3086WX	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3082WX	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3082W NX	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3088WX	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1

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