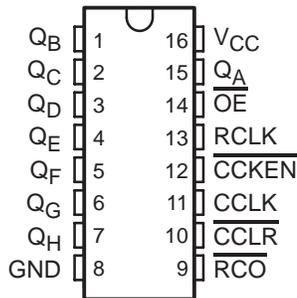


# SN54HC590A, SN74HC590A 8-BIT BINARY COUNTERS WITH 3-STATE OUTPUT REGISTERS

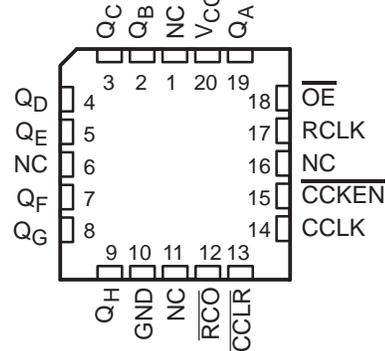
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- 2-V to 6-V  $V_{CC}$  Operation
- High-Current 3-State Parallel Register Outputs Can Drive Up To 15 LSTTL Loads
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 14$  ns
- $\pm 6$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max
- 8-Bit Counter With Register
- Counter Has Direct Clear

SN54HC590A . . . J OR W PACKAGE  
SN74HC590A . . . D, DW, OR N PACKAGE  
(TOP VIEW)



SN54HC590A . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

The 'HC590A devices contain an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register. The binary counter features direct clear ( $\overline{CCLR}$ ) and count-enable ( $\overline{CCKEN}$ ) inputs. A ripple-carry output ( $\overline{RCO}$ ) is provided for cascading. Expansion is accomplished easily for two stages by connecting  $\overline{RCO}$  of the first stage to  $\overline{CCKEN}$  of the second stage. Cascading for larger count chains can be accomplished by connecting  $\overline{RCO}$  of each stage to the counter clock (CCLK) input of the following stage.

CCLK and the register clock (RCLK) inputs are positive-edge triggered. If both clocks are connected together, the counter state always is one count ahead of the register. Internal circuitry prevents clocking from the clock enable.

## ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 25	SN74HC590AN	SN74HC590AN
	SOIC – D	Tube of 40	SN74HC590AD	HC590A
		Reel of 2500	SN74HC590ADR	
		Reel of 250	SN74HC590ADT	
	SOIC – DW	Tube of 40	SN74HC590ADW	HC590A
Reel of 2000		SN74HC590ADWR		
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC590AJ	SNJ54HC590AJ
	CFP – W	Tube of 150	SNJ54HC590AW	SNJ54HC590AW
	LCCC - FK	Tube of 55	SNJ54HC590AFK	SNJ54HC590AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

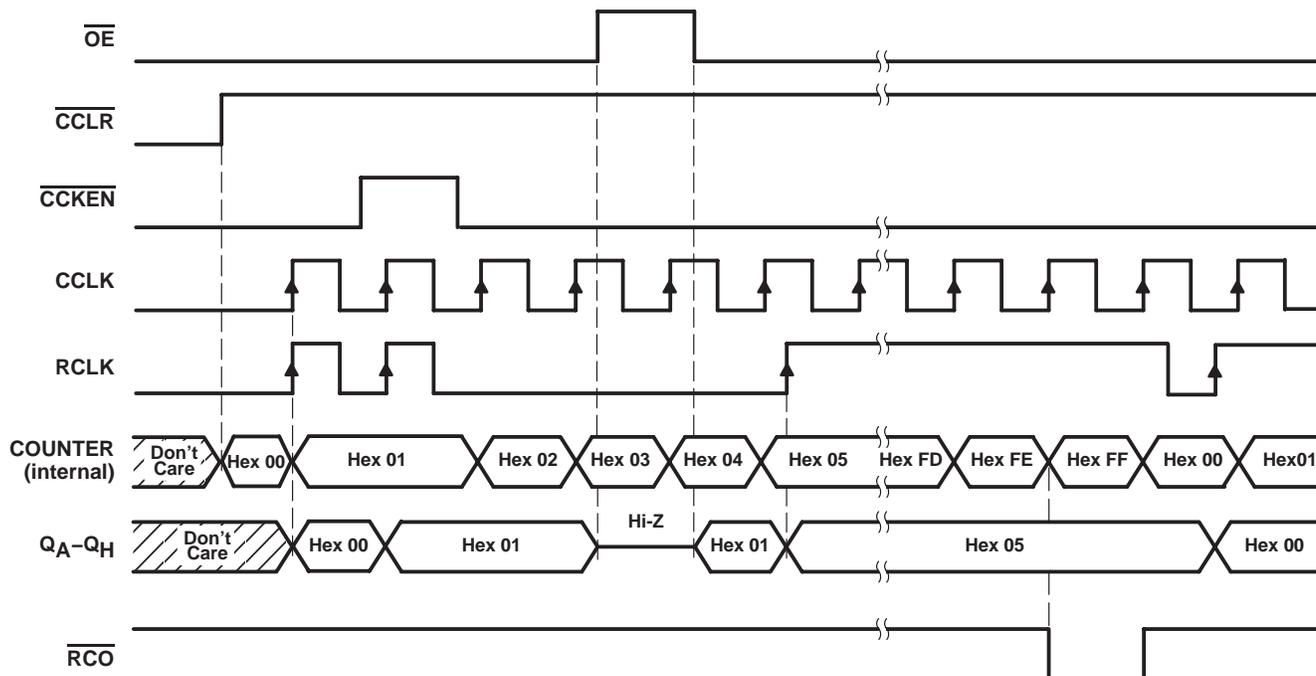
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN54HC590A, SN74HC590A 8-BIT BINARY COUNTERS WITH 3-STATE OUTPUT REGISTERS

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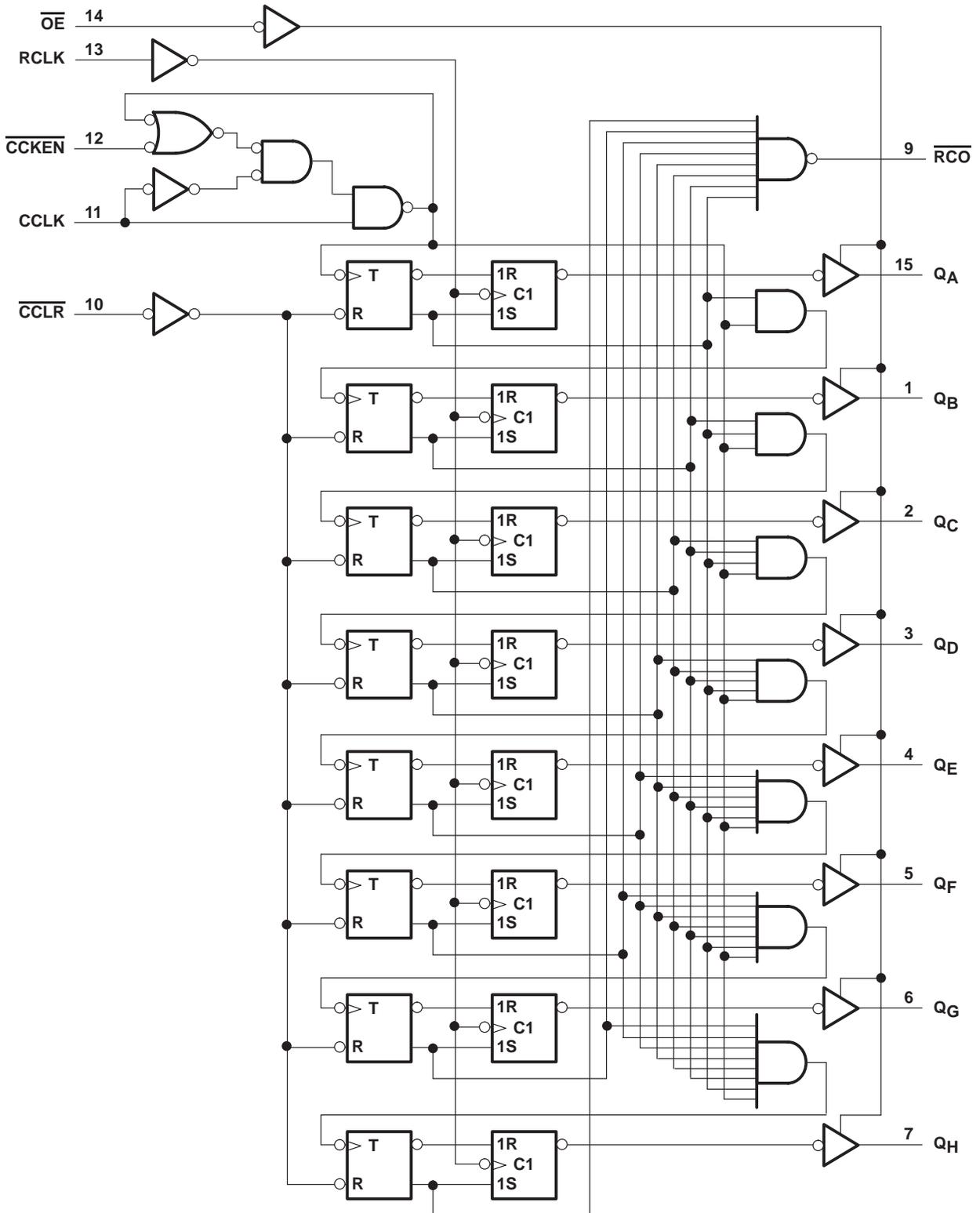
## timing diagram



### TIMING SEQUENCE

1. Clear Counter (asynchronous).
2. Count up: 0x01. Store 0x00 in register.
3. Inhibit counter clock (CCKEN = HIGH). Store 0x01 in register.
4. Count 0x02, 0x03.
5. 3-state the outputs.
6. Count up: 0x04
7. Enable outputs.
8. Continue up: 0x05
9. Store 0x05 in register.
10. Continue counting: 0x06...0xFD, 0xFE, 0xFF, 0x00, etc.
11. Store 0x00 in register.

**logic diagram (positive logic)**



Pin numbers shown are for the D, DW, J, N, and W packages.



**SN54HC590A, SN74HC590A**  
**8-BIT BINARY COUNTERS**  
**WITH 3-STATE OUTPUT REGISTERS**  
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC590A		SN74HC590A		UNIT	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2 V	1.9	1.998		1.9		1.9	V	
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		4.5 V	$\overline{RCO}$ , I <sub>OH</sub> = -4 mA	3.98	4.3		3.7		3.84		
			Q <sub>A</sub> -Q <sub>H</sub> , I <sub>OH</sub> = -6 mA	3.98	4.3		3.7		3.84		
			$\overline{RCO}$ , I <sub>OH</sub> = -5.2 mA	5.48	5.8		5.2		5.34		
6 V	Q <sub>A</sub> -Q <sub>H</sub> , I <sub>OH</sub> = -7.8 mA	5.48	5.8		5.2		5.34				
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2 V		0.002	0.1		0.1		V	
			4.5 V		0.001	0.1		0.1			0.1
			6 V		0.001	0.1		0.1			0.1
		4.5 V	$\overline{RCO}$ , I <sub>OL</sub> = 4 mA		0.17	0.26		0.4			0.33
			Q <sub>A</sub> -Q <sub>H</sub> , I <sub>OL</sub> = 6 mA		0.17	0.26		0.4			0.33
			$\overline{RCO}$ , I <sub>OL</sub> = 5.2 mA		0.15	0.26		0.4			0.33
6 V	Q <sub>A</sub> -Q <sub>H</sub> , I <sub>OL</sub> = 7.8 mA		0.15	0.26		0.4		0.33			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0	6 V		±0.1	±100		±1000		±1000	nA	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or 0	6 V		±0.01	±0.5		±10		±5	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0	6 V			8		160		80	μA	
C <sub>i</sub>		2 V to 6 V		3	10		10		10	pF	

**SN54HC590A, SN74HC590A**  
**8-BIT BINARY COUNTERS**  
**WITH 3-STATE OUTPUT REGISTERS**

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HC590A		SN74HC590A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	2 V	4		2.5		3.2		MHz
		4.5 V	20		13		16		
		6 V	24		16		19		
t <sub>w</sub>	CCLK or RCLK high or low	2 V	125		200		155		ns
		4.5 V	25		38		31		
		6 V	21		32		26		
	CCLR low	2 V	100		150		125		
		4.5 V	20		30		25		
		6 V	17		26		21		
t <sub>su</sub>	CCKEN low before CCLK↑	2 V	100		150		125		ns
		4.5 V	20		30		25		
		6 V	17		26		21		
	CCLR high (inactive) before CCLK↑	2 V	100		150		125		
		4.5 V	20		30		25		
		6 V	17		26		21		
	CCLK↑ before RCLK↑†	2 V	100		150		125		
		4.5 V	20		30		25		
		6 V	17		26		21		
t <sub>h</sub>	CCKEN low after CCLK↑	2 V	50		75		60		ns
		4.5 V	10		15		12		
		6 V	9		13		11		

† This setup time ensures that the register gets stable data from the counter outputs. The clocks may be tied together, in which case the register is one clock pulse behind the counter.

**SN54HC590A, SN74HC590A**  
**8-BIT BINARY COUNTERS**  
**WITH 3-STATE OUTPUT REGISTERS**  
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switching characteristics over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	SN54HC590A				UNIT	
				$T_A = 25^\circ\text{C}$			MIN		MAX
				MIN	TYP	MAX			
$f_{\text{max}}$			2 V	4	8	2.5	MHz		
			4.5 V	20	35	13			
			6 V	24	40	16			
$t_{\text{pd}}$	CCLK $\uparrow$	$\overline{\text{RCO}}$	2 V	80	150	225	ns		
			4.5 V	20	31	45			
			6 V	15	26	38			
$t_{\text{PLH}}$	$\overline{\text{CCLR}}\downarrow$	$\overline{\text{RCO}}$	2 V	70	130	195	ns		
			4.5 V	18	28	39			
			6 V	14	23	33			
$t_{\text{pd}}$	RCLK $\uparrow$	Q	2 V	70	140	210	ns		
			4.5 V	18	31	42			
			6 V	14	25	36			
$t_{\text{en}}$	$\overline{\text{OE}}\downarrow$	Q	2 V	80	125	185	ns		
			4.5 V	20	30	37			
			6 V	15	28	31			
$t_{\text{dis}}$	$\overline{\text{OE}}\uparrow$	Q	2 V	80	125	185	ns		
			4.5 V	20	30	37			
			6 V	15	28	31			
$t_t^*$		$\overline{\text{RCO}}$	2 V	38	75	110	ns		
			4.5 V	8	15	22			
			6 V	6	13	19			
		Q	2 V	38	60	90			
			4.5 V	8	12	18			
			6 V	6	10	15			

\* This parameter is not production tested for the SN54HC590A.

**SN54HC590A, SN74HC590A**  
**8-BIT BINARY COUNTERS**  
**WITH 3-STATE OUTPUT REGISTERS**

SCLS039F – DECEMBER 1982 – REVISED SEPTEMBER 2003

switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	SN74HC590A				UNIT	
				T <sub>A</sub> = 25°C			MIN		MAX
				MIN	TYP	MAX			
f <sub>max</sub>			2 V	4	8	3.2	MHz		
			4.5 V	20	35	16			
			6 V	24	40	19			
t <sub>pd</sub>	CCLK↑	$\overline{RCO}$	2 V		80	150	190	ns	
			4.5 V		20	30	38		
			6 V		15	26	33		
t <sub>PLH</sub>	$\overline{CCLR}$ ↓	$\overline{RCO}$	2 V		70	130	165	ns	
			4.5 V		18	26	33		
			6 V		14	22	28		
t <sub>pd</sub>	RCLK↑	Q	2 V		70	140	175	ns	
			4.5 V		18	28	35		
			6 V		14	24	30		
t <sub>en</sub>	$\overline{OE}$ ↓	Q	2 V		80	125	155	ns	
			4.5 V		20	25	31		
			6 V		15	21	26		
t <sub>dis</sub>	$\overline{OE}$ ↑	Q	2 V		80	125	155	ns	
			4.5 V		20	25	31		
			6 V		15	21	26		
t <sub>t</sub>		$\overline{RCO}$	2 V		38	75	95	ns	
			4.5 V		8	15	19		
			6 V		6	13	16		
		Q	2 V		38	60	75		
			4.5 V		8	12	15		
			6 V		6	10	13		

**SN54HC590A, SN74HC590A**  
**8-BIT BINARY COUNTERS**  
**WITH 3-STATE OUTPUT REGISTERS**  
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switching characteristics over recommended operating free-air temperature range,  $C_L = 150 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	SN54HC590A				UNIT	
				$T_A = 25^\circ\text{C}$			MIN		MAX
				MIN	TYP	MAX			
$t_{pd}$	RCLK $\uparrow$	Q	2 V	100	300	447	ns		
			4.5 V	24	60	90			
			6 V	20	51	77			
$t_{en}$	$\overline{OE}$	Q	2 V	90	200	300	ns		
			4.5 V	23	40	60			
			6 V	19	34	51			
$t_t^*$		Q	2 V	45	210	315	ns		
			4.5 V	17	42	63			
			6 V	13	36	53			

\* This parameter is not production tested for the SN54HC590A.

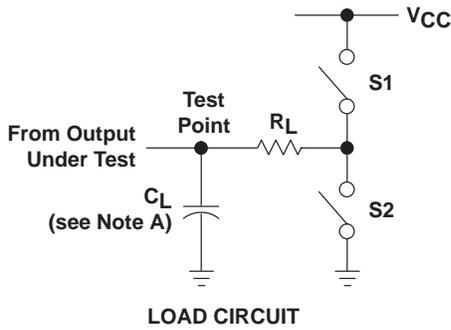
switching characteristics over recommended operating free-air temperature range,  $C_L = 150 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	SN74HC590A				UNIT	
				$T_A = 25^\circ\text{C}$			MIN		MAX
				MIN	TYP	MAX			
$t_{pd}$	RCLK $\uparrow$	Q	2 V	100	300	380	ns		
			4.5 V	24	60	76			
			6 V	20	51	65			
$t_{en}$	$\overline{OE}$	Q	2 V	90	200	250	ns		
			4.5 V	23	40	50			
			6 V	19	34	43			
$t_t$		Q	2 V	45	210	265	ns		
			4.5 V	17	42	53			
			6 V	13	36	45			

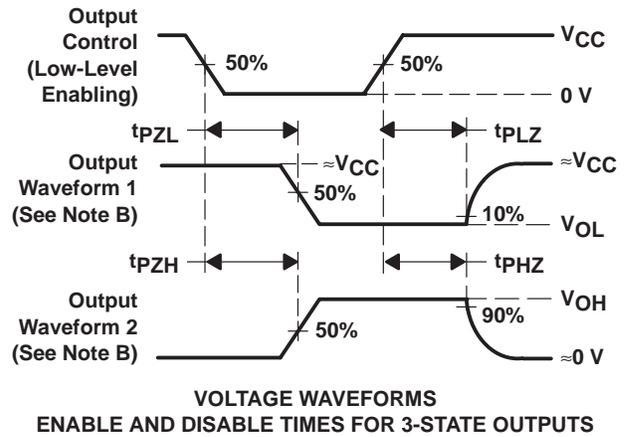
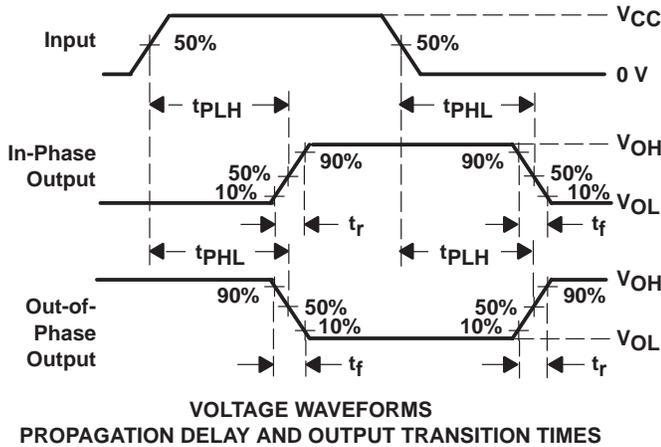
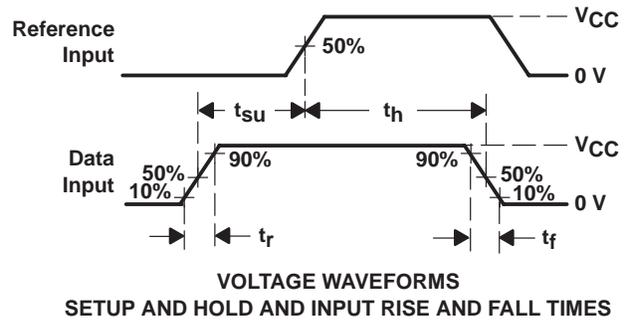
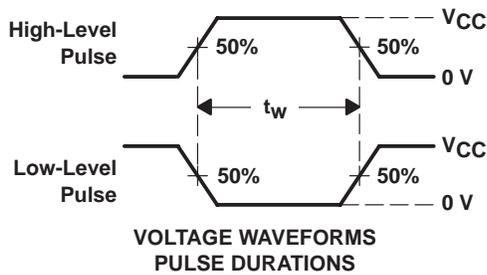
operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load	250	pF

**PARAMETER MEASUREMENT INFORMATION**



PARAMETER	$R_L$	$C_L$	S1	S2
$t_{en}$	1 k $\Omega$	50 pF or 150 pF	Open	Closed
			Closed	Open
$t_{dis}$	1 k $\Omega$	50 pF	Open	Closed
			Closed	Open
$t_{pd}$ or $t_t$	--	50 pF or 150 pF	Open	Open



- NOTES: A.  $C_L$  includes probe and test-fixture capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .  
 D. The outputs are measured one at a time with one input transition per measurement.  
 E.  $t_{PZL}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-89603012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 89603012A SNJ54HC 590AFK	<a href="#">Samples</a>
5962-8960301EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8960301EA SNJ54HC590AJ	<a href="#">Samples</a>
5962-8960301FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8960301FA SNJ54HC590AW	<a href="#">Samples</a>
SN54HC590AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54HC590AJ	<a href="#">Samples</a>
SN74HC590AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC590A	<a href="#">Samples</a>
SN74HC590ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC590A	<a href="#">Samples</a>
SN74HC590ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC590A	<a href="#">Samples</a>
SN74HC590ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC590A	<a href="#">Samples</a>
SN74HC590ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC590A	<a href="#">Samples</a>
SN74HC590ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC590A	<a href="#">Samples</a>
SN74HC590ADT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC590A	<a href="#">Samples</a>
SN74HC590ADW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC590A	<a href="#">Samples</a>
SN74HC590ADWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC590A	<a href="#">Samples</a>
SN74HC590ADWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC590A	<a href="#">Samples</a>
SN74HC590AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC590AN	<a href="#">Samples</a>
SN74HC590ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC590AN	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54HC590AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-89603012A SNJ54HC 590AFK	
SNJ54HC590AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8960301EA SNJ54HC590AJ	
SNJ54HC590AW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8960301FA SNJ54HC590AW	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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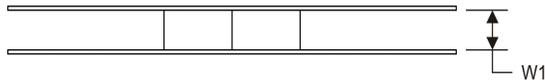
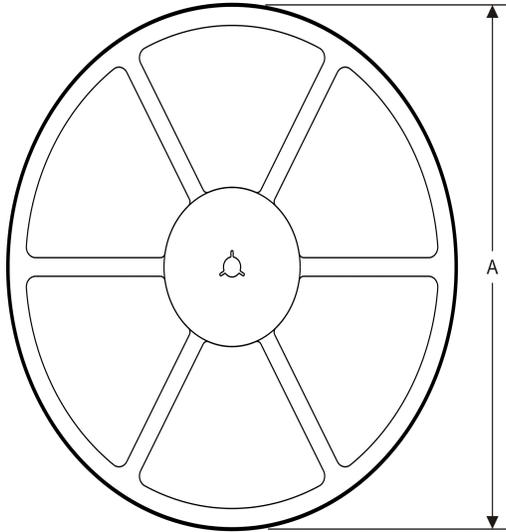
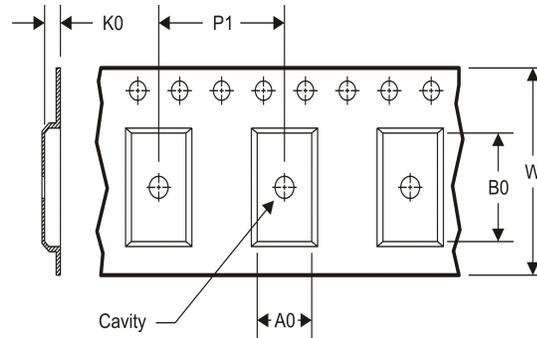
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54HC590A, SN74HC590A :**

- Catalog: [SN74HC590A](#)
- Military: [SN54HC590A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC590ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC590ADWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

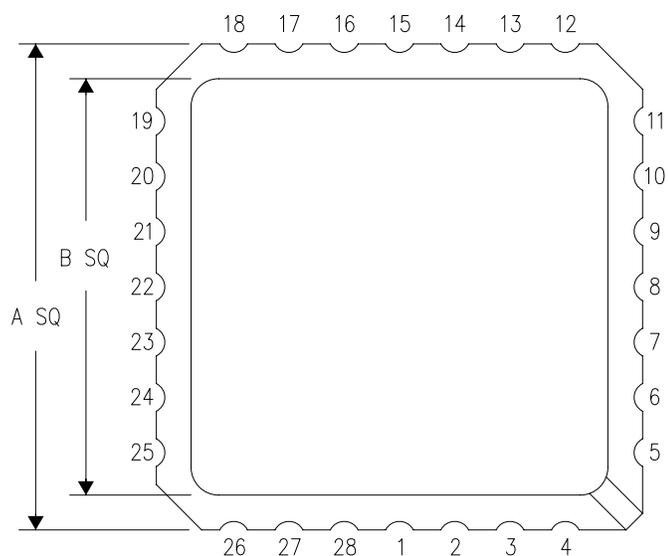

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC590ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74HC590ADWR	SOIC	DW	16	2000	367.0	367.0	38.0

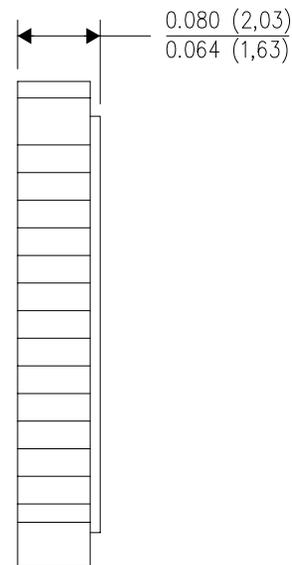
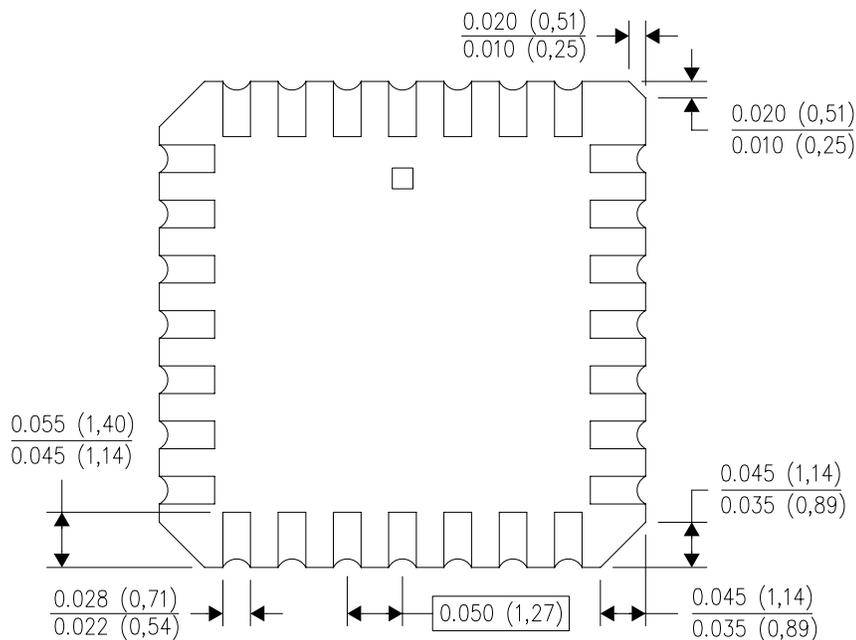
FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

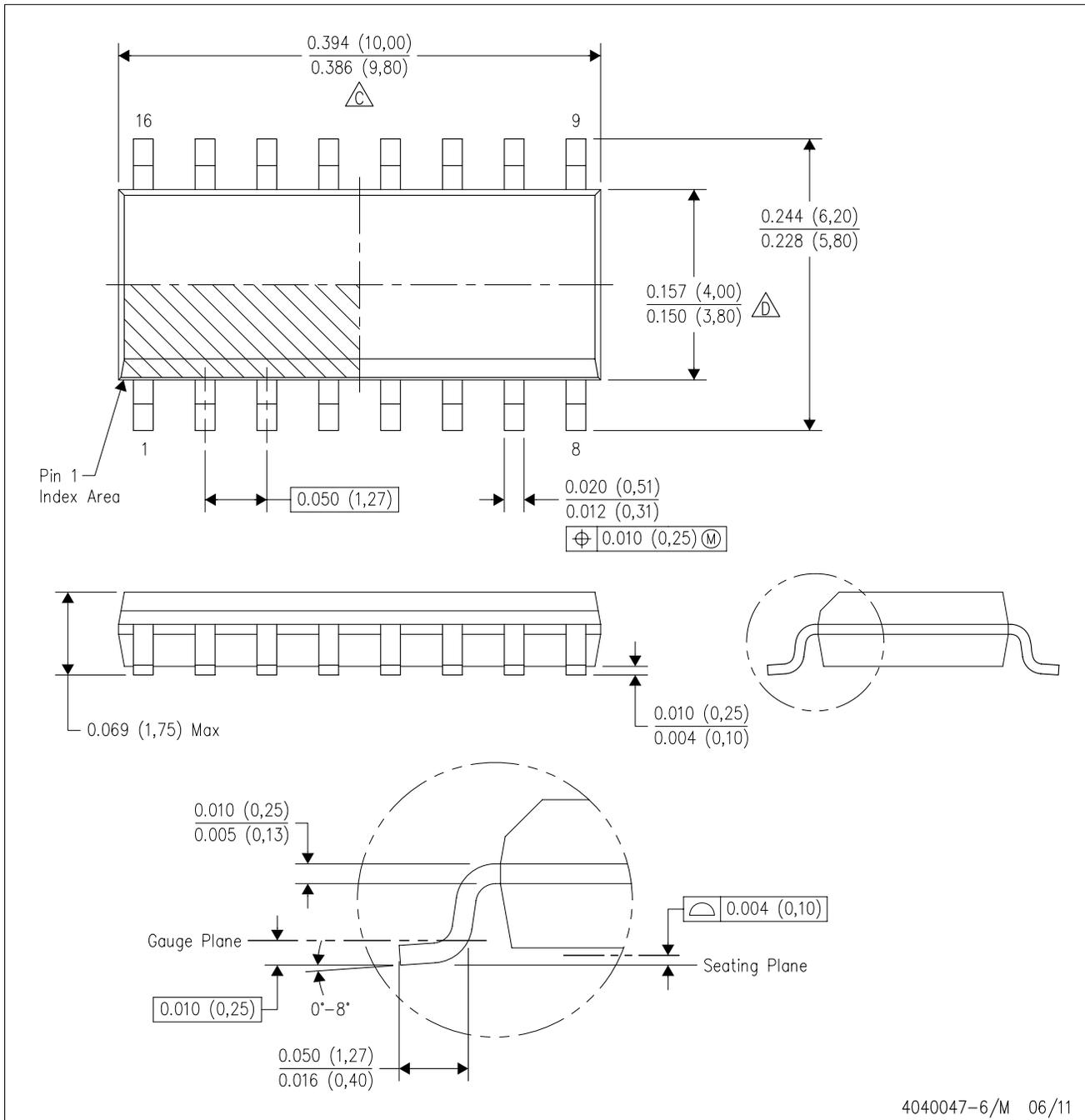


4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

D (R-PDSO-G16)

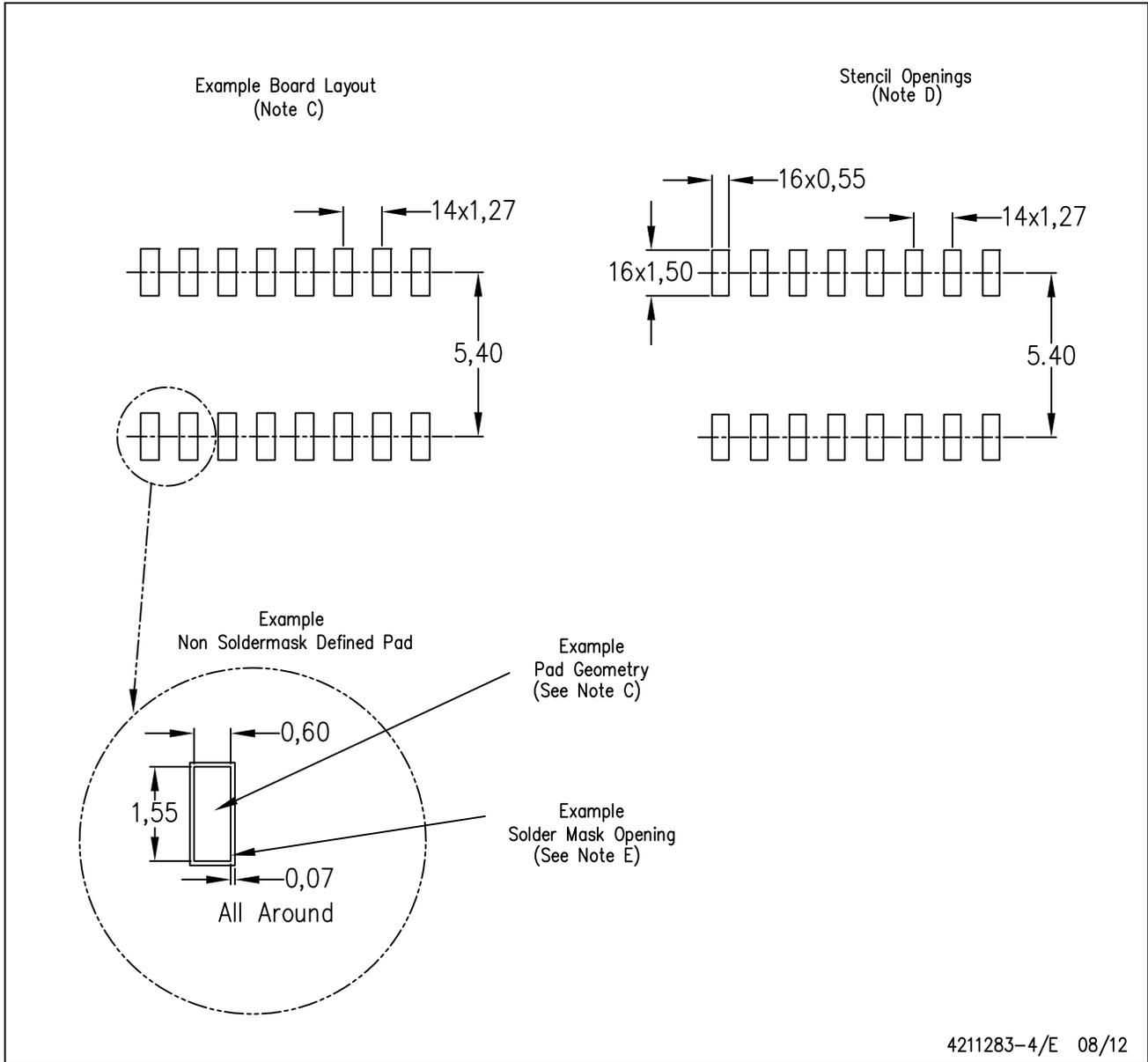
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

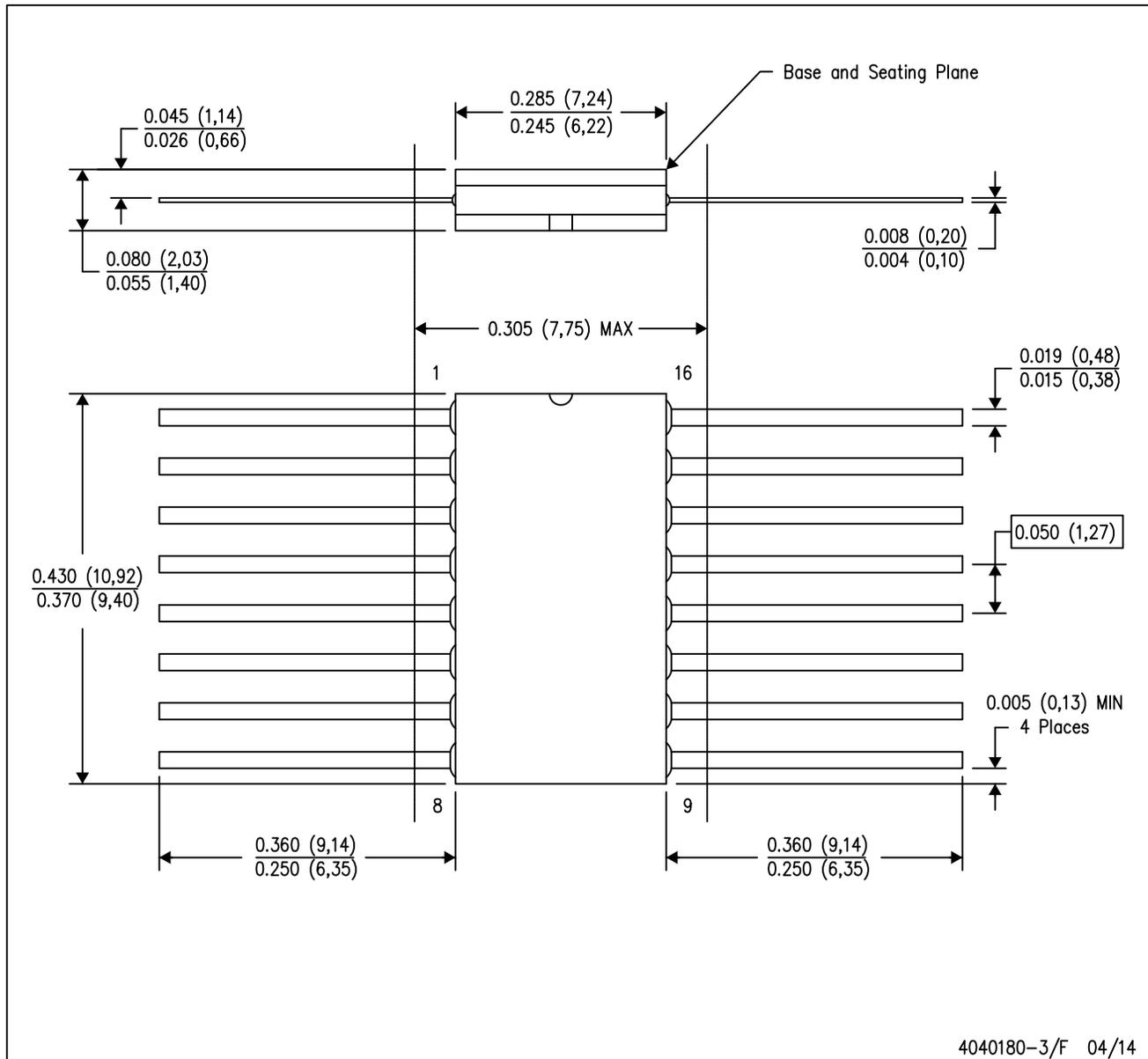
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

W (R-GDFP-F16)

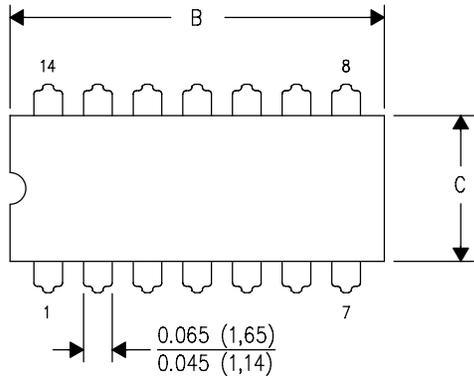
CERAMIC DUAL FLATPACK



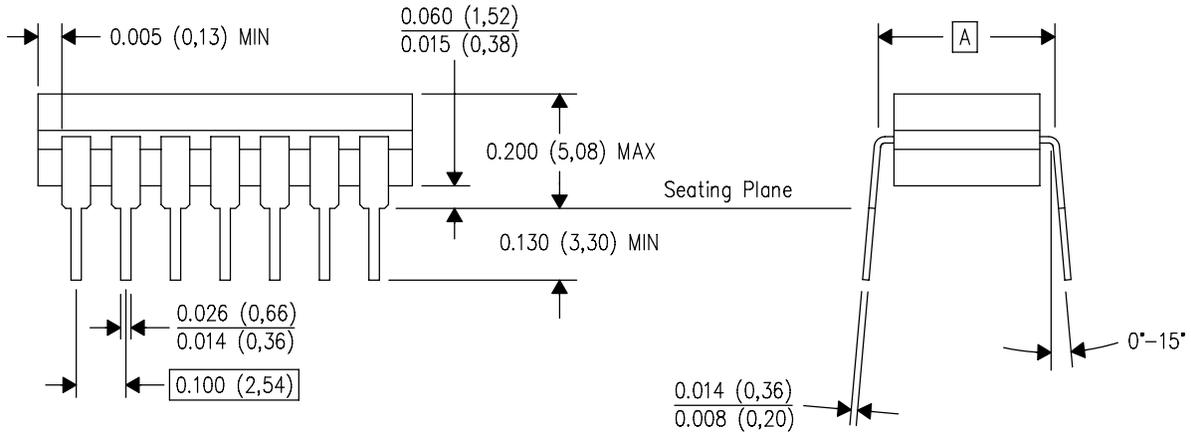
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP2-F16

J (R-GDIP-T\*\*)  
14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

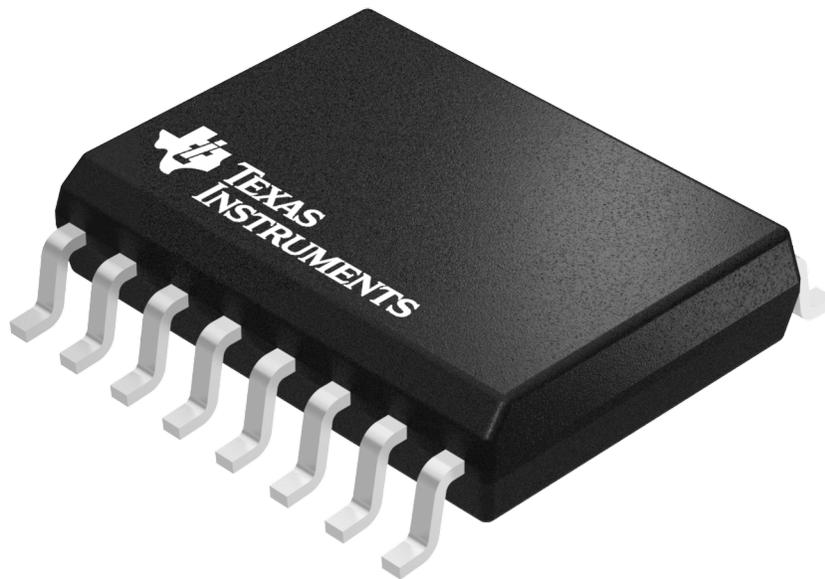
- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## GENERIC PACKAGE VIEW

DW 16

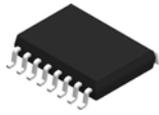
**SOIC - 2.65 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

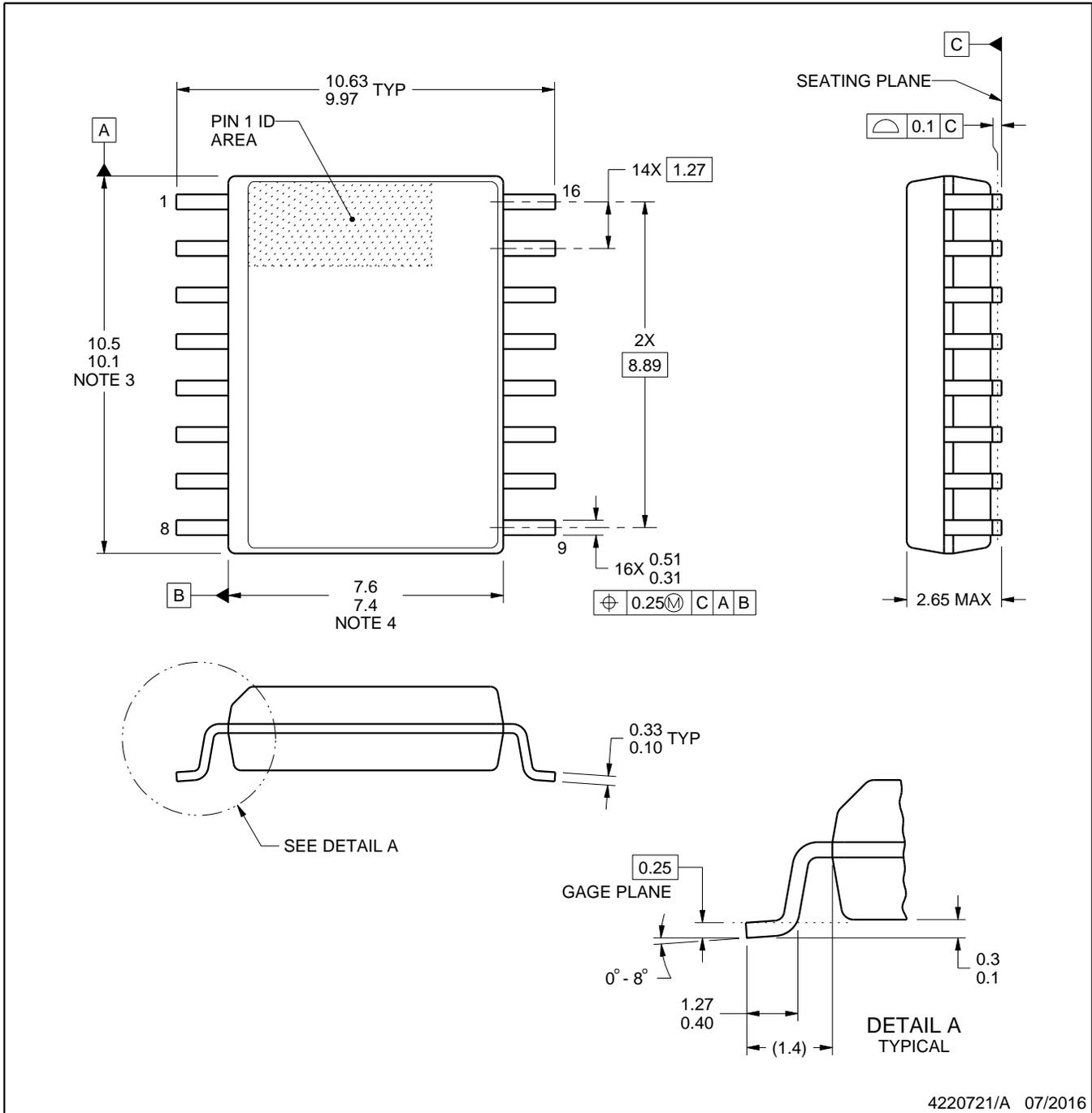
4040000-2/H



# DW0016A

# PACKAGE OUTLINE SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

### NOTES:

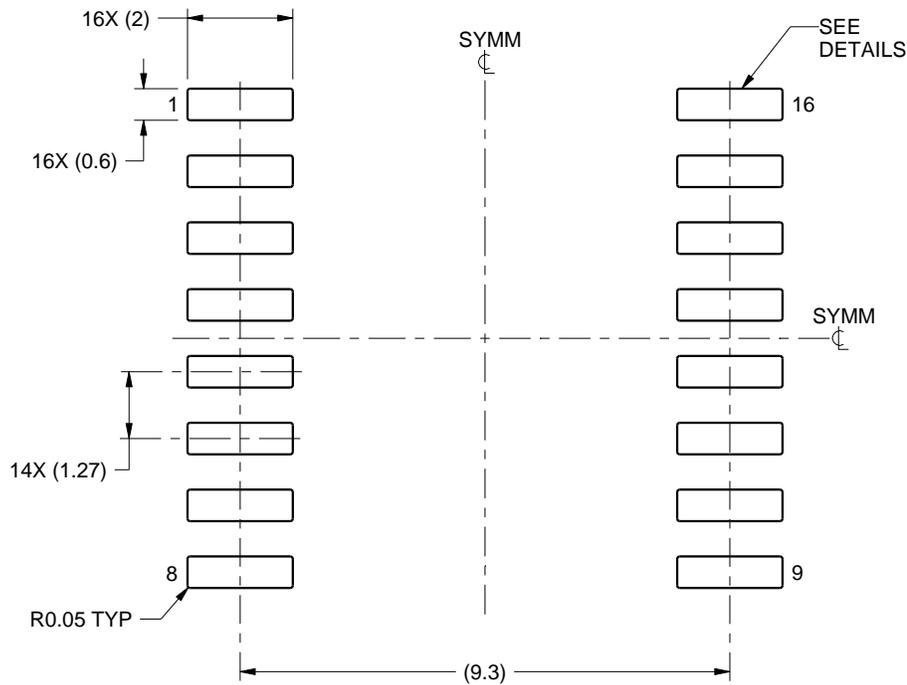
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

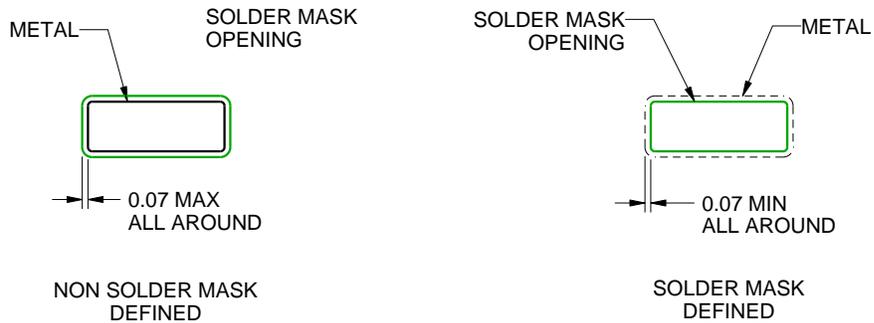
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

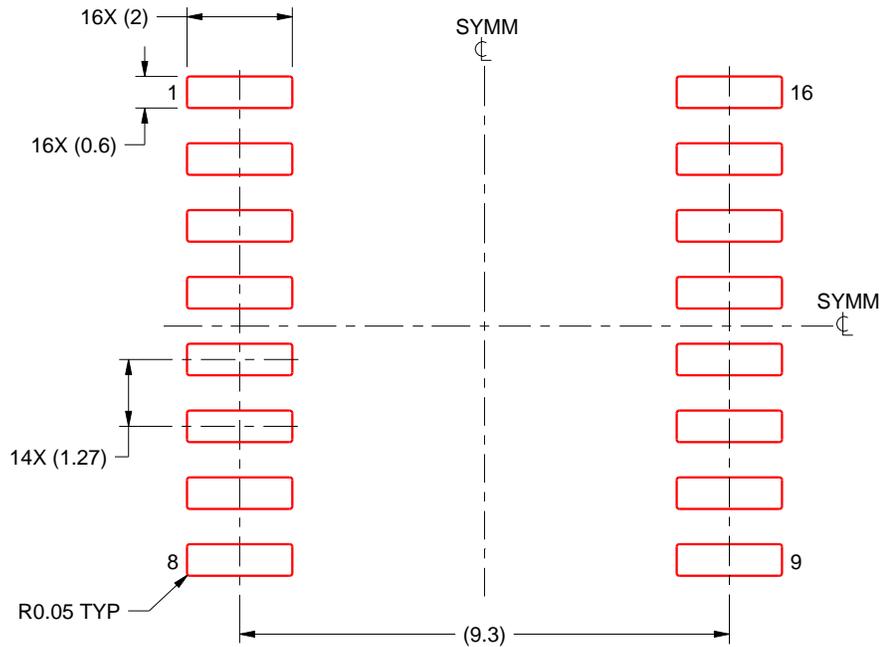
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220721/A 07/2016

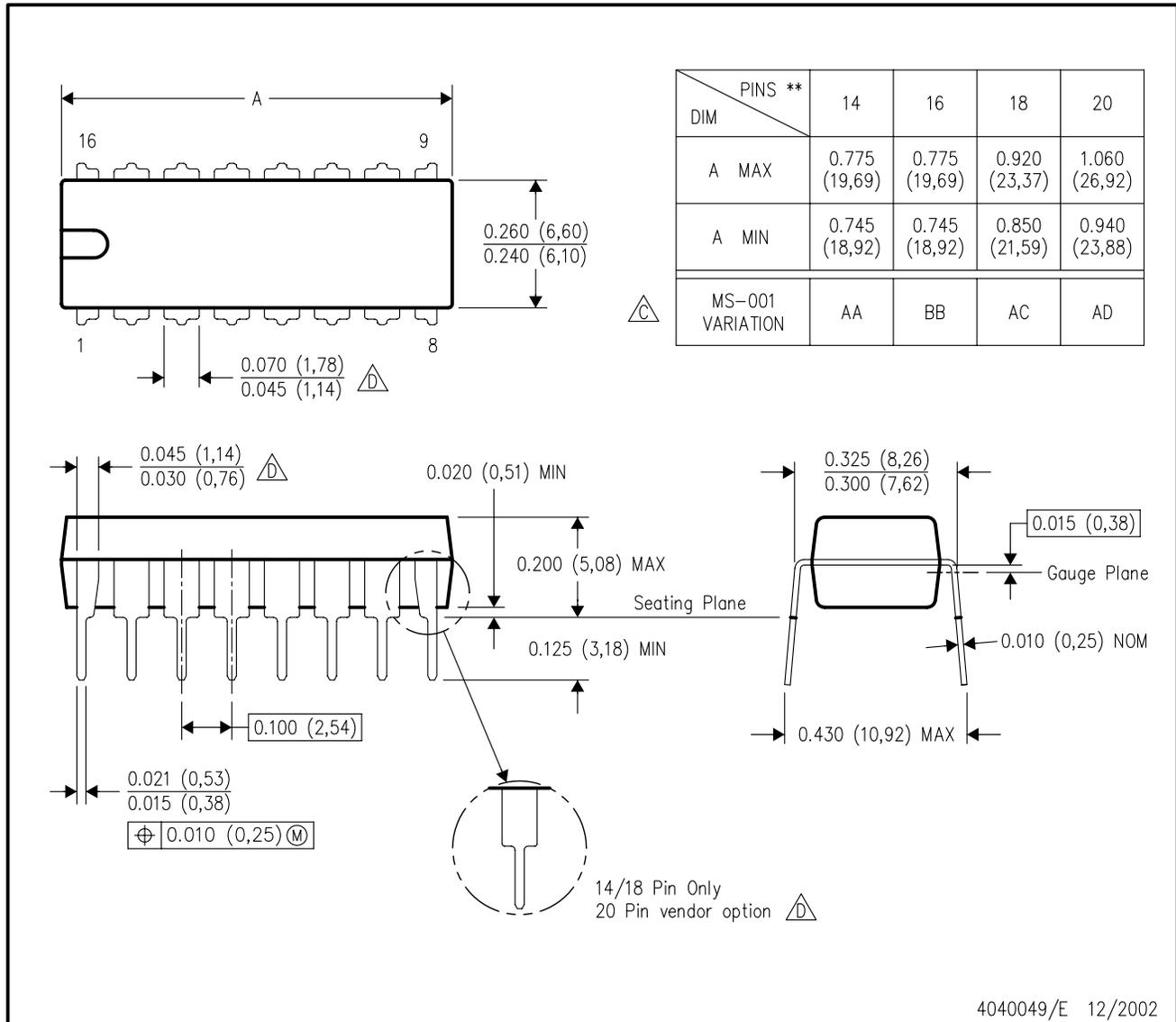
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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