Triple-Supply Power Management IC
for Powering FPGAs and DSPs

Check for Samples: TPS75003

FEATURES

- **Two 95% Efficient, 3A Buck Controllers and One 300mA LDO**
- **Tested and Endorsed by Xilinx for Powering the Spartan™-3, Spartan-3E and Spartan-3L FPGAs**
- **Adjustable (1.2V to 6.5V for Bucks, 1.0V to 6.5V for LDO) Output Voltages on All Channels**
- **Input Voltage Range: 2.2V to 6.5V**
- **Independent Soft-Start for Each Supply**
- **Independent Enable for Each Supply for Flexible Sequencing**
- **LDO Stable with 2.2μF Ceramic Output Cap**
- **Small, Low-Profile 4.5mm x 3.5mm x 0.9mm QFN Package**

APPLICATIONS

- **FPGA/DSP/ASIC Supplies**
- **Set-Top Boxes**
- **DSL Modems**
- **Plasma TV Display Panels**

DESCRIPTION

The TPS75003 is a complete power management solution for FPGA, DSP and other multi-supply applications. The device has been tested with and meets all of the Xilinx Spartan-3, Spartan-3E and Spartan-3L start-up profile requirements, including monotonic voltage ramp and minimum voltage rail rise time. Independent Enables for each output allow sequencing to minimize demand on the power supply at start-up. Soft-start on each supply limits inrush current during start-up. Two integrated buck controllers allow efficient, cost-effective voltage conversion for both low and high current supplies such as core and I/O. A 300mA LDO is integrated to provide an auxiliary rail such as V_{CCAUX} on the Xilinx Spartan-3 FPGA. All three supply voltages are offered in user-programmable options for maximum flexibility.

The TPS75003 is fully specified from −40°C to +85°C and is offered in a QFN package, yielding a highly compact total solution size with high power dissipation capability.
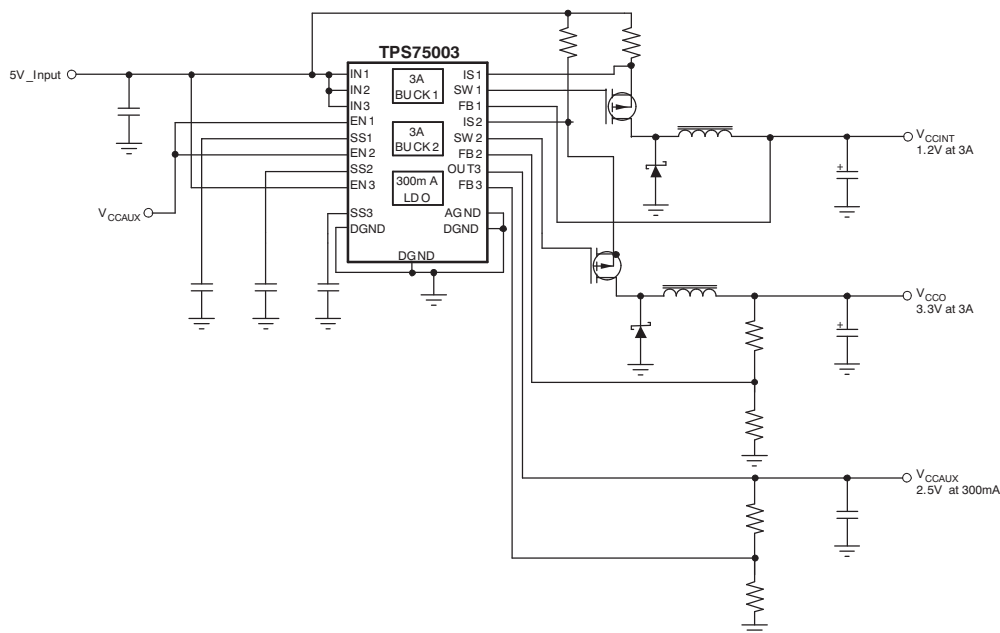
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION[1]

PRODUCT	V_{OUT}
TPS75003	Buck1: Adjustable Buck2: Adjustable LDO: Adjustable

(1) For the most current specifications and package information, see the Package Option Addendum located at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)[1]

	TPS75003	UNIT
V_{INX} range (IN1, IN2, IN3)	−0.3 to +7.0	V
V_{ENX} range (EN1, EN2, EN3)	−0.3 to V_{INX} +0.3	V
V_{SWX} range (SW1, SW2, SW3)	−0.3 to V_{INX} +0.3	V
V_{ISX} range (IS1, IS2, IS3)	−0.3 to V_{INX} +0.3	V
V_{OUT3} range	−0.3 to +7.0	V
V_{SSX} range (SS1, SS2, SS3)	−0.3 to V_{INX} +0.3	V
V_{FBX} range (FB1, FB2, FB3)	−0.3 to +3.3	V
Peak LDO output current (I_{OUT3})	Internally limited	—
Continuous total power dissipation	See Dissipation Ratings Table	—
Junction temperature range, T_J	−55 to +150	°C
Storage temperature range	−65 to +150	°C
ESD rating, HBM	1	kV
ESD rating, CDM	500	V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the Electrical Characteristics is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

	THERMAL METRIC[1][2]	TPS75003 RHL (20 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	42.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	51.8	
θ_{JB}	Junction-to-board thermal resistance	39.5	
ψ_{JT}	Junction-to-top characterization parameter	0.6	
ψ_{JB}	Junction-to-board characterization parameter	14.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	2.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

Product Folder Link(s): TPS75003

ELECTRICAL CHARACTERISTICS

$V_{EN1} = V_{IN1}$, $V_{EN2} = V_{IN2}$, $V_{EN3} = V_{IN3}$, $V_{IN1} = V_{IN2} = 2.2V$, $V_{IN3} = 3.0V$, $V_{OUT3} = 2.5V$, $C_{OUT1} = C_{OUT2} = 47\mu F$, $C_{OUT3} = 2.2\mu F$, $T_A = -40°C$ to $+85°C$, unless otherwise noted. Typical values are at $T_A = +25°C$.

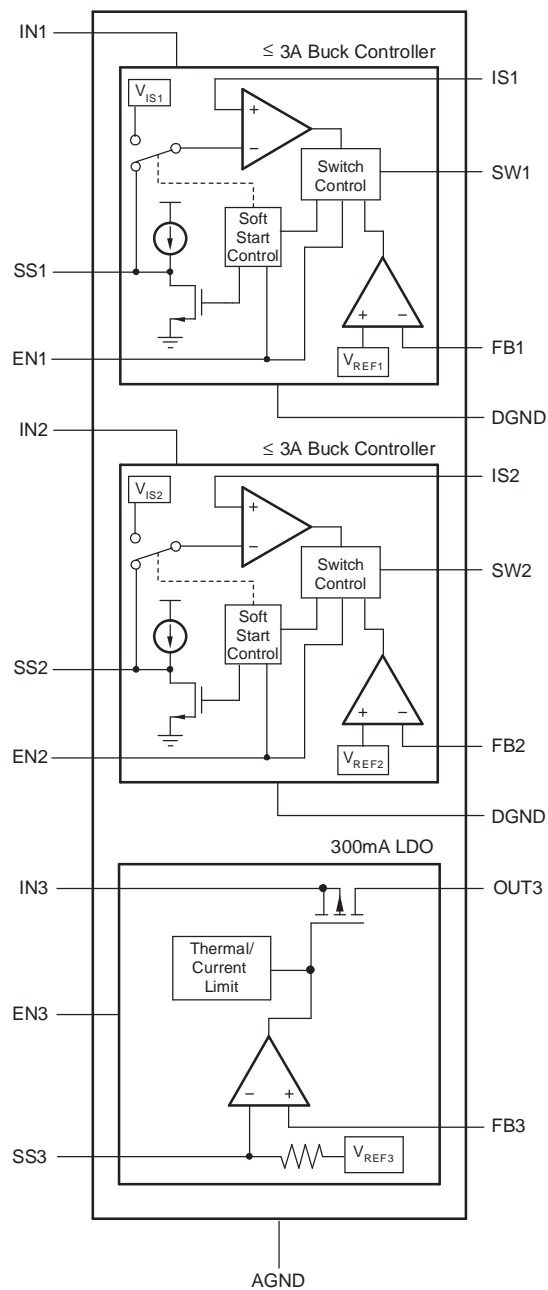|	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supply and Logic						
V_{INX}	Input Voltage Range (IN1, IN2, IN3)[1]		2.2		6.5	V
I_Q	Quiescent Current, $I_Q = I_{DGND} + I_{AGND}$	$I_{OUT1} = I_{OUT2} = 0mA$, $I_{OUT3} = 1mA$		75	150	μA
I_{SHDN}	Shutdown Supply Current	$V_{EN1} = V_{EN2} = V_{EN3} = 0V$		0.05	3.0	μA
$V_{IH1, 2}$	Enable High, enabled (EN1, EN2)		1.4		V_{INX}	V
V_{IH3}	Enable High, enabled (EN3)		1.14		V_{IN3}	V
V_{ILX}	Enable Low, shutdown (EN1, EN2, EN3)		0		0.3	V
I_{ENX}	Enable pin current (EN1, EN2, EN3)			0.01	0.5	μA
Buck Controllers 1 and 2						
$V_{OUT1,2}$	Adjustable Output Voltage Range[2]		V_{FBX}		V_{INX}	V
$V_{FB1,2}$	Feedback Voltage (FB1, FB2)			1.220		V
	Feedback Voltage Accuracy[1] (FB1, FB2)		−2		+2	%
$I_{FB1,2}$	Current into FB1, FB2 pins			0.01	0.5	μA
$V_{IS1,2}$	Reference Voltage for Current Sense		80	100	120	mV
$I_{IS1,2}$	Current into IS1, IS2 Pins			0.01	0.5	μA
$\Delta V_{OUT\%}/\Delta V_{IN}$	Line Regulation[1]	Measured with the circuit in Figure 1, $V_{OUT} + 0.5V \le V_{IN} \le 6.5V$		0.1		% / V
$\Delta V_{OUT\%}/\Delta I_{OUT}$	Load Regulation	Measured with the circuit in Figure 1, $30mA \le I_{OUT} \le 2A$		0.6		% / A
$n_{1,2}$	Efficiency[3]	Measured with the circuit in Figure 1, $I_{OUT} = 1A$		94		%
$t_{STR1,2}$	Startup Time[3]	Measured with the circuit in Figure 1, $R_L = 6\Omega$, $C_{OUT} = 100\mu F$, $C_{SS} = 2.2nF$		5		ms
$R_{DS,ON1,2}$	Gate Driver P-Channel and N-Channel MOSFET On-Resistance	$V_{IN1,2} > 2.5V$		4		Ω
		$V_{IN1,2} = 2.2V$		6		
$I_{SW1,2}$	Gate Driver P-Channel and N-Channel MOSFET Drive Current			100		mA
t_{ON}	Minimum On Time		1.36	1.55	1.84	μs
t_{OFF}	Minimum Off Time		0.44	0.65	0.86	μs

(1) To be in regulation, minimum V_{IN1} (or V_{IN2}) must be greater than $V_{OUT1,NOM}$ (or $V_{OUT2,NOM}$) by an amount determined by external components. Minimum $V_{IN3} = V_{OUT3} + V_{DO}$ or 2.2V, whichever is greater.
(2) Maximum V_{OUT} depends on external components and will be less than V_{IN}.
(3) Depends on external components.

ELECTRICAL CHARACTERISTICS (continued)

$V_{EN1} = V_{IN1}$, $V_{EN2} = V_{IN2}$, $V_{EN3} = V_{IN3}$, $V_{IN1} = V_{IN2} = 2.2V$, $V_{IN3} = 3.0V$, $V_{OUT3} = 2.5V$, $C_{OUT1} = C_{OUT2} = 47\mu F$, $C_{OUT3} = 2.2\mu F$, $T_A = -40°C$ to $+85°C$, unless otherwise noted. Typical values are at $T_A = +25°C$.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
LDO						
V_{OUT3}	Output Voltage Range		1.0		$6.5 - V_{DO}$	V
V_{FB3}	Feedback Pin Voltage			0.507		V
	Feedback Pin Voltage Accuracy[4]	$2.95V \leq V_{IN3} \leq 6.5V$ $1mA \leq I_{OUT3} \leq 300mA$	−4.0		+4.0	%
$\Delta V_{OUT\%}/\Delta V_{IN}$	Line Regulation[4]	$V_{OUT3} + 0.5V \leq V_{IN3} \leq 6.5V$		0.075		% / V
$\Delta V_{OUT\%}/\Delta I_{OUT}$	Load Regulation	$10mA \leq I_{OUT3} \leq 300mA$		0.01		% / mA
V_{DO}	Dropout Voltage ($V_{IN} = V_{OUT(NOM)} - 0.1$)[5]	$I_{OUT3} = 300mA$		250	350	mV
I_{CL3}	Current Limit	$V_{OUT} = 0.9 \times V_{OUT(NOM)}$	375	600	1000	mA
I_{FB3}	Current into FB3 pin			0.03	0.1	μA
V_n	Output Noise	BW = 100Hz − 100kHz, $I_{OUT3} = 300mA$		400		μV_{RMS}
t_{SD}	Thermal Shutdown Temperature for LDO	Shutdown, Temp Increasing		175		°C
		Reset, Temp Decreasing		160		
UVLO	Under-Voltage Lockout Threshold	V_{IN} Rising		1.80		V
	Under-Voltage Lockout Hysteresis	V_{IN} Falling		100		mV

(4) To be in regulation, minimum V_{IN1} (or V_{IN2}) must be greater than $V_{OUT1,NOM}$ (or $V_{OUT2,NOM}$) by an amount determined by external components. Minimum $V_{IN3} = V_{OUT3} + V_{DO}$ or 2.2V, whichever is greater.
(5) V_{DO} does not apply when $V_{OUT} + V_{DO} < 2.2V$.

DEVICE INFORMATION

Functional Block Diagram

TPS75003

RHL PACKAGE
4.5mm x 3.5mm QFN
(TOP VIEW)
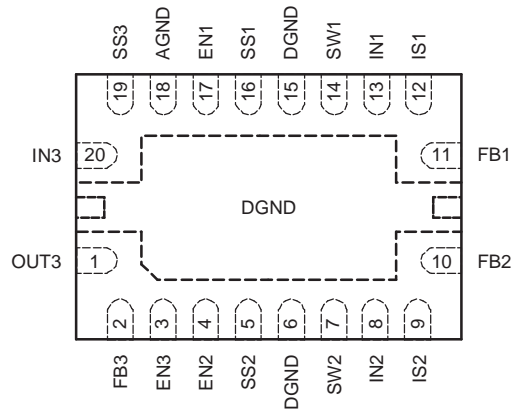
TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	RHL	
DGND	6, 15, PAD	Ground connection for BUCK1 and BUCK2 converters. Pins 6 and 15 should be connected to the back side exposed pad by a short metal trace as shown in the *PCB Layout* section of this data sheet.
AGND	18	Ground connection for LDO.
IN1	13	Input supply to BUCK1.
IN2	8	Input supply to BUCK2.
IN3	20	Input supply to LDO.
EN1	17	Driving the enable pin (ENx) high turns on BUCK1 regulator. Driving this pin low puts it into shutdown mode, reducing operating current. The enable pin does not trigger on fast negative going transients.
EN2	4	Same as EN1 but for BUCK2 controller.
EN3	3	Same as EN1 but for LDO.
SS1	16	Connecting a capacitor between this pin and ground increases start-up time of the BUCK1 regulator by slowing the ramp-up of current limit. This high-impedance pin is noise-sensitive; careful layout is important. See the *Typical Characteristics, Applications,* and *PCB Layout* sections for details.
SS2	5	Same as SS1 but for BUCK2 regulator.
SS3	19	Connecting a capacitor from this pin to ground slows the start-up time of the LDO reference, therby slowing output voltage ramp-up. See the *Applications* section for details.
IS1	12	Current sense input for BUCK1 regulator. The voltage difference between this pin and IN1 is compared to an internal reference to set current limit. For a robust output start-up ramp, careful layout and bypassing are required. See the *Applications* section for details.
IS2	9	Same as IS1 but compared to IN2 and used for BUCK2 controller.
SW1	14	Gate drive pin for external BUCK1 P-channel MOSFET.
SW2	7	Same as SW1 but for BUCK2 controller.
FB1	11	Feedback pin. Used to set the output voltage of BUCK1 regulator.
FB2	10	Same as FB1 but for BUCK2 controller.
FB3	2	Same as FB1 but for LDO.
OUT3	1	Regulated LDO output. A small ceramic capacitor (≥ 2.2μF) is needed from this pin to ground to ensure stability.

Product Folder Link(s): *TPS75003*

Typical Application Circuit for Powering the Xilinx Spartan-3 FPGA
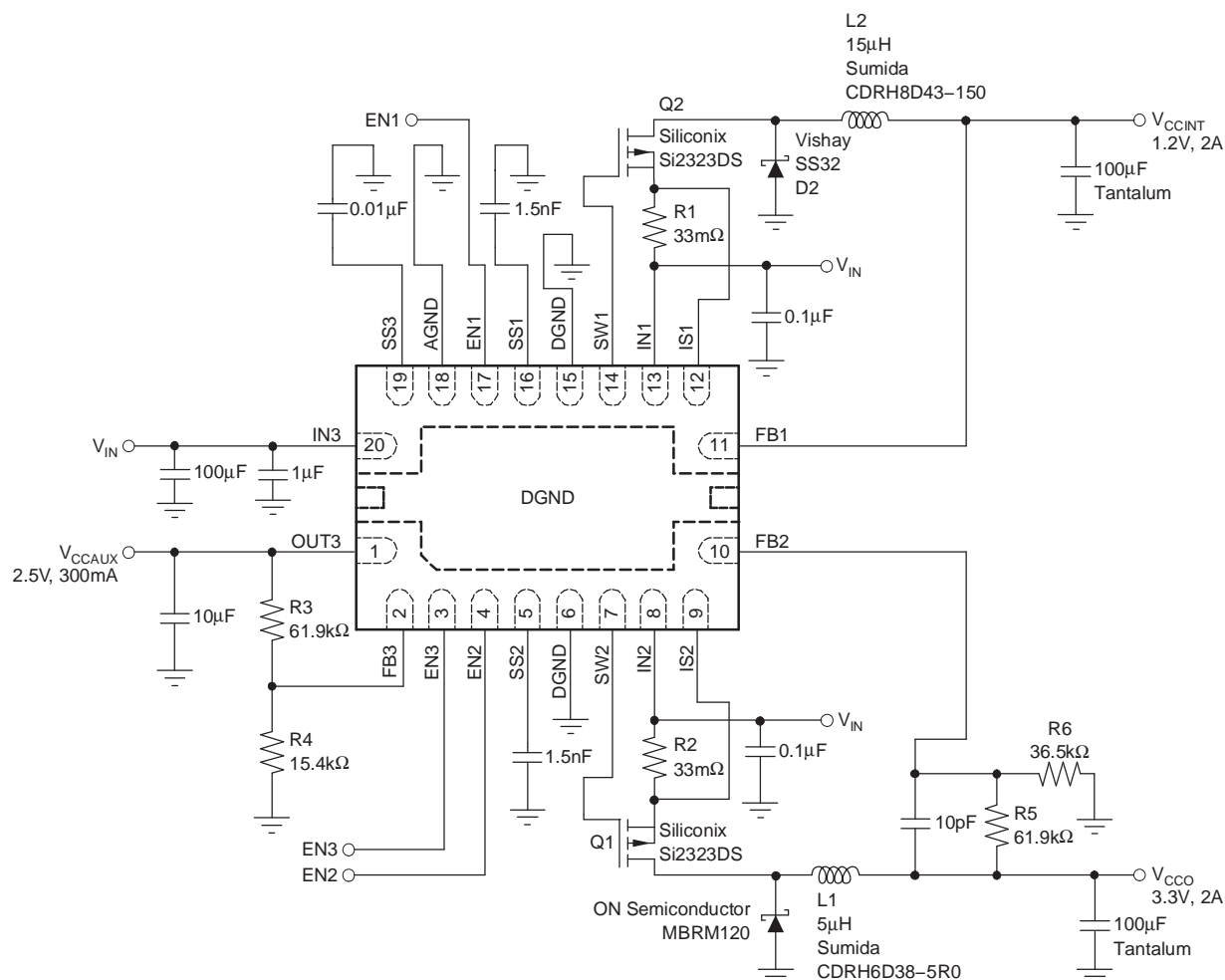
Figure 1.

TYPICAL CHARACTERISTICS
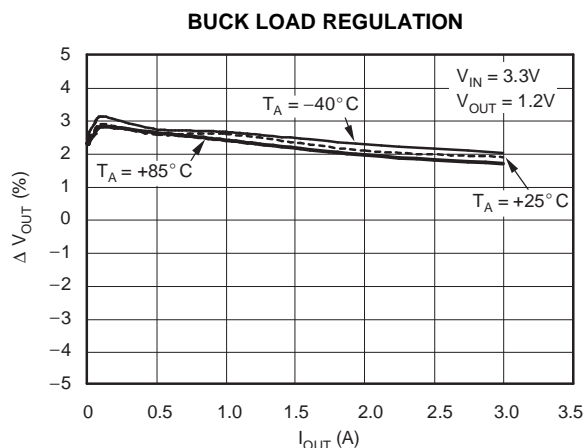
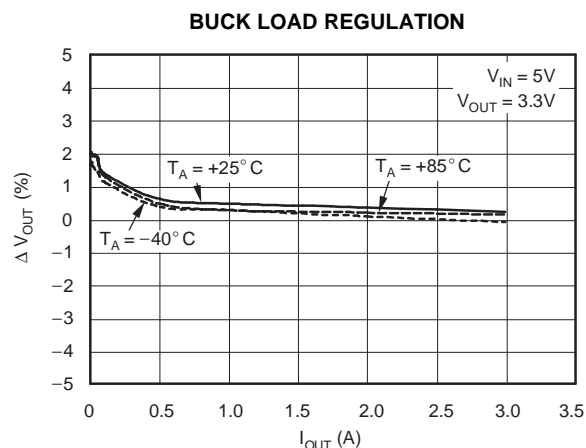Measured using circuit in Figure 1.

Buck Converter

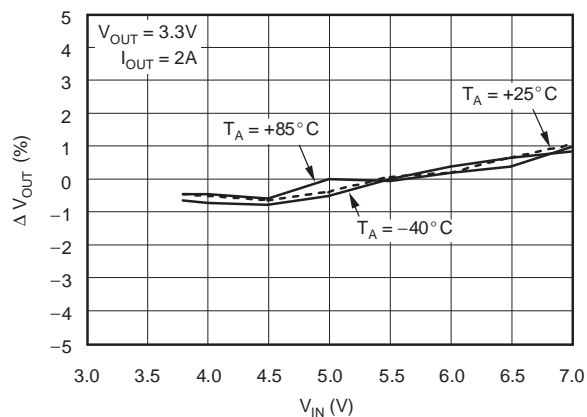BUCK LOAD REGULATION

V_{IN} = 3.3V
V_{OUT} = 1.2V

T_A = −40°C

T_A = +85°C

T_A = +25°C

Figure 2.

BUCK LOAD REGULATION

V_{IN} = 5V
V_{OUT} = 3.3V

T_A = +25°C

T_A = +85°C

T_A = −40°C

Figure 3.

TYPICAL CHARACTERISTICS (continued)

Measured using circuit in Figure 1.

BUCK LINE REGULATION
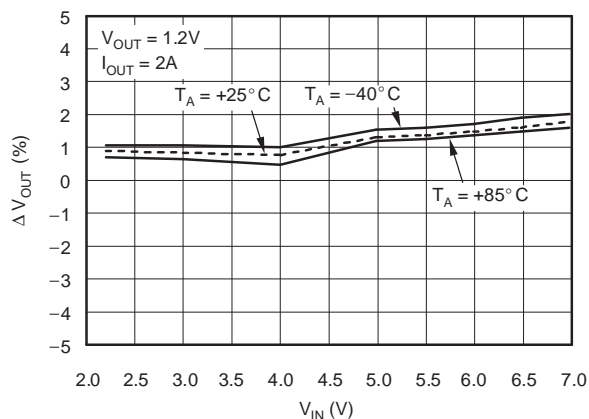
Figure 4.

BUCK LINE REGULATION

Figure 5.

BUCK SWITCHING FREQUENCY
vs
I_{OUT}, T_A
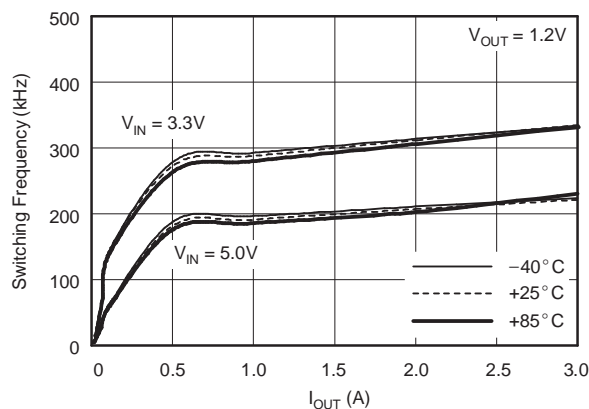
Figure 6.

BUCK SWITCHING FREQUENCY
vs
I_{OUT}
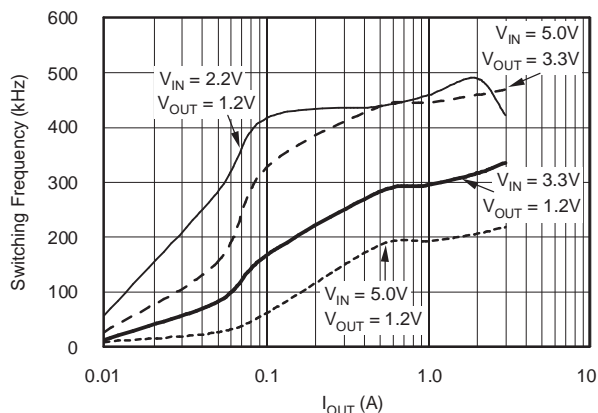
Figure 7.

BUCK OUTPUT VOLTAGE RIPPLE
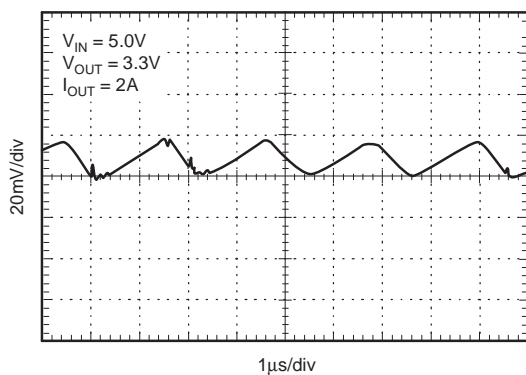
Figure 8.

EFFICIENCY vs
I_{OUT}

Figure 9.

Product Folder Link(s): *TPS75003*

TYPICAL CHARACTERISTICS (continued)

Measured using circuit in Figure 1.

**BUCK START-UP
vs
V_{IN} and I_{OUT} [1]**

EN
V_{IN} = 5V, I_{OUT} = 0.5A
V_{IN} = 5V, I_{OUT} = 1.0A
V_{IN} = 3.3V, I_{OUT} = 1.0A
V_{OUT} (500mV/div)
V_{IN} = 5V, I_{OUT} = 2.0A
V_{IN} = 3.3V, I_{OUT} = 2.0A
C_{SS} = 0.01µF
V_{OUT} = 1.2V
20ms/div

Figure 10.

**BUCK START-UP
vs
V_{IN} and C_{OUT} [1]**

EN
V_{OUT} (500mV/div)
V_{IN} = 5V, C_{OUT} = 330µF
V_{IN} = 5V, C_{OUT} = 100µF
V_{IN} = 3.3V, C_{OUT} = 680µF
V_{IN} = 3.3V, C_{OUT} = 100µF
C_{SS} = 0.01µF
V_{OUT} = 1.2V
20ms/div

Figure 11.

**BUCK START-UP
vs
V_{IN} and C_{SS} [1]**

EN
V_{OUT} (500mV/div)
V_{IN} = 3.3V, C_{SS} = 0.001µF
V_{IN} = 5V, C_{SS} = 0.001µF
V_{IN} = 5V, C_{SS} = 0.01µF
V_{IN} = 3.3V, C_{SS} = 0.01µF
I_{OUT} = 1A
V_{OUT} = 1.2V
20ms/div

Figure 12.

**BUCK START-UP
vs
I_{OUT} and C_{SS} [1]**

V_{IN} = 5V
V_{OUT} = 3.3V   EN
V_{OUT} (2V/div)
I_{OUT} = 2A, C_{SS} = 560pF
I_{OUT} = 0.5A, C_{SS} = 560pF
I_{OUT} = 0.5A, C_{SS} = 1500pF
I_{OUT} = 2A, C_{SS} = 1500pF
5ms/div

Figure 13.

**BUCK START-UP
vs
V_{IN} and R_{SENSE} [1]**

V_{OUT} = 1.2V, C_{SS} = 0.01µF
EN
V_{IN} = 3.3V, I_{OUT} = 1A, R_S = 0.020
V_{IN} = 3.3V, I_{OUT} = 1A, R_S = 0.033
V_{IN} = 5V, I_{OUT} = 1A, R_S = 0.020
V_{OUT} (1V/div)
V_{IN} =5V, I_{OUT} = 1A, R_S = 0.033
20ms/div

Figure 14.

(1)xxxSee the section, *Soft-Start Capacitor Selection (Buck Controllers)* .

(1) See the section, *Soft-Start Capacitor Selection (Buck Controllers)* .

TYPICAL CHARACTERISTICS (continued)

Measured using circuit in Figure 1.

LDO Converter
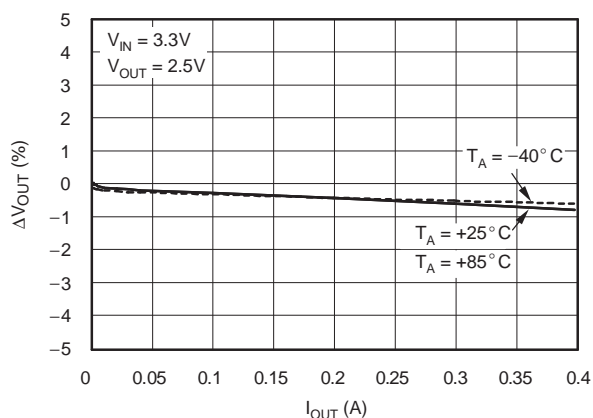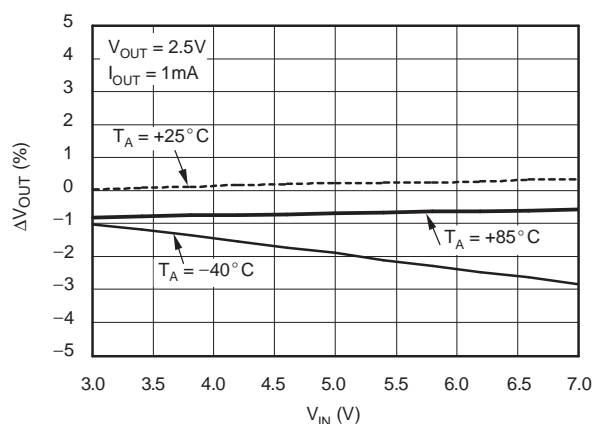
Figure 15.

Figure 16.

Figure 17.

Figure 18.

Figure 19.

Figure 20.

Product Folder Link(s): *TPS75003*

TYPICAL CHARACTERISTICS (continued)

Measured using circuit in Figure 1.

**LDO V_OUT
vs
T_A**

Figure 21.

Product Folder Link(s): *TPS75003*
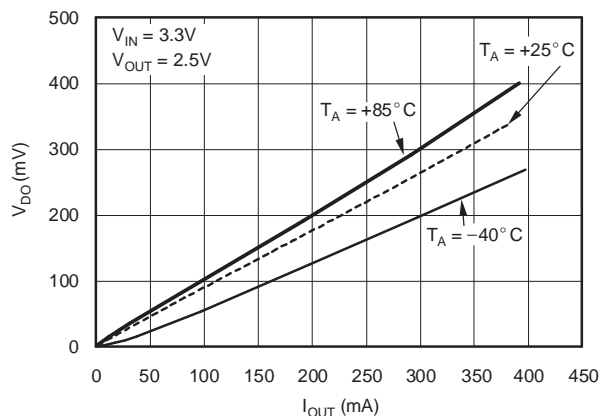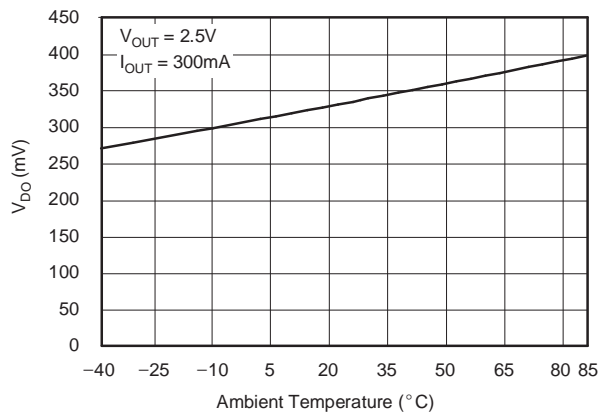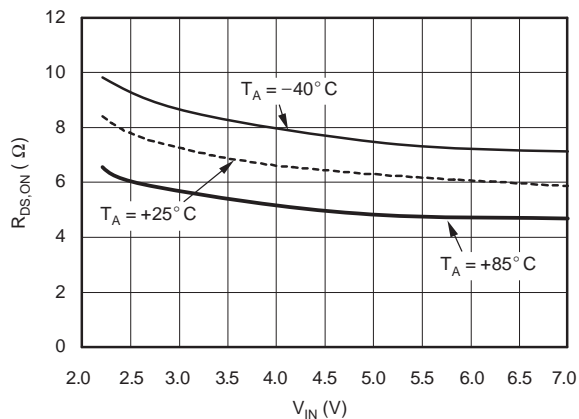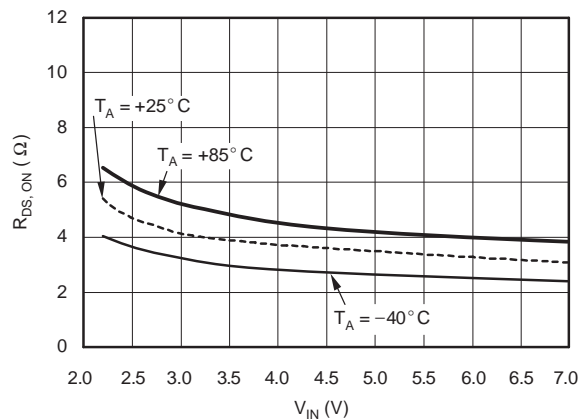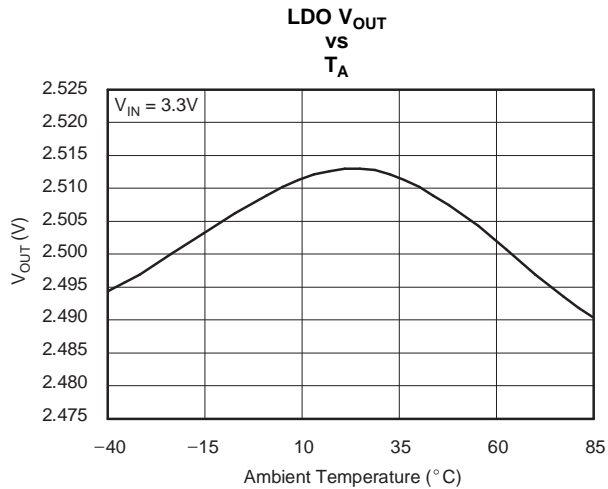
APPLICATION INFORMATION

The TPS75003 is an integrated power management IC designed specifically to power DSPs and FPGAs such as the Xilinx Spartan-3, Spartan-3E and Spartan-3L. Two non-synchronous buck controllers can be configured to supply up to 3A for both CORE and I/O rails. A low dropout linear regulator powers auxiliary rails up to 300mA. All channels have independent enable and soft-start, allowing control of inrush current and output voltage ramp time as required by the application.

Figure 1 shows a typical application circuit for powering the Xilinx Spartan-3 FPGA. Table 1 through Table 4 show component values that have been tested for use with up to 3A load currents. Inductors in Table 1 are tested up to the respective saturation currents. Other similar external components can be substituted as desired; however, in all cases the circuits that are used should be tested for compliance to application requirements.

Table 1. Inductors Tested with the TPS75003

PART NUMBER	MANUFACTURER	INDUCTANCE	DC RESISTANCE	SATURATION CURRENT
SLF7032T–100M1R4	TDK	10μH ±20%	53mΩ ±20%	1.4A
SLF6025–150MR88	TDK	15μH ±20%	85mΩ ±20%	0.88A
CDRH6D28–5R0	Sumida	5μH	23mΩ	2.4A
CDRH6D38-5R0	Sumida	5μH	18mΩ	2.9A
CDRH103R–100	Sumida	10μH	45mΩ	2.4A
CDRH4D28–100	Sumida	10μH	96mΩ	1.0A
CDRH8D43-150	Sumida	15μH	42mΩ	2.9A
CDRH5D18–6R2	Sumida	6.2μH	71mΩ	1.4A
DO3316P–472	Coilcraft	4.7μH	18mΩ	5.4A
DT3316P–153	Coilcraft	15μH	60mΩ	1.8A
DT3316P–223	Coilcraft	22μH	84mΩ	1.5A
744052006	Wurth	6.2μH	80mΩ	1.45A
74451115	Wurth	15μH	90mΩ	0.8A

Table 2. PMOS Transistors Tested with the TPS75003

PART NUMBER	MANUFACTURER	$R_{DS,ON}$ (TYP)	V_{DS}	I_D	PACKAGE
Si5447DC	Vishay Siliconix	0.11Ω at VGS = –2.5V	–20V	–3.5A at +25°C	1206
Si5475DC	Vishay Siliconix	0.041Ω at VGS = –2.5V	–12V	–6.6A at +25°C	1206
Si2323DS	Vishay Siliconix	0.052Ω at VGS = –2.5V	–20V	–4.1A at +25°C	SOT23
Si2301ADS	Vishay Siliconix	0.19Ω at VGS = –2.5V	–20V	–1.4A at +25°C	SOT23
Si2323DS	Vishay Siliconix	0.41Ω at VGS = –2.5V	–20V	–4.1A at +25°C	SOT23
FDG326P	Fairchild	0.17Ω at VGS = –2.5V	–20V	–1.5A	SC70

Table 3. Diodes Tested with the TPS75003

PART NUMBER	MANUFACTURER	V_R	I_F	PACKAGE
MBRM120LT3	ON Semiconductor	20V	1.0A	DO216AA
MBR0530T1	ON Semiconductor	30V	1.5A	SOD123
ZHCS2000TA	Zetex	40V	2.0A	SOT23–6
B320	Diodes Inc.	20V	3.0A	SMA
SS32	Fairchild	20V	3.0A	DO214AB

Product Folder Link(s): *TPS75003*

Table 4. Capacitors Tested with the TPS75003

PART NUMBER	MANUFACTURER	CAPACITANCE	ESR	VOLTAGE RATING
6TPB47M (PosCap)	Sanyo	47μF	0.1Ω	6.3V
T491D476M010AS	Kemet	47μF	0.8Ω	10V
B45197A	Epco	47μF	0.175Ω	16V
B45294−R1107−M40	Epco	100μF	0.045Ω	6.3V
594D476X0016C2	Vishay	47μF	0.11Ω	16V
594D127X96R3C2	Vishay	120μF	0.085Ω	6.3V
TPSC107K006R0150	AVX	100μF	0.15Ω	6.3V
6TPS100MC	Sanyo	100μF	0.45Ω	6.3V

OPERATION (BUCK CONTROLLERS)

Channels 1 and 2 contain two identical non-synchronous buck controllers that use minimum on-time/minimum off-time hysteretic control. (Refer to Figure 1.) For clarity, BUCK1 is used throughout the discussion of device operation. When V_{OUT1} is below its target, an external PMOS (Q1) is turned on for at least the minimum on-time, increasing current through the inductor (L1) until V_{OUT1} reaches its target value or the current limit (set by R1) is reached. Once either of these conditions is met, the PMOS is switched off for at least the minimum off-time of the device. After the minimum off-time has passed, the output voltage is monitored and the switch is turned on again when necessary.

When output current is low, the buck controllers operate in discontinuous mode. In this mode, each switching cycle begins at zero inductor current, rises to a maximum value, then falls back to zero current. When current reaches zero on the falling edge, ringing occurs at the resonant frequency of the inductor and stray switch node capacitance. This operation is normal; it does not affect circuit performance, and can be minimized if desired by using an RC snubber and/or a resistor in series with the gate of the PMOS, as shown in Figure 22.
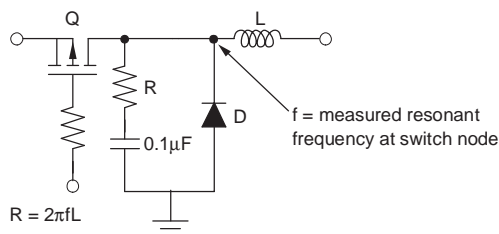
Figure 22. RC Snubber and Series Gate Resistor Used to Minimize Ringing

At higher output currents, the TPS75003 operates in continuous mode. In continuous mode, there is no ringing at the switch node and V_{OUT} is equal to V_{IN} times the duty cycle of the switching waveform.

When V_{IN} approaches or falls below V_{OUT}, the buck controllers operate in 100% duty cycle mode, fully turning on the external PMOS to allow regulation at lower dropout than would otherwise be possible.

Enable (Buck Controllers)

The enable pins (EN1 and EN2) for the buck controllers are active high. When the enable pin is driven low and input voltage is present at IN1 or IN2, an on-chip FET is turned on to discharge the soft-start pin SS1 or SS2, respectively. If the soft-start feature is being used, enable should be driven high at least 10μs after V_{IN} is applied to ensure this discharge cycle occurs.

UVLO (Buck Controllers)

An under-voltage lockout circuit is present to prevent turning on the external PMOS (Q1 or Q2) until a reliable operating voltage is reached on the appropriate regulator (IN1 or IN2). This prevents the buck controllers from mis-operation at low input voltages.

Current Limit (Buck Controllers)

An external resistor (R1 or R2) is used to set the current limit for the external PMOS transistor (Q1 or Q2). These resistors are connected between IN1 and IS1 (or IN2 and IS2) to provide a reference voltage across these pins that is proportional to the current flowing through the PMOS transistor. This reference voltage is compared to an internal reference to determine if an over-current condition exists. When current limit is exceeded, the external PMOS is turned off for the minimum off-time. Current limit detection is disabled for 10ns any time the PMOS is turned on to avoid triggering on switching noise. In 100% duty cycle mode, current limit is always enabled. Current limit is calculated using the V_{IS1} or V_{IS2} specification in the *Electrical Characteristics* section, shown in Equation 1:

$$I_{LIMIT} = \frac{V_{IS1,2}}{R_{1,2}}$$

(1)

The current limit resistor must be appropriately rated for the dissipated power determined by its RMS current calculated by Equation 2:

$$I_{RMS} = I_{OUT}\sqrt{D} = I_{OUT}\sqrt{\frac{V_{OUT}}{V_{IN}}}$$

$$P_{DISS} = (I_{RMS})^2 \cdot R$$

(2)

For low-cost applications the $I_{S1,2}$ pin can be connected to the drain of the PMOS, using $R_{DS,ON}$ instead of R1 or R2 to set current limit. Variations in the PMOS $R_{DS,ON}$ must be taken into account to ensure that current limit will protect external components such as the inductor, the diode, and the switch itself from damage as a result of over-current.

Short-Circuit Protection (Buck Controllers)

In an overload condition, the current rating of the external components (PMOS, diode, and inductor) can be exceeded. To help guard against this, the TPS75003 increases its minimum off-time when the voltage at the feedback pin is lower than the reference voltage. When the output is shorted (V_{FB} is zero), minimum off-time is increased to approximately 4μs. The increase in off-time is proportional to the difference between the voltage at the feedback pin and the internal reference.

Soft-Start (Buck Controllers)

The buck controllers each have independent soft-start capability to limit inrush during start-up and to meet timing requirements of the Xilinx Spartan-3 FPGA. Limiting inrush current by using soft-start, or by staggering the turn-on of power rails, also guards against voltage drops at the input source due to its output impedance. Refer to the soft-start circuitry shown in Figure 23 and the soft-start timing diagram shown in Figure 24. BUCK 1 will be discussed in this section; it is identical to BUCK2. Note that pins SS1 and SS2 are very high-impedance and cannot be probed using a typical oscilloscope setup. When input voltage is applied at IN1 and EN1 is driven low, any charge on the SS pin is discharged by an on-chip pull-down transistor. When EN1 is driven high, an on-chip current source starts charging the external soft-start capacitor C_{SS1}. The voltage on the capacitor is compared to the voltage across the current sense resistor R1 to determine if an over-current condition exists. If the voltage drop across the sense resistor goes above the reference voltage, then the external PMOS is shut off for the minimum off-time. This implementation provides a cycle-by-cycle current limit and allows the user to program the soft-start time over a wide range for most applications. For detailed information on choosing C_{SS1} and C_{SS2}, see the section, ***Soft-Start Capacitor Selection (Buck Controllers)*** .
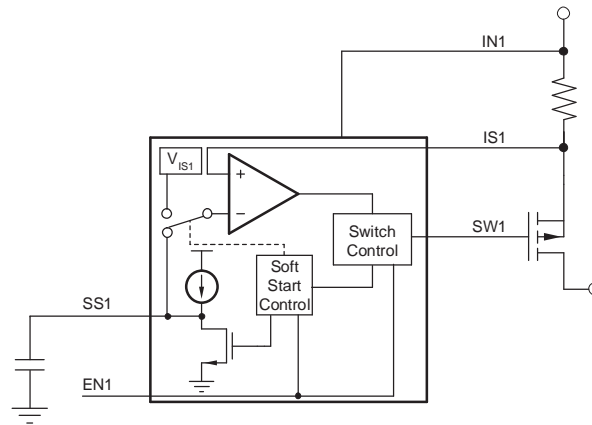
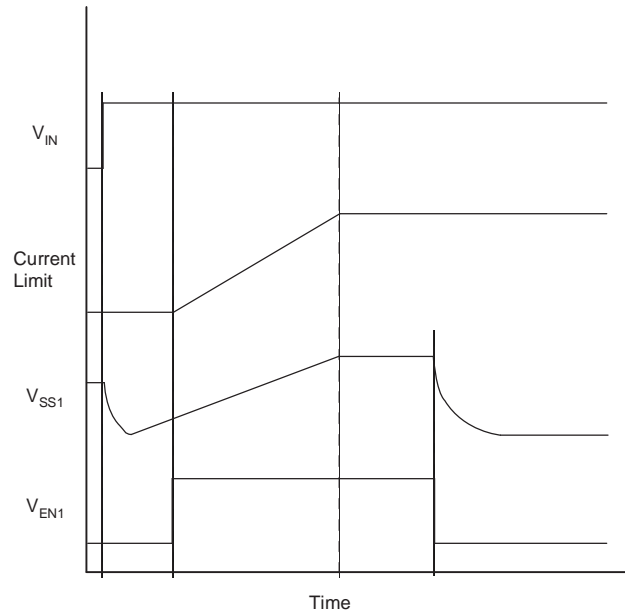**Figure 23. Soft-Start Circuitry**

Figure 24. Soft-Start Timing Diagram

Input Capacitor C_{IN1}, C_{IN2} Selection (Buck Controllers)

It is good analog design practice to place input capacitors near the inputs of the device in order to ensure a low impedance input supply. 10μF to 22μF of capacitance for each buck converter is adequate for most applications, and should be placed within 100mils (0.01in, or 2.54mm) of the IN1 and IN2 pins to minimize the effects of pulsed current switching noise on the soft-start circuitry during the first ~1V of output voltage ramp. Low ESR capacitors also help to minimize noise on the supply line. The minimum value of capacitance can be estimated using Equation 3:

$$C_{IN, \, MIN} = \frac{(1/2)L \times (\Delta I_L)^2}{V_{(RIPPLE)} \times V_{IN}} \approx \frac{(1/2)L \times (0.3 \times I_{OUT})^2}{V_{(RIPPLE)} \times V_{IN}}$$

(3)

Note that the capacitors must be able to handle the RMS current in continuous conduction mode, which can be calculated using Equation 4:

$$I_{C,IN(RMS)} \approx I_{OUT} \sqrt{\left(\frac{V_{OUT}}{V_{IN,MIN}} \right)}$$

(4)

Inductor Value Selection (Buck Controllers)

The inductor is chosen based on inductance value and maximum current rating. Larger inductors reduce current ripple (and therefore, output voltage ripple) but are physically larger and more expensive. Inductors with lower DC resistance typically improve efficiency, but also have higher cost and larger physical size. The buck converters work well with inductor values between 4.7μH and 47μH in most applications. When selecting an inductor, the current rating should exceed the current limit set by R_{IS} or $R_{DS,ON}$ (see the *Current Limit* section). To determine the minimum inductor size, first determine if the device will operate in minimum on-time or minimum off-time mode. The device will operate in minimum on-time mode if Equation 5 is satisfied:

$$V_{IN} - V_{OUT} - I_{OUT} \times r_{DS(on)} - R_L \times I_{OUT} \geq \frac{t_{(OFF,min)} \times \left(V_{OUT} + V_{SCHOTTKY} + R_L \times I_{OUT} \right)}{t_{ON,MIN}}$$

(5)

where R_L = the inductor DC resistance.

Minimum inductor size needed when operating in minimum on-time mode is given by Equation 6:

$$L_{MIN} = \frac{\left(V_{IN} - V_{OUT} - I_{OUT} \times r_{DS(on)} - R_L \times I_{OUT} \right) \times t_{ON,MIN}}{\Delta I_L}$$

(6)

Minimum inductor size needed when operating in minimum off-time mode is given by Equation 7:

$$L_{MIN} = \frac{\left(V_{OUT} + V_{SCHOTTKY} + R_L \times I_{OUT} \right) \times t_{OFF,MIN}}{\Delta I_L}$$

(7)

where ΔI_L = (20%–30%) x $I_{OUT-MAX}$

External PMOS Transistor Selection (Buck Controllers)

The external PMOS transistor is selected based on threshold voltage (V_T), on-resistance ($R_{DS,ON}$), gate capacitance (C_G) and voltage rating. The PMOS V_T magnitude must be much lower than the lowest voltage at IN1 or IN2 that will be used. A V_T magnitude that is 0.5V less than the lowest input voltage is normally sufficient. The PMOS gate will see voltages from 0V to the maximum input voltage, so gate-to-source breakdown should be a few volts higher than the maximum input supply. The drain-to-source of the device will also see this full voltage swing, and should therefore be a few volts higher than the maximum input supply. The RMS current in the PMOS can be estimated by using Equation 8:

$$I_{PMOS(RMS)} \approx I_{OUT} \sqrt{D} = I_{OUT} \sqrt{\frac{V_{OUT}}{V_{IN}}}$$

(8)

The power dissipated in the PMOS is comprised of both conduction and switching losses. Switching losses are typically insignificant. The conduction losses are a function of the RMS current and the $R_{DS,ON}$ of the PMOS, and are calculated by Equation 9:

$$P_{(cond)} = \left(I_{OUT} \sqrt{D} \right)^2 \times r_{DS(on)} \times \left(1 + TC \times \left[T_J - 25°C \right] \right) \approx \left(I_{OUT} \sqrt{D} \right) \times r_{DS(on)}$$

(9)

Diode Selection (Buck Controllers)

The diode is off when the PMOS is on, and on when the PMOS is off. Since it will be turned on and off at a relatively high frequency, a Schottky diode is recommended for good performance. The peak current rating of the diode should exceed the peak current limit set by the sense resistor $R_{IS1,2}$. A diode with low reverse leakage current and low forward voltage at operating current will optimize efficiency. Equation 10 calculates the estimated average power dissipation:

$$I_{(diode)(RMS)} \approx I_{OUT}(1-D) = I_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

(10)

Output Capacitor Selection (Buck Controllers)

The output capacitor is selected based on output voltage ripple and transient response requirements. As a result of the nature of the hysteretic control loop, a minimum ESR of a few tens of mΩ should be maintained for good operation unless a feed-forward resistor is used. Low ESR bulk tantalum or PosCap capacitors work best in most applications. A 1.0μF ceramic capacitor can be used in parallel with this capacitor to filter higher frequency spikes. The output voltage ripple can be estimated by Equation 11:

$$\Delta V_{PP} = \Delta I \times \left[ESR + \left(\frac{1}{8 \times C_{OUT} \times f}\right)\right] \approx 1.1 \Delta I \times ESR$$

(11)

To calculate the capacitance needed to achieve a given voltage ripple as a result of a load transient from zero output to full current, use Equation 12:

$$C_{OUT} = \frac{L \times \Delta I_{OUT}^2}{(V_{IN} - V_{OUT}) \times \Delta V}$$

(12)

If only ceramic or other very low ESR output capacitor configurations are desired, additional voltage ripple must be passed to the feedback pin. See Application Note SLVA210, *Using Ceramic Output Capacitors with the TPS6420x and TPS75003 Buck Controllers*, available for download at www.ti.com, for detailed application information.

Output Voltage Ripple Effect on V$_{OUT}$ (Buck Controllers)

Output voltage ripple causes V_{OUT} to be higher or lower than the target value by half of the peak-to-peak voltage ripple. For minimum on-time, the ripple adds to the voltage; for minimum off-time, it subtracts from the voltage.

Soft-Start Capacitor Selection (Buck Controllers)

The soft-start for BUCK1 and BUCK2 is not intended to be a precision function. However, the startup time (from a positive transition on Enable to V_{OUT} reaching its final value) has a linear relationship to C_{SS} up to approximately 800pF, which results in a startup time of approximately 4ms. Above this value of C_{SS}, the variation in start-up time increases rapidly. This variation can occur from unit to unit and even between the two BUCK controllers in one device. Therefore, do not depend on the soft-start feature for sequencing multiple supplies if values of C_{SS} greater than 800pF are used.

BUCK1 is discussed in this section; it is identical to BUCK2. Soft-start is implemented on the buck controllers by ramping current limit from 0 to its target value (set by R1) over a user-defined time. This time is set by the external soft-start cap connected to pin SS1. If SS1 is left open, a small on-chip capacitor will provide a current limit ramp time of approximately 250μs. Figure 25 shows the effects of R1 and SS1 on the current limit start-up ramp.
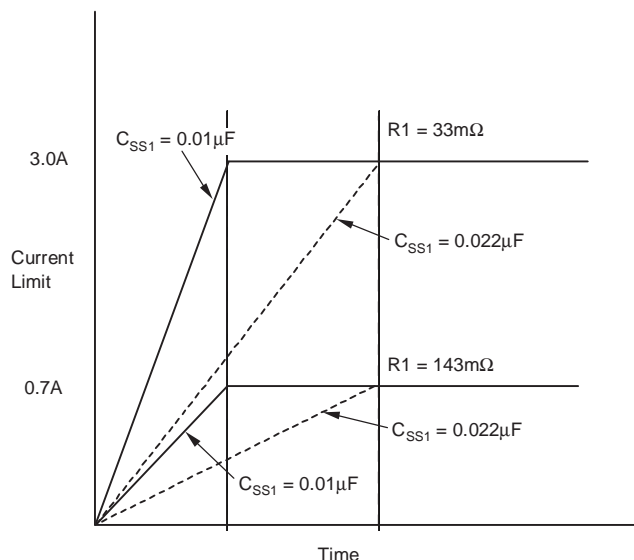
Figure 25. Effects of C_{SS1} and R_1 on Current Ramp Limit

This soft-start current limit ramp can be used to provide inrush current control or output voltage ramp control. While the current limit ramp can be easily understood by looking at Figure 25, the output voltage ramp is a complex function of many variables. The dominant variables in this process are V_{OUT1}, C_{SS1}, I_{OUT1}, and R_1. Less important variables are V_{IN1} and L_1.

The best way to set a target start-up time is through bench measurement under target conditions, adjusting C_{SS1} to get the desired startup profile. To stay above a minimum start-up time, set the nominal start-up time to approximately five times the minimum. To stay below a maximum time, set the nominal start-up time at one-fifth of the maximum. Fastest start-up times occur at maximum V_{IN1}, with minimum V_{OUT1}, L_1, C_{OUT1}, C_{SS1}, and I_{OUT1}. Slowest start-up times occur under opposite conditions.

Refer to Figure 10 to Figure 14 for characterization curves showing how the start-up profile is affected by these critical parameters.

Output Voltage Setting Selection (Buck Controllers)

Output voltage is set using two resistors as shown for Buck2 in Figure 1. Output voltage is then calculated using Equation 13:

$$V_{OUT} = V_{FB}\left(\frac{R_5}{R_6} + 1\right)$$

(13)

where V_{FB} = 1.22V.

LDO OPERATION

The TPS75003 LDO uses a PMOS pass element and is offered in an adjustable version for ease of programming to any output voltage. When used to power $V_{CC,AUX}$ it is set to 2.5V; it can optionally be set to other output voltages to power other circuitry. The LDO has integrated soft-start, independent enable, and short-circuit and thermal protection. The LDO can be used to power $V_{CC,AUX}$ on the Xilinx Spartan-3 FPGA when 3.3V JTAG signals are used as described in Application Note SLVA159 (available for download from www.ti.com).

Input Capacitor Selection (LDO)

Although an input capacitor is not required, it is good analog design practice to connect a 0.1μF to 10μF low ESR capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, stability, and ripple rejection. A higher value capacitor may be needed if large, fast rise-time load transients are anticipated, or if the device is located far from its power source.

Product Folder Link(s): *TPS75003*

Output Capacitor Selection (LDO)

A 2.2μF or greater capacitor is required near the output of the device to ensure stability. The LDO is stable with any capacitor type, including ceramic. If improved transient response or ripple rejection is required, larger and/or lower ESR output capacitors can be used.

Soft-Start (LDO)

The LDO uses an external soft-start capacitor, C_{SS3}, to provide an RC-ramped reference voltage to the control loop. (See the Functional Block Diagram.) This is a voltage-controlled soft-start, as compared to the current-controlled soft-start used by the buck controllers. The start-up waveform can be approximated by Equation 14:

$$V_{OUT}(t) = V_{OUT,SET}\left(1 - e^{-\frac{t}{RC}}\right)$$

(14)

where $R = 480 \times 10^3$ and C = capacitance in μF from SS3 to GND. The time taken to reach 90% of final V_{OUT} can be approximated by Equation 15:

$$T_{90\%} = 2.3 \cdot 480 \times 10^3 \cdot C_{SS3}(\mu F)$$

(15)

Setting Output Voltage (LDO)

Output voltage is set using two resistors as shown in Figure 1. Output voltage is then calculated using Equation 16:

$$V_{OUT} = V_{FB}\left(\frac{R_3}{R_4} + 1\right)$$

(16)

where $V_{FB} = 0.507V$.

Internal Current Limit (LDO)

The internal current limit of the LDO helps protect the regulator during fault conditions. When an over-current condition is detected, the output voltage will be reduced until the current falls to a level that will not damage the device. For good device reliability, the LDO should not operate at current limit.

Enable Pin (LDO)

The active high enable pin (EN3) can be used to put the device into shutdown mode. If shutdown and soft-start capability are not required, EN3 can be tied to IN3.

Dropout Voltage (LDO)

The LDO uses a PMOS transistor to achieve low dropout. When $(V_{IN} - V_{OUT})$ is less than the dropout voltage (V_{DO}), the pass device is in its linear region of operation, and the input-output resistance is the $R_{DS,ON}$ of the pass transistor. In this region, the regulator is said to be out of regulation; ripple rejection, line regulation, and load regulation degrade as $(V_{IN} - V_{OUT})$ falls much below 0.5V.

Transient Response (LDO)

The LDO does not have an on-chip pull-down circuit for output is over-voltage conditions. This feature permits applications that connect higher voltage sources such as an alternate power supply to the output. This design also results in an output overshoot of several percent if the load current quickly drops to zero. The amplitude of overshoot can be reduced by increasing C_{OUT}; the duration of overshoot can be reduced by adding a load resistor.

Thermal Protection (LDO)

Thermal protection disables the output when the junction temperature, T_J, reaches unsafe levels. When the junction cools, the output is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage. For good long term reliability, the device should not be continuously operated at or near thermal shutdown.

Power Dissipation (LDO)

The TPS75003 comes in a QFN-style package with an exposed lead frame on the package underside. The exposed lead frame is the primary path for removing heat and should be soldered to a PC board that is configured to remove the amount of power dissipated by the LDO, as calculated by Equation 17:

$$P_D = (V_{IN3} - V_{OUT3}) \times I_{OUT3} \tag{17}$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to assure the required output voltage. The two buck converters do not contribute a significant amount of dissipated power. Using heavier copper will increase the overall effectiveness of removing heat from the device. The addition of plated through-holes to heat-dissipating layers will also improve the heatsink effectiveness.

PCB Layout Considerations

As with any switching regulators, careful attention must be paid to board layout. A typical application circuit and corresponding recommended printed circuit board (PCB) layout with emphasis on the most sensitive areas are shown in Figure 26 through Figure 28.
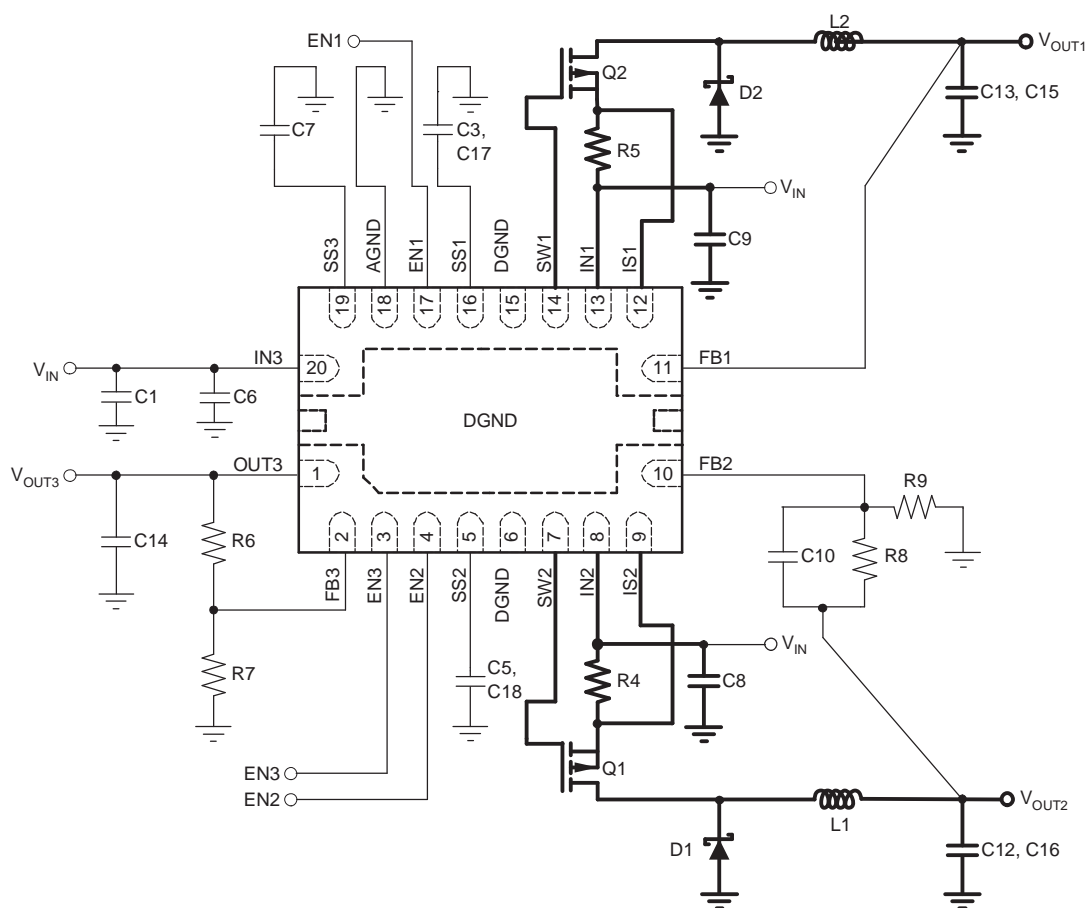
Note: Most sensitive areas are highlighted by bold lines.

Figure 26. Typical Application Circuit

Product Folder Link(s): *TPS75003*
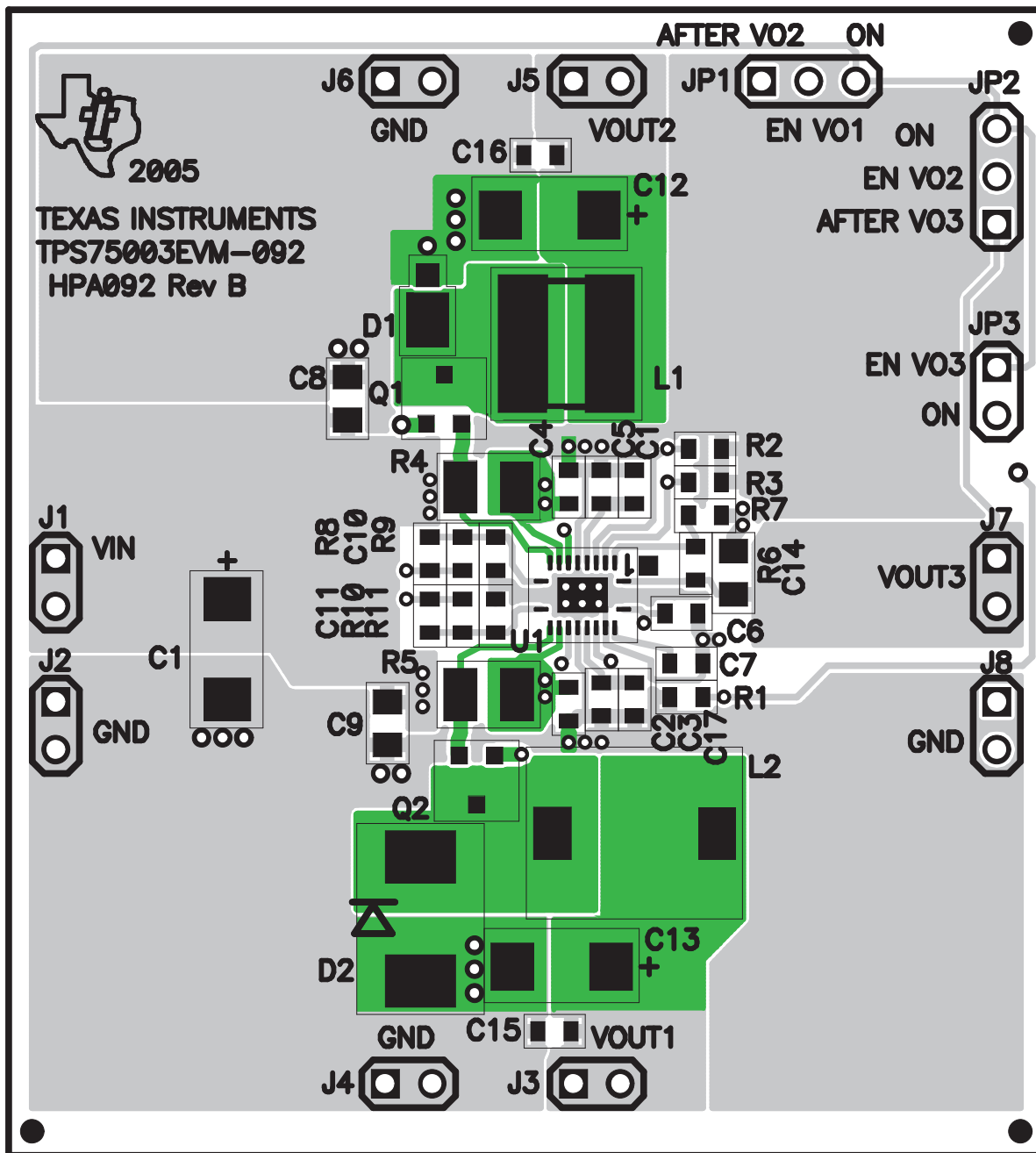
Note: Most sensitive areas are highlighted in green.

Figure 27. Recommended PCB Layout, Component Side, Top View
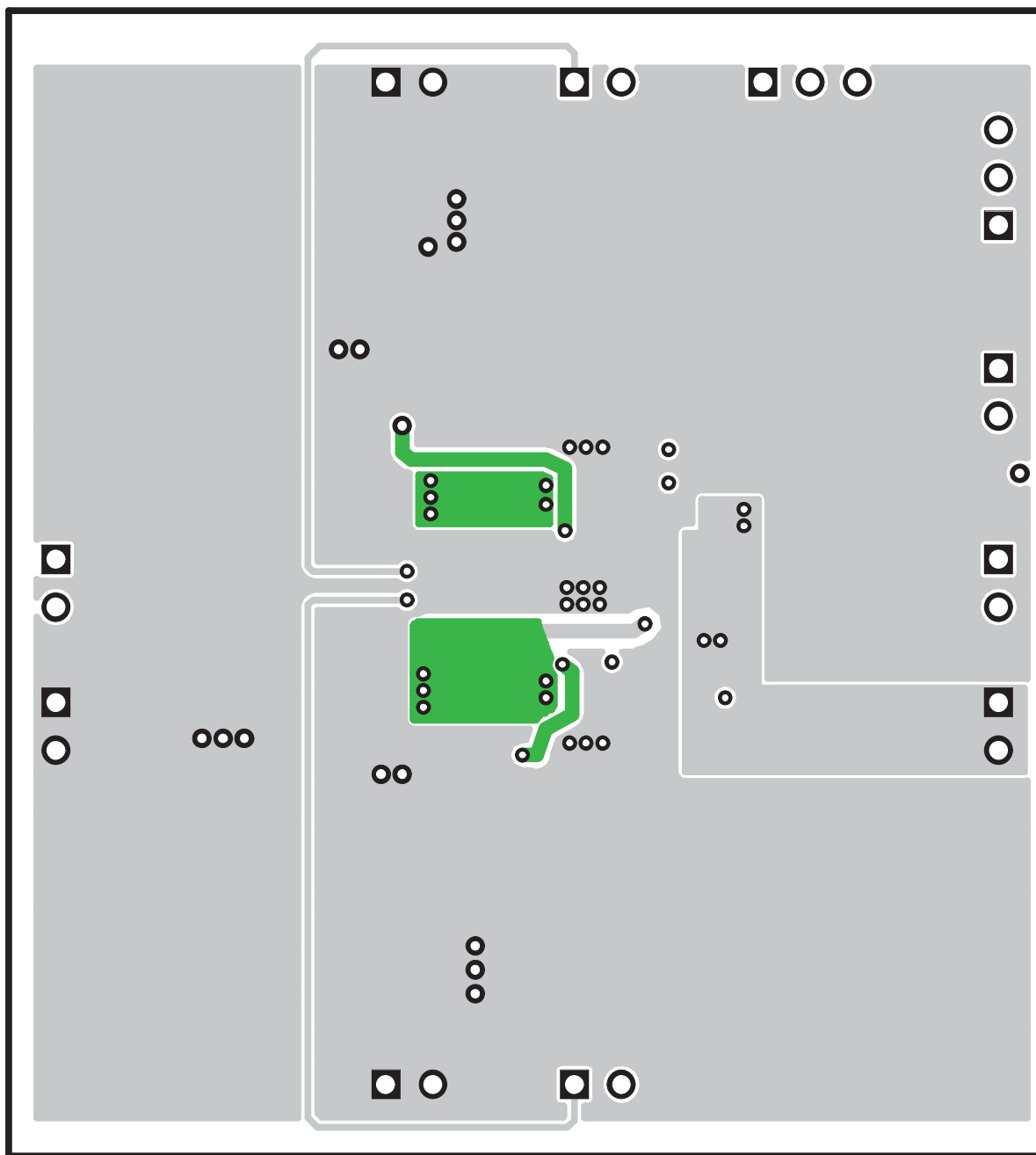
Note: Most sensitive areas are highlighted in green.

Figure 28. Recommended PCB Layout, Bottom Side, Top View

Product Folder Link(s): *TPS75003*

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (August, 2008) to Revision I	Page
• Replaced the *Dissipation Ratings* table with the *Thermal Information* table 2	

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS75003RHLR	ACTIVE	VQFN	RHL	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	75003	Samples
TPS75003RHLRG4	ACTIVE	VQFN	RHL	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	75003	Samples
TPS75003RHLT	ACTIVE	VQFN	RHL	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	75003	Samples
TPS75003RHLTG4	ACTIVE	VQFN	RHL	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	75003	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS75003 :

● Enhanced Product: TPS75003-EP

NOTE: Qualified Version Definitions:

● Enhanced Product - Supports Defense, Aerospace and Medical Applications

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

K0 — P1

B0 — W

Cavity — A0

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

| Q1 | Q2 | | Q1 | Q2 |
| Q3 | Q4 | | Q3 | Q4 |

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS75003RHLR	VQFN	RHL	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
TPS75003RHLT	VQFN	RHL	20	250	180.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS75003RHLR	VQFN	RHL	20	3000	367.0	367.0	35.0
TPS75003RHLT	VQFN	RHL	20	250	210.0	185.0	35.0
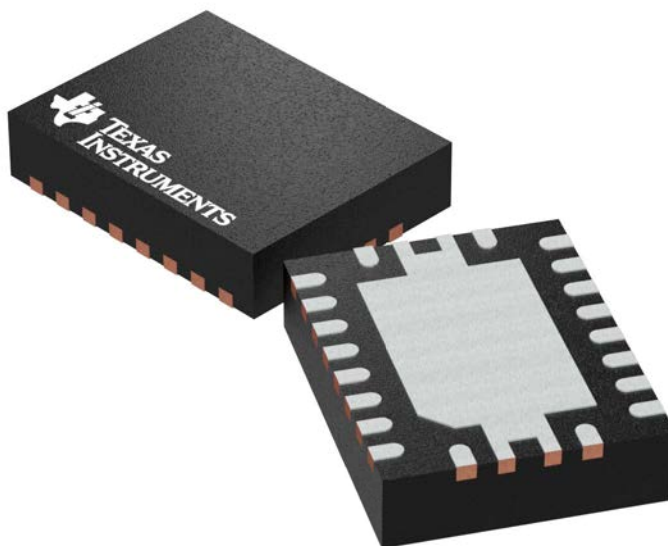
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4205346/L

B

3.6
3.4

A

PIN 1 INDEX AREA

4.6
4.4

C

1 MAX

SEATING PLANE

0.08 | C

2.05±0.1

2X 1.5

SYMM

20X 0.5 / 0.3

14X 0.5

10

11

9

12

(0.2) TYP

2X 3.5

SYMM

21

3.05±0.1

2

19

PIN 1 ID
(OPTIONAL)

1

20

20X 0.29 / 0.19

4X (0.2)

0.1 M | C | A | B
0.05 M | C

2X (0.55)

4219071 / A   05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

TEXAS INSTRUMENTS
www.ti.com

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 18X

SOLDER MASK DETAILS

4219071 / A   05/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to theri locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
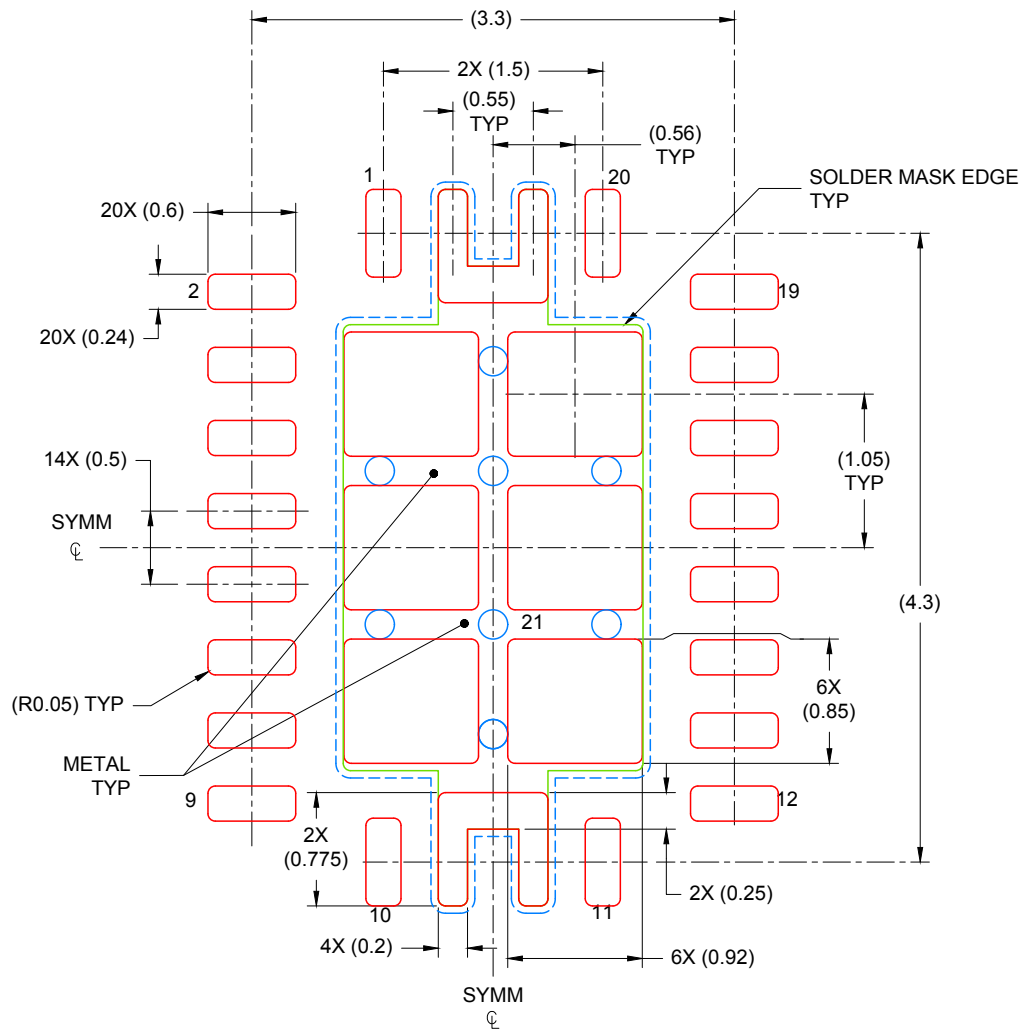
SOLDER PASTE EXAMPLE
BASED ON 0.1mm THICK STENCIL

EXPOSED PAD
75% PRINTED COVERAGE BY AREA
SCALE: 20X

4219071 / A   05/2017

NOTES: (continued)

7.   Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..