UCC2813-0/-1/-2/-3/-4/-5-Q1
LOW-POWER BICMOS CURRENT-MODE PWM

SGLS245D − MAY 2004 − REVISED APRIL 2008

- **Qualified for Automotive Applications**
- **ESD Protection Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **100-μA Typical Starting Supply Current**
- **500-μA Typical Operating Supply Current**
- **Operation to 1 MHz**
- **Internal Soft Start**
- **Internal Fault Soft Start**
- **Internal Leading-Edge Blanking of the Current Sense Signal**
- **1-A Totem-Pole Output**
- **70-ns Typical Response From Current-Sense to Gate Drive Output**
- **1.5% Tolerance Voltage Reference**
- **Same Pinout as UC3802, UC3842, and UC3842A**

description

The UCC2813-0/-1/-2/-3/-4/-5 family of high-speed low-power integrated circuits contain all of the control and drive components required for off-line and dc-to-dc fixed-frequency current-mode switching power supplies with minimal parts count.

These devices have the same pin configuration as the UC2842/3/4/5 family and also offer the added features of internal full-cycle soft start and internal leading-edge blanking of the current-sense input.

The UCC2813-0/-1/-2/-3/-4/-5 family offers choice of maximum duty cycle and critical voltage levels. Lower reference parts, such as the UCC2813-3 and UCC2813-5, fit best into battery-operated systems, while the higher reference and the higher undervoltage lockout (UVLO) hysteresis of the UCC2813-2 and UCC2813-4 make these ideal choices for use in off-line power supplies.

The UCC2813-x series is specified for the automotive temperature range of −40°C to 125°C.

PART NUMBER	MAXIMUM DUTY CYCLE	REFERENCE VOLTAGE	TURN-ON THRESHOLD	TURN-OFF THRESHOLD
UCC2813-0	100%	5 V	7.2 V	6.9 V
UCC2813-1	50%	5 V	9.4 V	7.4 V
UCC2813-2	100%	5 V	12.5 V	8.3 V
UCC2813-3	100%	4 V	4.1 V	3.6 V
UCC2813-4	50%	5 V	12.5 V	8.3 V
UCC2813-5	50%	4 V	4.1 V	3.6 V

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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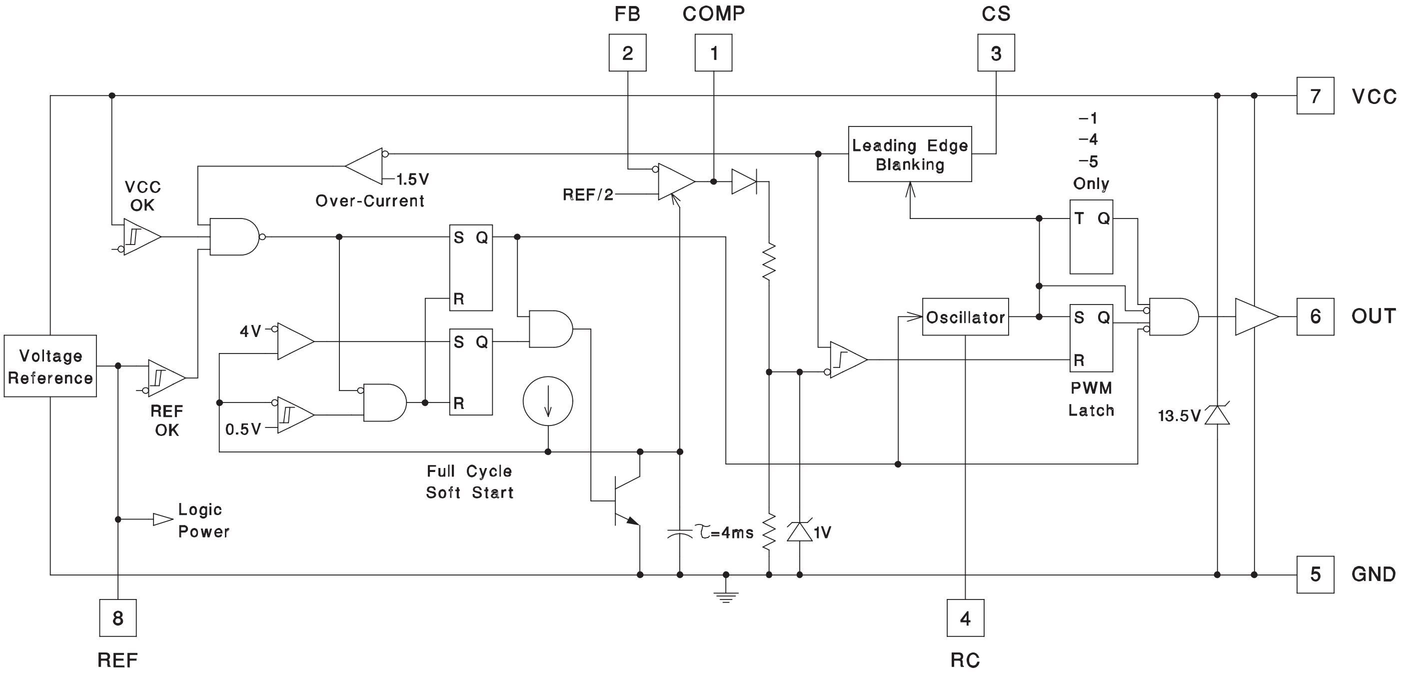
block diagram



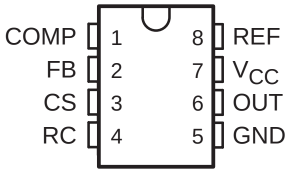
AVAILABLE OPTIONS†‡

T_A	ORDERABLE PART NUMBER
−40°C to 125°C	UCC2813QDR-0Q1
	UCC2813QDR-1Q1
	UCC2813QDR-2Q1
	UCC2813QDR-3Q1
	UCC2813QDR-4Q1
	UCC2813QDR-5Q1
	UCC2813QPWR-3Q1

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

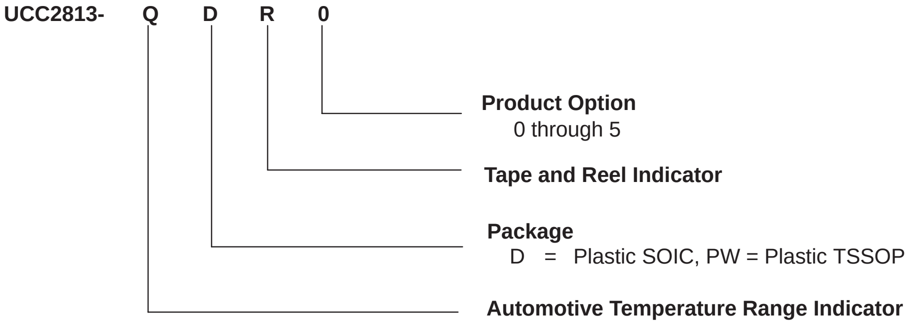
‡ Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

D PACKAGE
(TOP VIEW)



TSSOP-8 PW PACKAGE
(TOP VIEW)

ordering information



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†‡

V_{CC} voltage §	12 V
V_{CC} current §	30 mA
Output current, I_O	±1 A
Output energy (capacitive load)	20 μJ
Analog inputs (FB, CS)	−0.3 V to 6.3 V
Power dissipation at $T_A < +25°C$ (D package)	0.65 W
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds	300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Unless otherwise indicated, voltages are reference to ground and currents are positive into and negative out of the specified terminals.

§ In normal operation V_{CC} is powered through a current limiting resistor. Absolute maximum of 12 V applies when V_{CC} is driven from a low impedance source such that I_{CC} does not exceed 30 mA (which includes gate drive current requirement).

electrical characteristics $T_A = -40°C$ to 125°C, $V_{CC} = 10$ V (see Note 1), RT = 100 kΩ from REF to RC, CT = 330 pF from RC to GND, 0.1-F capacitor from V_{CC} to GND, 0.1-F capacitor from V_{REF} to GND, and $T_A = T_J$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Reference Section						
Output voltage	$T_J = 25°C$, I = 0.2 mA	UCC2813-0/-1/-2/-4	4.925	5	5.075	V
		UCC2813-3/-5	3.94	4	4.06	
Load regulation voltage	I = 0.2 mA to 5 mA			10	30	mV
Total variation voltage	See Note 5	UCC2813-0/-1/-2/-4	4.84	5	5.1	V
		UCC2813-3/-5	3.84	4	4.08	
Output noise voltage	f = 10 Hz to 10 kHz, See Note 7	$T_J = 25°C$		70		μV
Long term stability	1000 hours, See Note 7	$T_A = 125°C$		5		mV
Output short-circuit current			−5		−35	mA

electrical characteristics T_A = −40°C to 125°C, V_{CC} = 10 V (see Note 1), RT = 100 kΩ from REF to RC, CT = 330 pF from RC to GND, 0.1 F capacitor from V_{CC} to GND, 0.1 F capacitor from V_{REF} to GND and T_A = T_J (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Oscillator Section						
Oscillator frequency	See Note 2	UCC2813-0/-1/-2/-4	40	46	52	kHz
		UCC2813-3/-5	26	31	36	
Temperature stability	See Note 7			2.5		%
Amplitude, peak to peak			2.25	2.4	2.55	V
Oscillator peak voltage				2.45		V
Error Amplifier Section						
Input voltage	COMP = 2.5 V	UCC2813-0/-1/-2/-4	2.42	2.5	2.56	V
	COMP = 2.0 V	UCC2813-3/-5	1.92	2	2.05	
Input bias current			−2		2	µA
Open loop voltage gain			60	80		dB
COMP sink current	FB = 2.7 V,	COMP = 1.1 V	0.3		3.5	mA
COMP source current	FB = 1.8 V,	COMP = REF − 1.2 V	−0.2	−0.5	−0.8	mA
Gain bandwidth product	See Note 7			2		MHz
PWM Section						
Maximum duty cycle		UCC2813-0/-2/-3	97	99	100	%
		UCC2813-1/-4/-5	48	49	50	
Minimum duty cycle	COMP = 0 V				0	%
Current Sense Section						
Gain	See Note 3		1.1	1.65	1.8	V/V
Maximum input signal	COMP = 5 V,	See Note 4	0.9	1	1.1	V
Input bias current			−200		200	nA
CS blank time			50	100	150	ns
Over-current threshold voltage			1.32	1.55	1.7	V
COMP to CS offset voltage	CS = 0 V		0.45	0.9	1.35	V
Output Section (OUT)						
Low-level output voltage	I_{OUT} = 20 mA	All parts		0.1	0.4	V
	I_{OUT} = 200 mA	All parts		0.35	0.9	
	I_{OUT} = 50 mA, V_{CC} = 5 V	UCC2813-3/-5		0.15	0.4	
	I_{OUT} = 20 mA, V_{CC} = 0 V	All parts		0.7	1.2	
High-level output voltage, V_{SAT} (V_{CC} − OUT)	I_{OUT} = −20 mA	All parts		0.15	0.4	V
	I_{OUT} = −200 mA	All parts		1	1.9	
	I_{OUT} = −50 mA, V_{CC} = 5 V	UCC2813-3/-5		0.4	0.9	
Rise time	C_L = 1 nF			41	70	ns
Fall time	C_L = 1 nF			44	75	ns

electrical characteristics T_A = −40°C to 125°C, V_{CC} = 10 V (see Note 1), RT = 100 kΩ from REF to RC, CT = 330 pF from RC to GND, 0.1 F capacitor from V_{CC} to GND, 0.1 F capacitor from V_{REF} to GND, and T_A = T_J (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Undervoltage Lockout Section						
Start threshold	See Note 6	UCC2813-0	6.6	7.2	7.8	V
		UCC2813-1	8.6	9.4	10.2	
		UCC2813-2/-4	11.5	12.5	13.5	
		UCC2813-3/-5	3.7	4.1	4.5	
Stop threshold	See Note 6	UCC2813-0	6.3	6.9	7.5	V
		UCC2813-1	6.8	7.4	8	
		UCC2813-2/-4	7.6	8.3	9	
		UCC2813-3/-5	3.2	3.6	4	
Start to stop hysteresis		UCC2813-0	0.12	0.3	0.48	V
		UCC2813-1	1.6	2	2.4	
		UCC2813-2/-4	3.5	4.2	5.1	
		UCC2813-3/-5	0.2	0.5	0.8	
Soft-Start Section						
COMP rise time	FB = 1.8 V,	Rise from 0.5 V to REF − 1 V		4	10	ms
Overall						
Start-up current	V_{CC} < Start hreshold			0.1	0.23	mA
Operating supply current	FB = 0 V,	CS = 0 V, RC = 0 V		0.5	1.2	mA
V_{CC} internal zener voltage	I_{CC} = 10 mA,	See Notes 6 and 8	12	13.5	15	V
V_{CC} internal zener voltage minus start threshold voltage	See Note 6	UCC2813-2/-4	0.5	1.0		V

NOTES:
1. Adjust V_{CC} above the start threshold before setting at 10 V.
2. Oscillator frequency for the UCC2813-0, UCC2813-2, and UCC2813-3 is the output frequency.
   Oscillator frequency for the UCC2813-1, UCC2813-4, and UCC2813-5 is twice the output frequency.
3. Gain is defined by: $A = \frac{\Delta V_{COMP}}{\Delta V_{CS}}$ $0 \le V_{CS} \le 0.8$ V.
4. Parameter measured at trip point of latch with pin 2 at 0 V.
5. Total variation includes temperature stability and load regulation.
6. Start threshold, stop threshold, and Zener shunt thresholds track one another.
7. Not production tested
8. The device is fully operating in clamp mode as the forcing current is higher than the normal operating supply current.

detailed terminal descriptions

COMP

COMP is the output of the error amplifier and the input of the PWM comparator.

Unlike other devices, the error amplifier in the UCC2813 family is a true, low output-impedance, 2-MHz operational amplifier. As such, the COMP terminal can both source and sink current. However, the error amplifier is internally current limited, so that one can command zero duty cycle by externally forcing COMP to GND.

The UCC2813 family features built-in full-cycle soft start. Soft start is implemented as a clamp on the maximum COMP voltage.

CS

CS is the input to the current sense comparators. The UCC2813 family has two different current sense comparators: the PWM comparator and an overcurrent comparator.

The UCC2813 family contains digital current sense filtering, which disconnects the CS terminal from the current sense comparator during the 100 ns interval immediately following the rising edge of the OUT pin. This digital filtering, also called leading-edge blanking, means that in most applications, no analog filtering (RC filter) is required on CS. Compared to an external RC filter technique, the leading-edge blanking provides a smaller effective CS to OUT propagation delay. Note, however, that the minimum non-zero on time of the OUT signal is directly affected by the leading-edge blanking and the CS to OUT propagation delay.

The overcurrent comparator is only intended for fault sensing, and exceeding the overcurrent threshold causes a soft start cycle.

FB

FB is the inverting input of the error amplifier. For best stability, keep FB lead length as short as possible and FB stray capacitance as small as possible.

GND

GND is reference ground and power ground for all functions on this part.

OUT

OUT is the output of a high-current power driver capable of driving the gate of a power MOSFET with peak currents exceeding ±750 mA. OUT is actively held low when V_{CC} is below the UVLO threshold.

The high-current power driver consists of FET output devices, which can switch all of the way to GND and all of the way to V_{CC}. The output stage also provides a low impedance to overshoot and undershoot. This means that, in many cases, external Schottky clamp diodes are not required.

detailed descriptions (continued)

RC

RC is the oscillator timing pin. For fixed frequency operation, set timing capacitor charging current by connecting a resistor from REF to RC. Set frequency by connecting timing capacitor from RC to GND. For best perfomance, keep the timing capacitor lead to GND as short and direct as possible. If possible, use separate ground traces for the timing capacitor and all other functions.

The frequency of oscillation can be estimated with the following equations:

$$\text{UCC2813−0/1/2/4}: \; F = \frac{1.5}{R \times C}$$

$$\text{UCC2813−3/UCC2813−5}: \; F = \frac{1.0}{R \times C} \qquad (1)$$

where frequency is in Hz, resistance is in ohms, and capacitance is in farads. The recommended range of the timing resistors is between 10 kΩ and 200 kΩ and the timing capacitor is 100 pF to 1000 pF. Never use a timing resistor less than 10 k.

To prevent noise problems, bypass V_{CC} to GND with a ceramic capacitor as close to the V_{CC} pin as possible. An electrolytic capacitor may also be used in addition to the ceramic capacitor.

voltage reference (REF)

REF is the voltage reference for the error amplifier and also for many other functions on the IC. REF is also used as the logic power supply for high-speed switching logic on the IC.

When V_{CC} is greater than 1 V and less than the UVLO threshold, REF is pulled to ground through a 5-kΩ resistor. This means that REF can be used as a logic output indicating power system status. It is important for reference stability that REF is bypassed to GND with a ceramic capacitor as close to the pin as possible. An electrolytic capacitor may also be used in addition to the ceramic capacitor. A minimum of 0.1-µF ceramic capacitor is required. Additional REF bypassing is required for external loads greater than 2.5 mA on the reference.

To prevent noise problems with high-speed switching transients, bypass REF to ground with a ceramic capacitor close to the IC package.

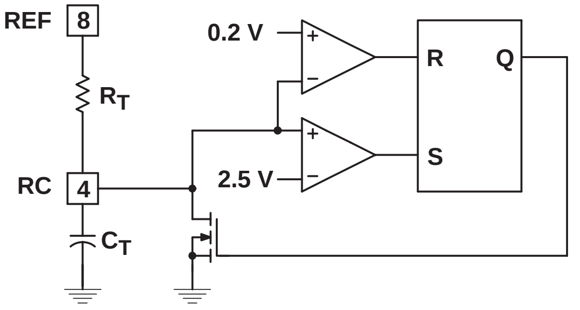
power (V_{CC})

V_{CC} is the power input connection for this device. In normal operation, V_{CC} is powered through a current-limiting resistor. Although quiescent V_{CC} current is low, total supply current will be higher, depending on OUT current. Total V_{CC} current is the sum of quiescent V_{CC} current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Q_g), average OUT current can be calculated from:

$$I_{OUT} = Q_g \times F. \qquad (2)$$

PARAMETER MEASUREMENT INFORMATION

Oscillator



The UCC2813-0/-1/-2/-3/-4/-5 oscillator generates a sawtooth waveform on RC. The rise time is set by the time constant of RT and CT. The fall time is set by CT and an internal transistor on-resistance of approximately 125. During the fall time, the output is off and the maximum duty cycle is reduced below 50% or 100% depending on the part number. Larger timing capacitors increase the discharge time and reduce the maximum duty cycle and frequency.

Figure 1

Error Amplifier Gain/Phase Response

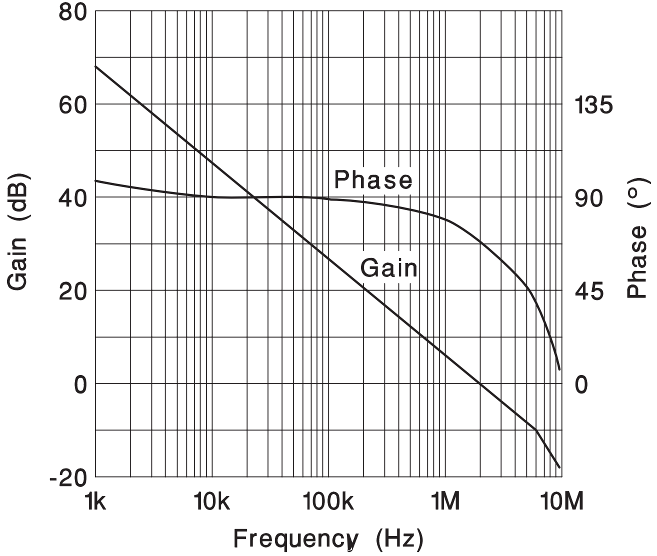


Figure 2

UCC2813-3/5 V_{REF} vs V_{CC}

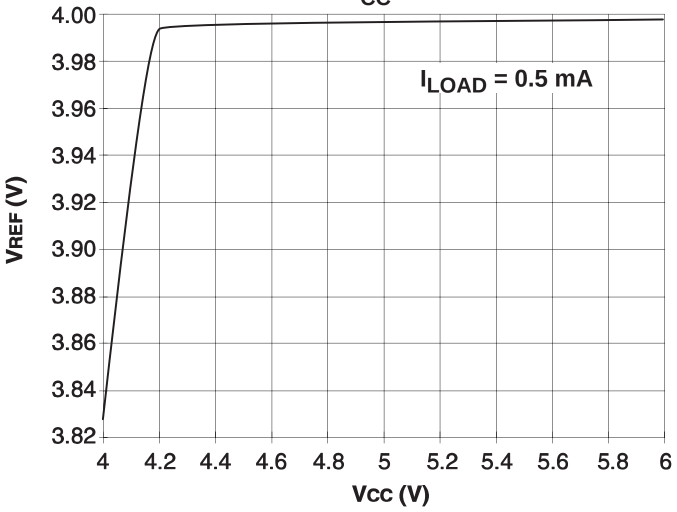


Figure 3

UCC2813-0/1/2/4 Oscillator Frequency vs R_T and C_T

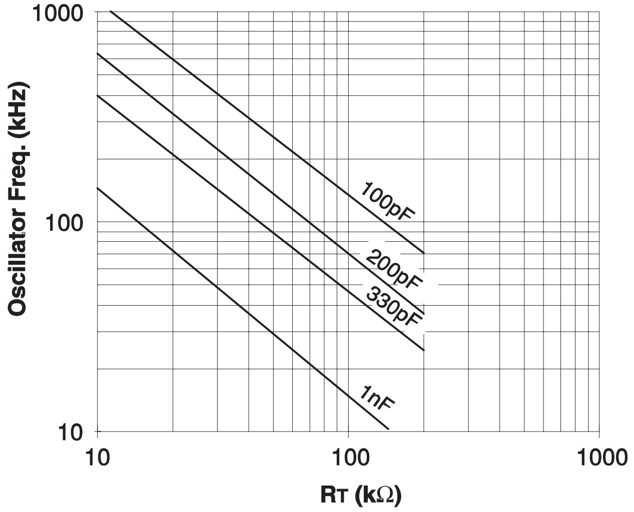


Figure 4

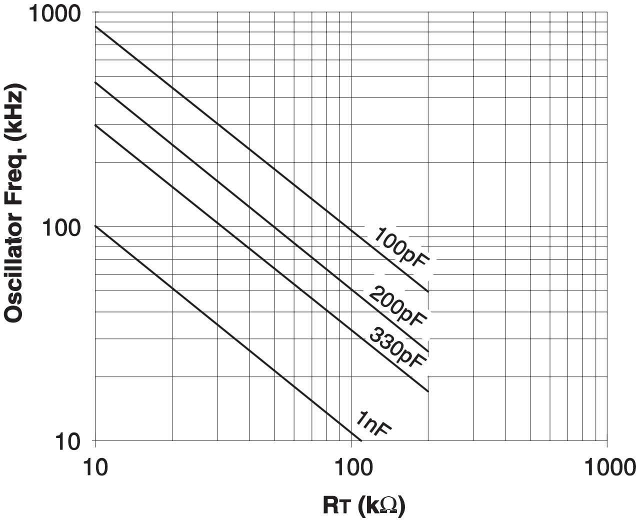

UCC2813-3/5 Oscillator Frequency vs R_T and C_T

Figure 5

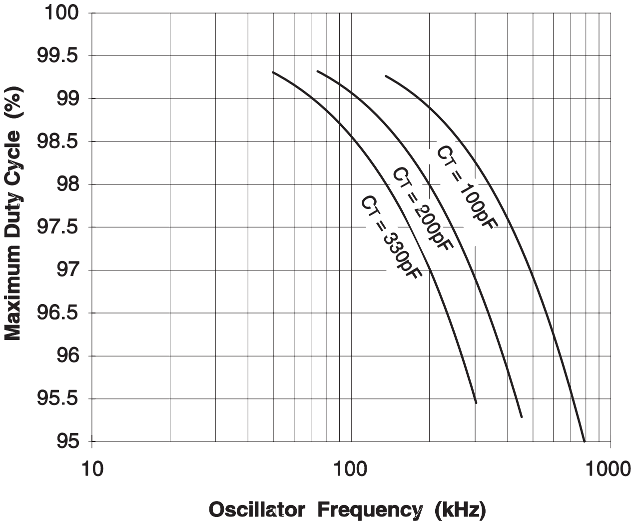

UCC2813-0/2/3 Maximum Duty Cycle vs Oscillator Frequency

Figure 6

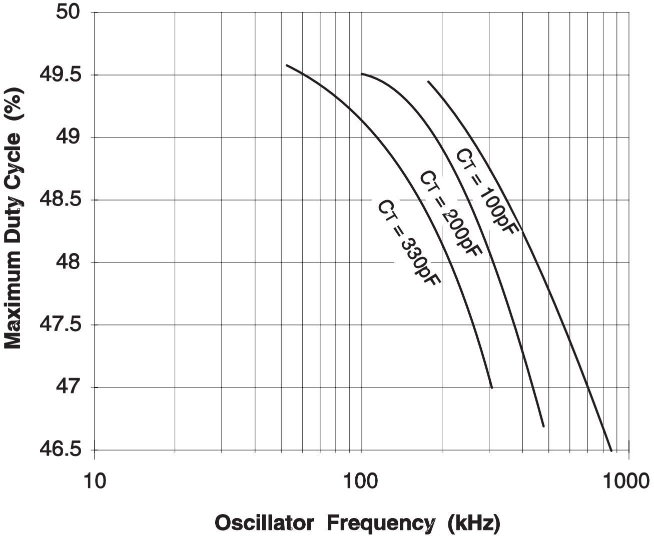

UCC2813-1/4/5 Maximum Duty Cycle vs Oscillator Frequency

Figure 7

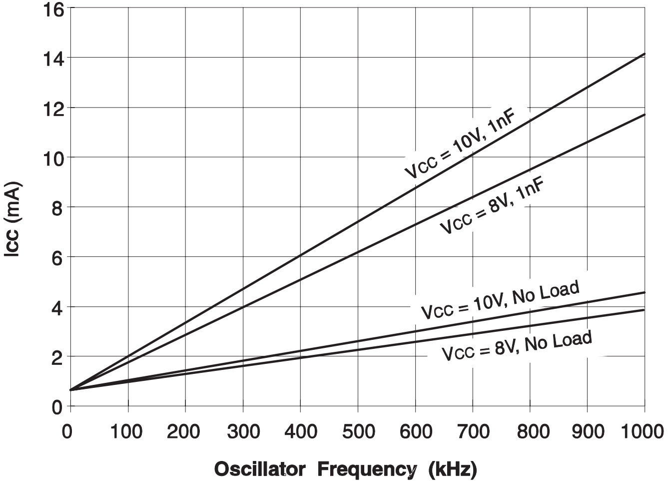

UCC2813-0 I_{CC} vs Oscillator Frequency

Figure 8

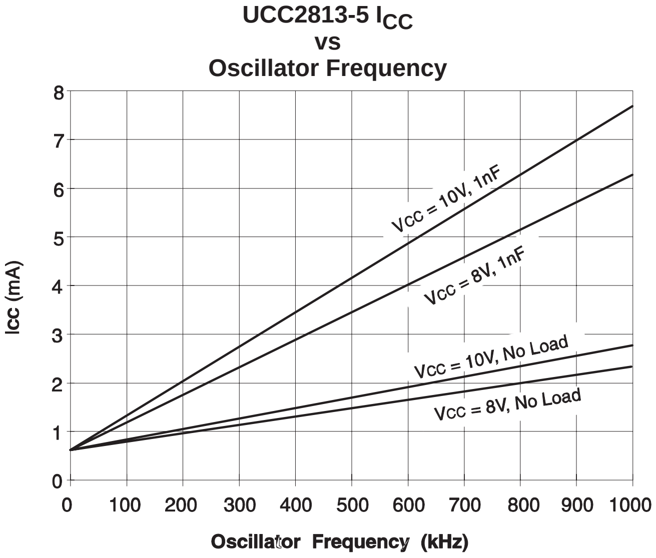


Figure 9

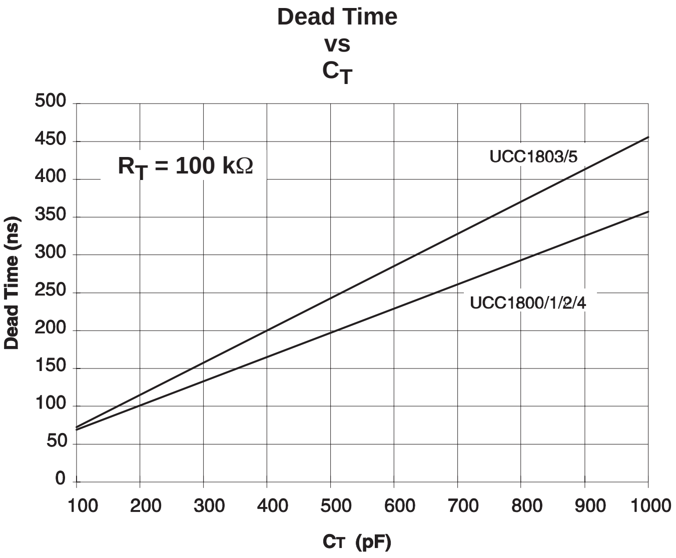


Figure 10

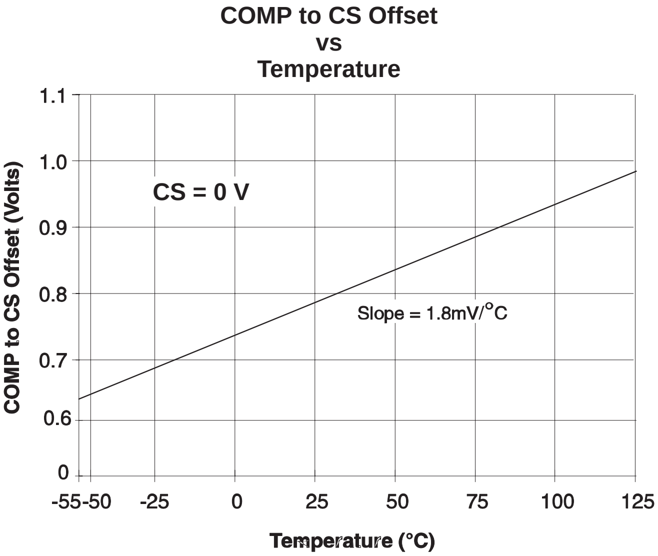


Figure 11

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC2813QDR-0Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2813-0 ~ 2813-0Q1)	Samples
UCC2813QDR-1Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2813-1 ~ 2813-1Q1)	Samples
UCC2813QDR-2Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2813-2 ~ 2813-2Q1)	Samples
UCC2813QDR-3Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2813-3 ~ 2813-3Q1)	Samples
UCC2813QDR-4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2813-4 ~ 2813-4Q1)	Samples
UCC2813QDR-5Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2813-5 ~ 2813-5Q1)	Samples
UCC2813QPWR-3Q1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	28133Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UCC2813-0-Q1, UCC2813-1-Q1, UCC2813-2-Q1, UCC2813-3-Q1, UCC2813-4-Q1, UCC2813-5-Q1 :

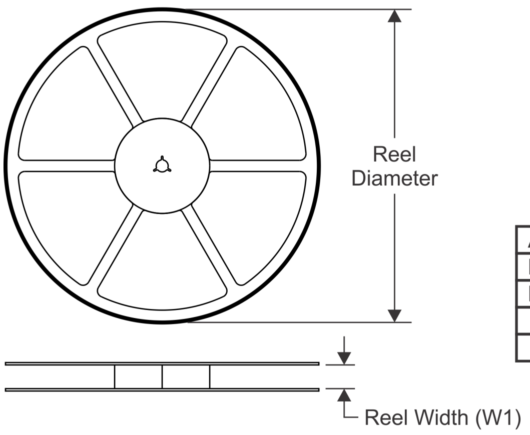
- Catalog: UCC2813-0, UCC2813-1, UCC2813-2, UCC2813-3, UCC2813-4, UCC2813-5

NOTE: Qualified Version Definitions:

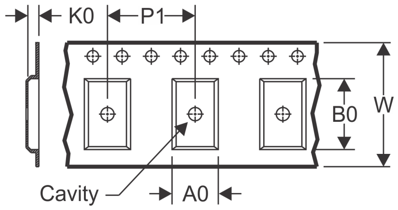
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

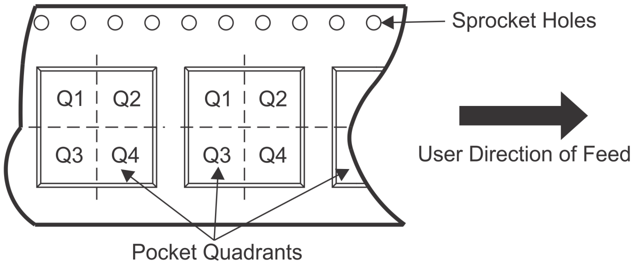


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

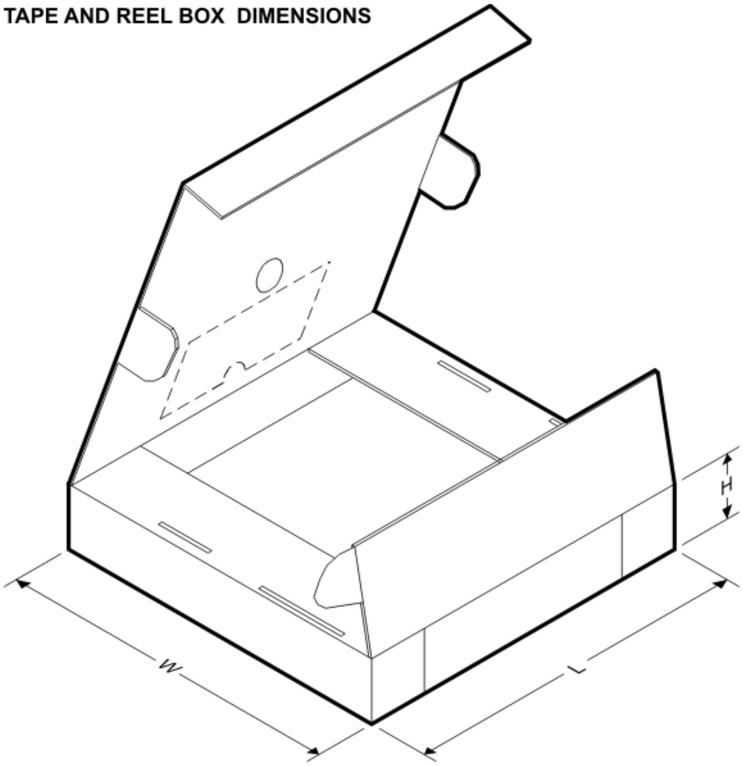
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2813QDR-0Q1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2813QDR-1Q1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2813QDR-2Q1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2813QDR-3Q1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2813QDR-4Q1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2813QDR-5Q1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2813QPWR-3Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

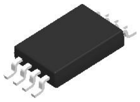
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2813QDR-0Q1	SOIC	D	8	2500	367.0	367.0	35.0
UCC2813QDR-1Q1	SOIC	D	8	2500	367.0	367.0	35.0
UCC2813QDR-2Q1	SOIC	D	8	2500	367.0	367.0	35.0
UCC2813QDR-3Q1	SOIC	D	8	2500	367.0	367.0	35.0
UCC2813QDR-4Q1	SOIC	D	8	2500	367.0	367.0	35.0
UCC2813QDR-5Q1	SOIC	D	8	2500	367.0	367.0	35.0
UCC2813QPWR-3Q1	TSSOP	PW	8	2000	367.0	367.0	35.0

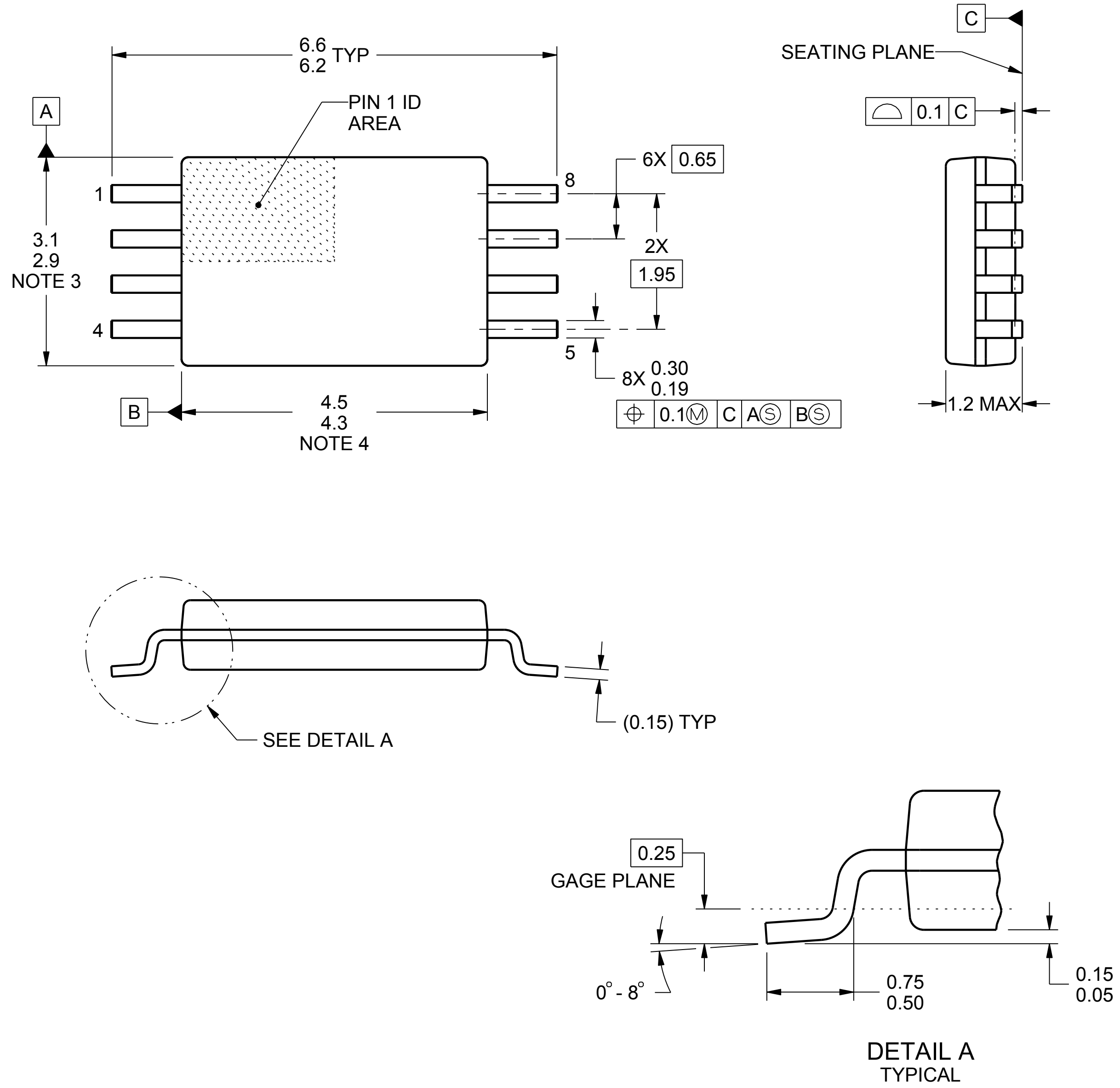
PW0008A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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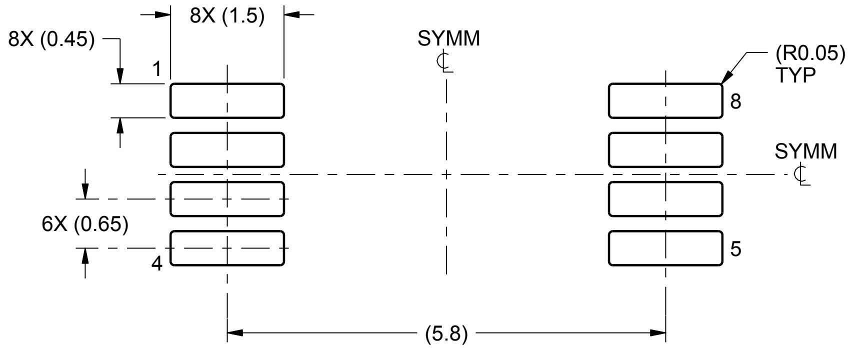
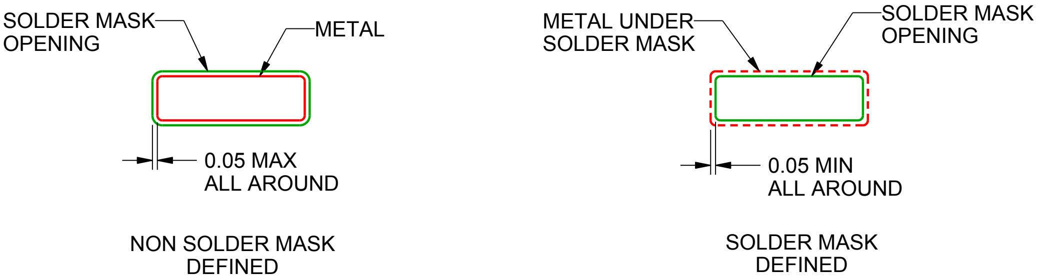
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



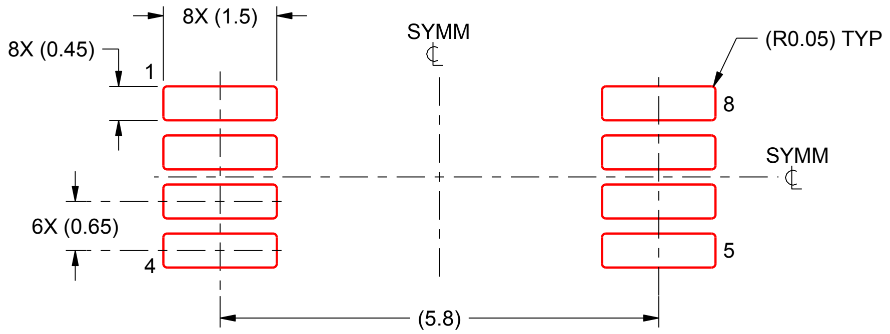
LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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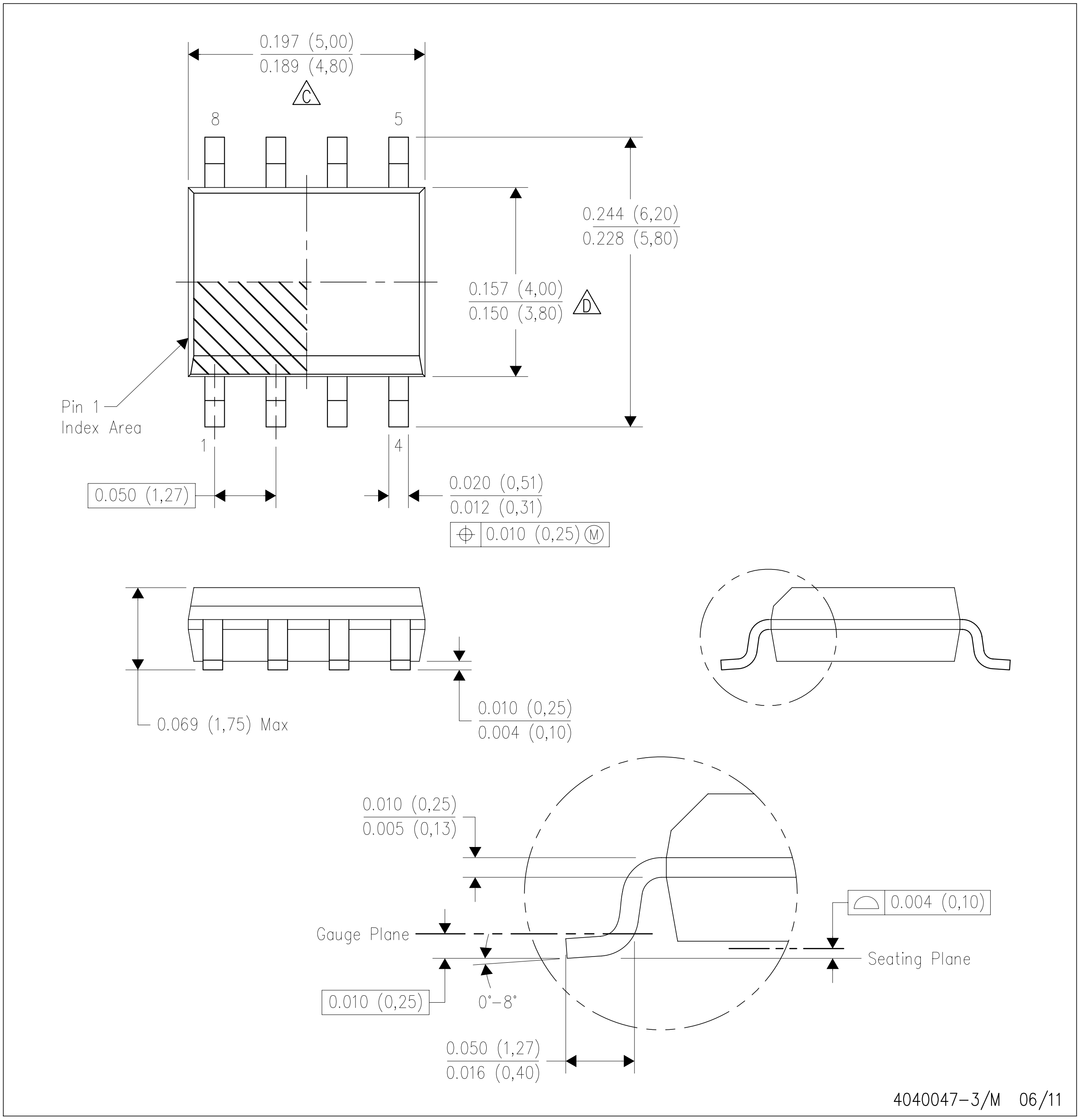
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

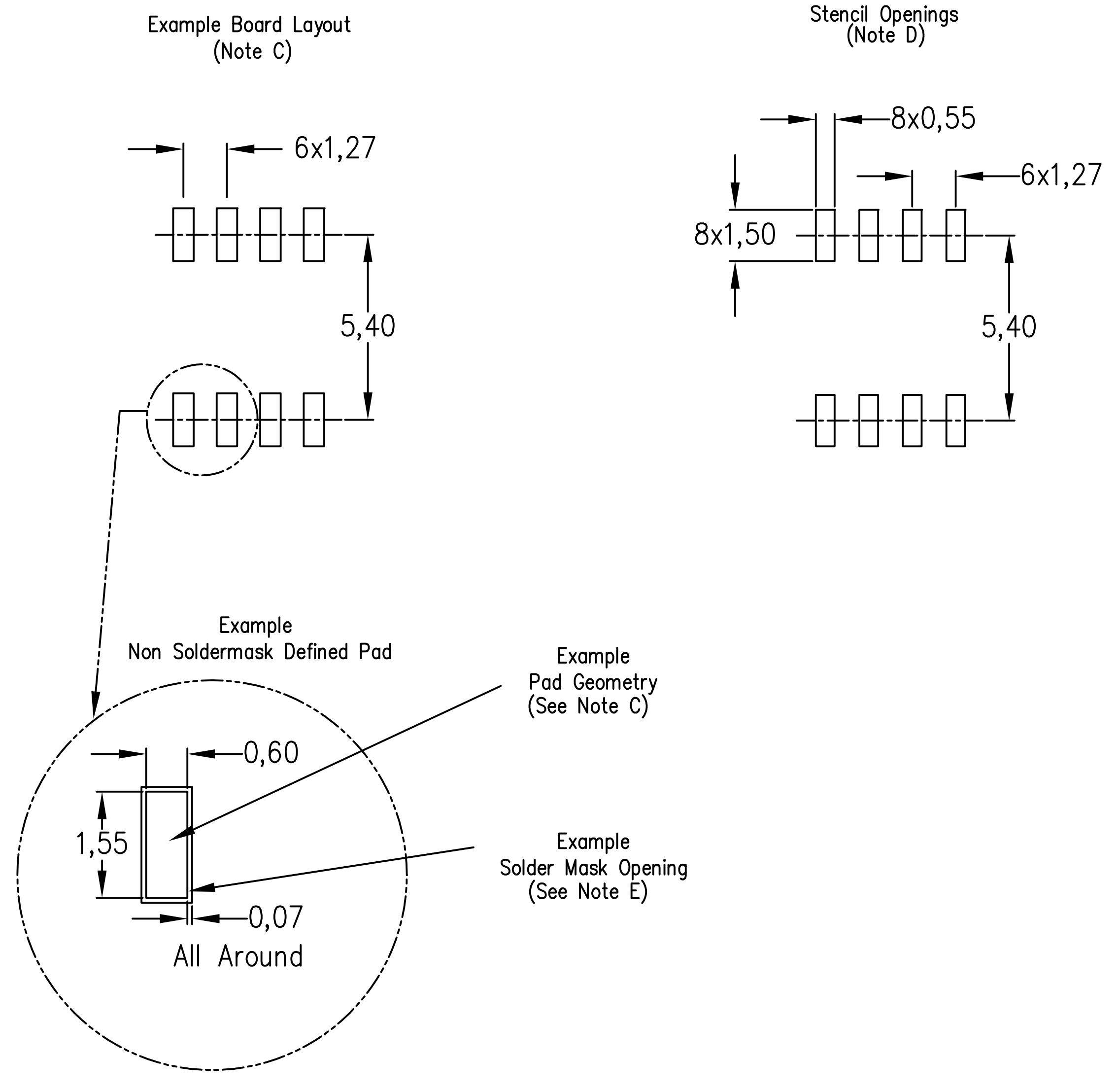
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



4211283-2/E 08/12

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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