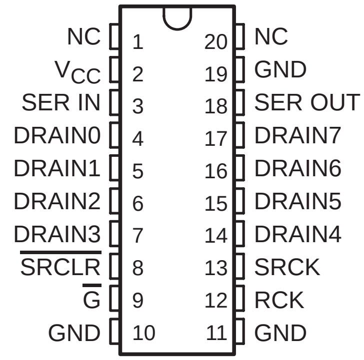
- **Low $r_{DS(on)}$ . . . 5 Ω**
- **Avalanche Energy . . . 30 mJ**
- **Eight Power DMOS-Transistor Outputs of 150-mA Continuous Current**
- **500-mA Typical Current-Limiting Capability**
- **Output Clamp Voltage . . . 50 V**
- **Enhanced Cascading for Multiple Stages**
- **All Registers Cleared With Single Input**
- **Low Power Consumption**

**DW OR N PACKAGE**
**(TOP VIEW)**



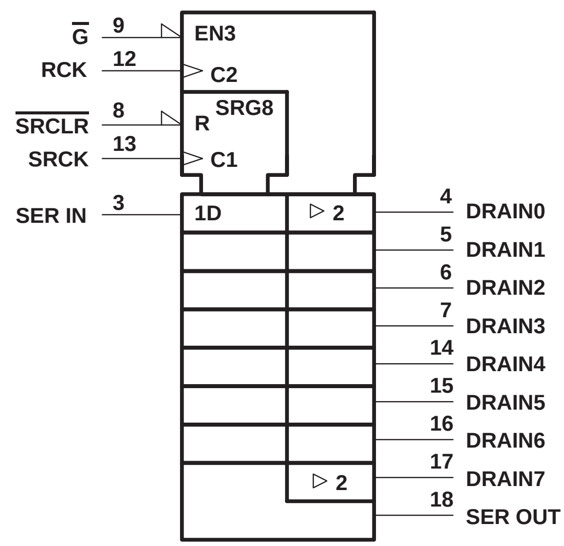

NC − No internal connection

## description

The TPIC6B596 is a monolithic, high-voltage, medium-current power 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift-register clear ($\overline{\text{SRCLR}}$) is high. When $\overline{\text{SRCLR}}$ is low, all registers in the device are cleared. When output enable ($\overline{\text{G}}$) is held high, all data in the output buffers is held low and all drain outputs are off. When $\overline{\text{G}}$ is held low, data from the storage register is transparent to the output buffers. When data in the output buffers is low, the DMOS-transistor outputs are off. When data is high, the DMOS-transistor outputs have sink-current capability. The serial output (SER OUT) is clocked out of the device on the falling edge of SRCK to provide additional hold time for cascaded applications. This will provide improved performance for applications where clock signals may be skewed, devices are not located near one another, or the system must tolerate electromagnetic interference.

**logic symbol†**




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Outputs are low-side, open-drain DMOS transistors with output ratings of 50 V and 150-mA continuous sink-current capability. Each output provides a 500-mA typical current limit at $T_C$ = 25°C. The current limit decreases as the junction temperature increases for additional device protection.

The TPIC6B596 is characterized for operation over the operating case temperature range of −40°C to 125°C.



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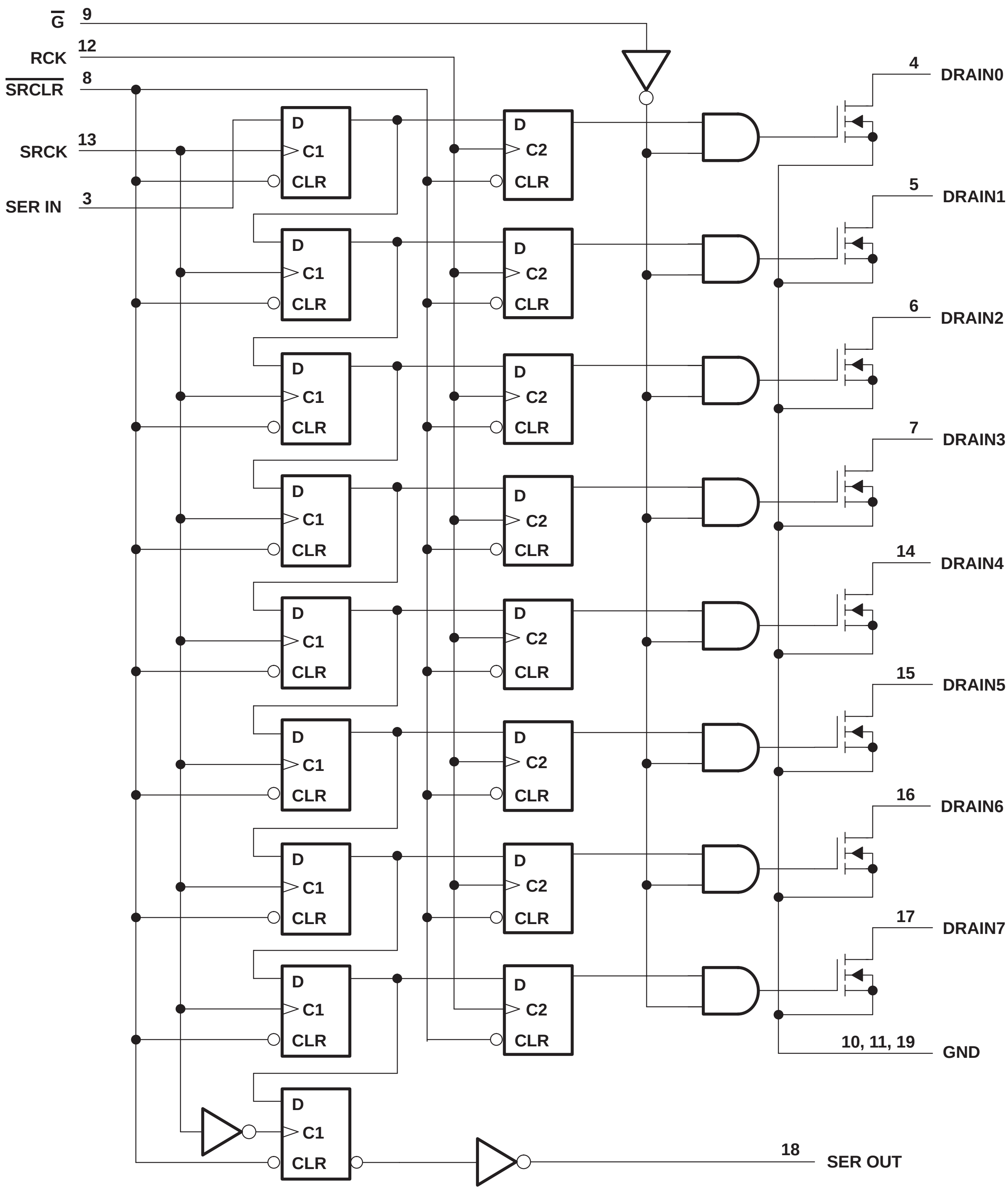
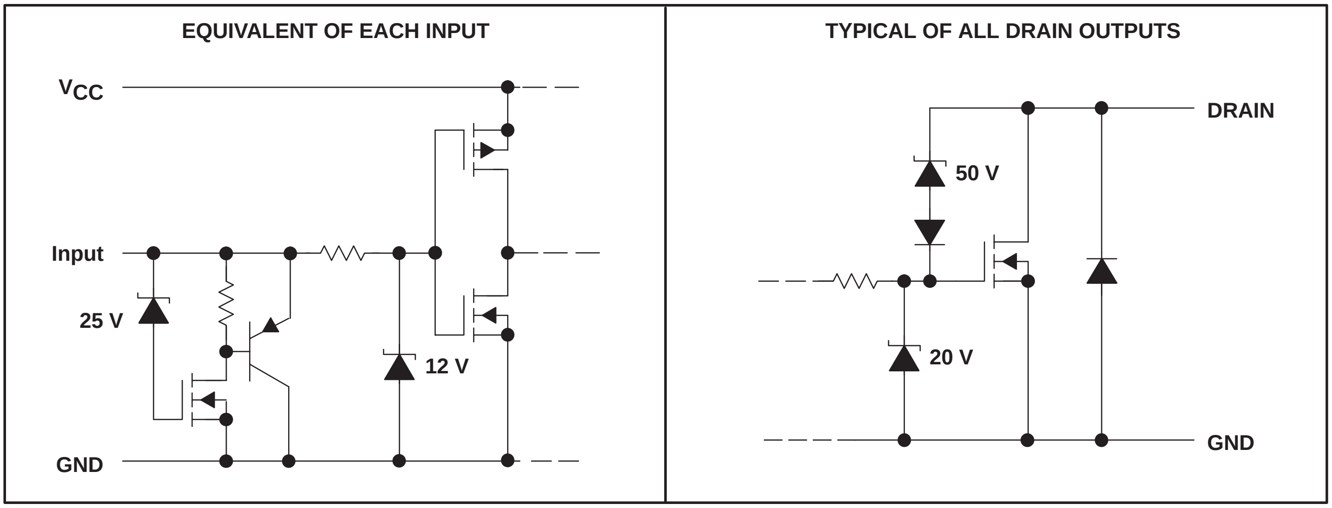
SLIS095A − MARCH 2000 − REVISED MAY 2005

## logic diagram (positive logic)



## schematic of inputs and outputs




## absolute maximum ratings over recommended operating case temperature range (unless otherwise noted)†

| | |
|---|---|
| Logic supply voltage, $V_{CC}$ (see Note 1) | 7 V |
| Logic input voltage range, $V_I$ | −0.3 V to 7 V |
| Power DMOS drain-to-source voltage, $V_{DS}$ (see Note 2) | 50 V |
| Continuous source-to-drain diode anode current | 500 mA |
| Pulsed source-to-drain diode anode current (see Note 3) | 1 A |
| Pulsed drain current, each output, all outputs on, $I_D$, $T_C$ = 25°C (see Note 3) | 500 mA |
| Continuous drain current, each output, all outputs on, $I_D$, $T_C$ = 25°C | 150 mA |
| Peak drain current single output, $I_{DM}$,$T_C$ = 25°C (see Note 3) | 500 mA |
| Single-pulse avalanche energy, $E_{AS}$ (see Figure 4) | 30 mJ |
| Avalanche current, $I_{AS}$ (see Note 4) | 500 mA |
| Continuous total dissipation | See Dissipation Rating Table |
| Operating virtual junction temperature range, $T_J$ | −40°C to 150°C |
| Operating case temperature range, $T_C$ | −40°C to 125°C |
| Storage temperature range | −65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. Each power DMOS source is internally connected to GND.
3. Pulse duration ≤ 100 µs and duty cycle ≤ 2%.
4. DRAIN supply voltage = 15 V, starting junction temperature ($T_{JS}$) = 25°C, L = 200 mH, $I_{AS}$ = 0.5 A (see Figure 4).

**DISSIPATION RATING TABLE**

| PACKAGE | $T_C \le 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_C$ = 25°C | $T_C$ = 125°C POWER RATING |
|---|---|---|---|
| DW | 1389 mW | 11.1 mW/°C | 278 mW |
| N | 1050 mW | 10.5 mW/°C | 263 mW |

## recommended operating conditions

| | MIN | MAX | UNIT |
|---|---|---|---|
| Logic supply voltage, $V_{CC}$ | 4.5 | 5.5 | V |
| High-level input voltage, $V_{IH}$ | 0.85 $V_{CC}$ | | V |
| Low-level input voltage, $V_{IL}$ | | 0.15 $V_{CC}$ | V |
| Pulsed drain output current, $T_C$ = 25°C, $V_{CC}$ = 5 V (see Notes 3 and 5) | −500 | 500 | mA |
| Setup time, SER IN high before SRCK↑, $t_{su}$ (see Figure 2) | 15 | | ns |
| Hold time, SER IN high after SRCK↑, $t_h$ (see Figure 2) | 15 | | ns |
| Pulse duration, $t_w$ (see Figure 2) | 40 | | ns |
| Operating case temperature, $T_C$ | −40 | 125 | °C |

NOTES: 3. Pulse duration ≤ 100 µs and duty cycle ≤ 2%.
5. Technique should limit $T_J - T_C$ to 10°C maximum.

## electrical characteristics, $V_{CC}$ = 5 V, $T_C$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{(BR)DSX}$ | Drain-to-source breakdown voltage | $I_D$ = 1 mA | | 50 | | | V |
| $V_{SD}$ | Source-to-drain diode forward voltage | $I_F$ = 100 mA | | | 0.85 | 1 | V |
| $V_{OH}$ | High-level output voltage, SER OUT | $I_{OH}$ = −20 µA, $V_{CC}$ = 4.5 V | | 4.4 | 4.49 | | V |
| | | $I_{OH}$ = −4 mA, $V_{CC}$ = 4.5 V | | 4 | 4.2 | | |
| $V_{OL}$ | Low-level output voltage, SER OUT | $I_{OL}$ = 20 µA, $V_{CC}$ = 4.5 V | | | 0.005 | 0.1 | V |
| | | $I_{OL}$ = 4 mA, $V_{CC}$ = 4.5 V | | | 0.3 | 0.5 | |
| $I_{IH}$ | High-level input current | $V_{CC}$ = 5.5 V, $V_I = V_{CC}$ | | | | 1 | µA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = 5.5 V, $V_I$ = 0 | | | | −1 | µA |
| $I_{CC}$ | Logic supply current | $V_{CC}$ = 5.5 V | All outputs off | | 20 | 100 | µA |
| | | | All outputs on | | 150 | 300 | |
| $I_{CC(FRQ)}$ | Logic supply current at frequency | $f_{SRCK}$ = 5 MHz, $C_L$ = 30 pF, All outputs off, See Figures 2 and 6 | | | 0.4 | 5 | mA |
| $I_N$ | Nominal current | $V_{DS(on)}$ = 0.5 V, $I_N = I_D$, $T_C$ = 85°C | See Notes 5, 6, and 7 | | 90 | | mA |
| $I_{DSX}$ | Off-state drain current | $V_{DS}$ = 40 V, $V_{CC}$ = 5.5 V | | | 0.1 | 5 | µA |
| | | $V_{DS}$ = 40 V, $V_{CC}$ = 5.5 V, $T_C$ = 125°C | | | 0.15 | 8 | |
| $r_{DS(on)}$ | Static drain-source on-state resistance | $I_D$ = 100 mA, $V_{CC}$ = 4.5 V | See Notes 5 and 6 and Figures 7 and 8 | | 4.2 | 5.7 | Ω |
| | | $I_D$ = 100 mA, $T_C$ = 125°C, $V_{CC}$ = 4.5 V | | | 6.8 | 9.5 | |
| | | $I_D$ = 350 mA, $V_{CC}$ = 4.5 V | | | 5.5 | 8 | |

NOTES: 5. Technique should limit $T_J - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at $T_C$ = 85°C.

## switching characteristics, $V_{CC}$ = 5 V, $T_C$ = 25°C

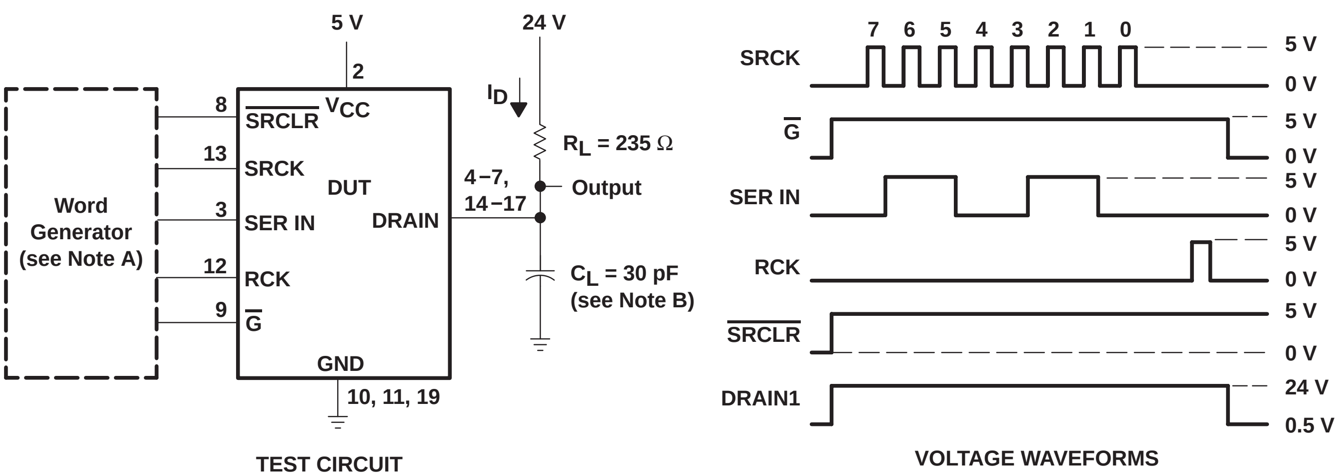
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output from $\overline{G}$ | $C_L$ = 30 pF, $I_D$ = 100 mA, See Figures 1, 2, and 9 | | 150 | | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output from $\overline{G}$ | | | 90 | | ns |
| $t_r$ | Rise time, drain output | | | 200 | | ns |
| $t_f$ | Fall time, drain output | | | 200 | | ns |
| $t_{pd}$ | Propagation delay time, SRCK↓ to SEROUT | $C_L$ = 30 pF, $I_D$ = 100 mA, See Figure 2 | | 15 | | ns |
| $f_{(SRCK)}$ | Serial clock frequency | $C_L$ = 30 pF, $I_D$ = 100 mA, See Note 8 | | | 10 | MHz |
| $t_a$ | Reverse-recovery-current rise time | $I_F$ = 100 mA, di/dt = 20 A/µs, See Notes 5 and 6 and Figure 3 | | 100 | | ns |
| $t_{rr}$ | Reverse-recovery time | | | 300 | | |

NOTES: 5. Technique should limit $T_J - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
8. This is the maximum serial clock frequency assuming cascaded operation where serial data is passed from one stage to a second stage. The clock period allows for SRCK → SEROUT propagation delay and setup time plus some timing margin.

## thermal resistance

| PARAMETER | | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal resistance, junction-to-ambient | DW package | All 8 outputs with equal power | | 90 | °C/W |
| | | N package | | | 95 | |

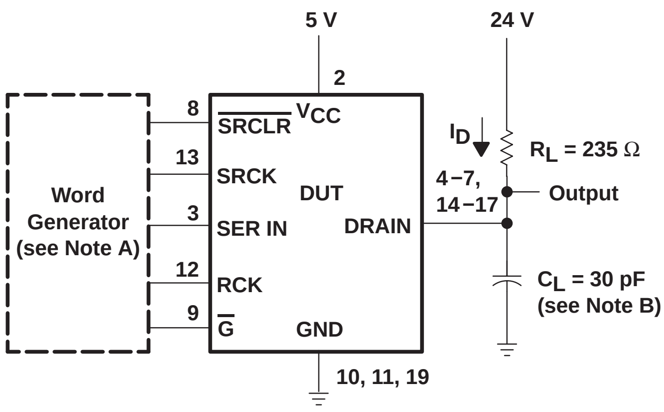
## PARAMETER MEASUREMENT INFORMATION



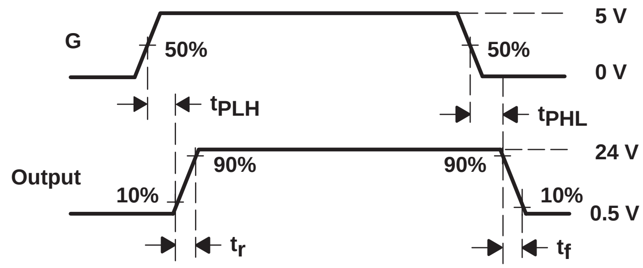

NOTES: A. The word generator has the following characteristics: $t_r \leq$ 10 ns, $t_f \leq$ 10 ns, $t_W$ = 300 ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O$ = 50 Ω.
B. $C_L$ includes probe and jig capacitance.

**Figure 1. Resistive-Load Test Circuit and Voltage Waveforms**

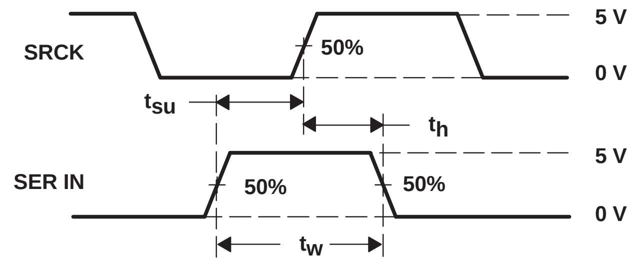
## PARAMETER MEASUREMENT INFORMATION



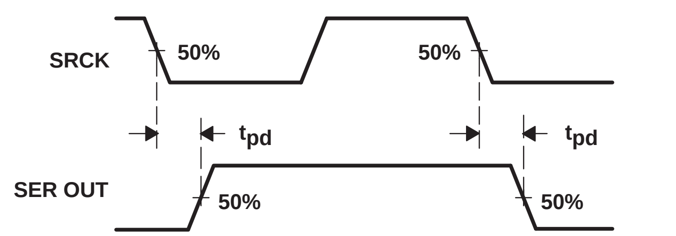

TEST CIRCUIT




SWITCHING TIMES




INPUT SETUP AND HOLD WAVEFORMS

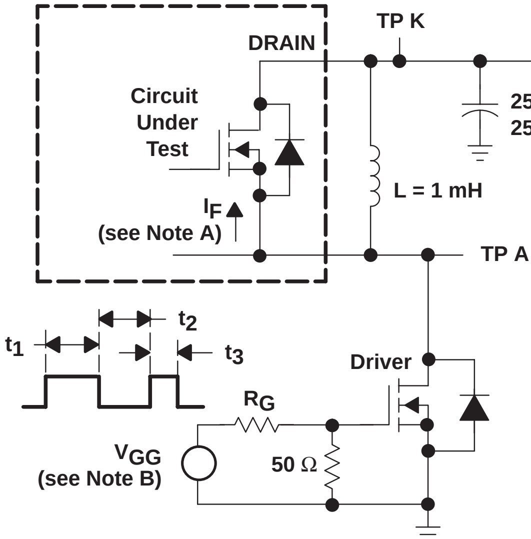



SER OUT PROPAGATION DELAY WAVEFORM

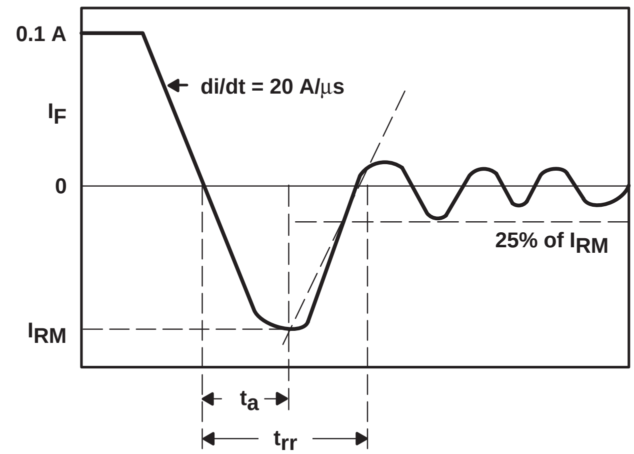
NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_W = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. $C_L$ includes probe and jig capacitance.

**Figure 2. Test Circuit, Switching Times, and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT

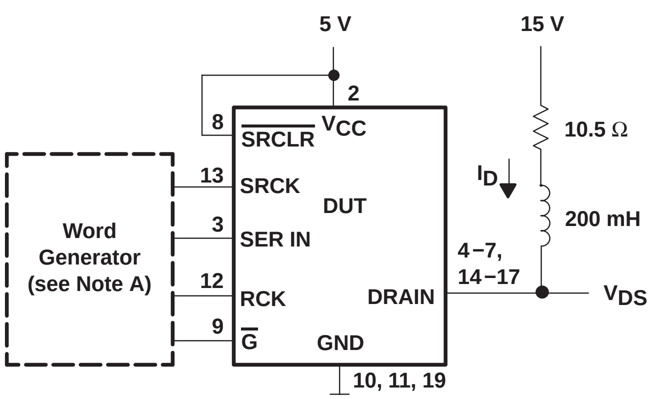



CURRENT WAVEFORM

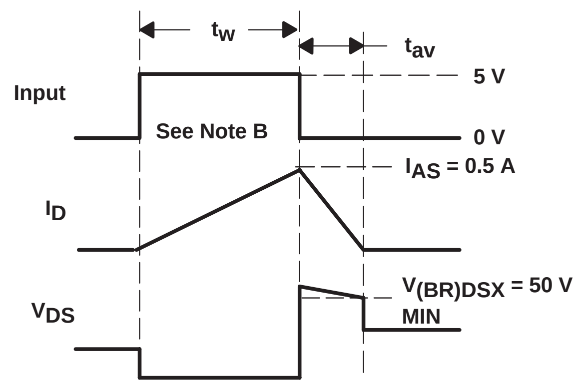
NOTES: A. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

B. The $V_{GG}$ amplitude and $R_G$ are adjusted for di/dt = 20 A/μs. A $V_{GG}$ double-pulse train is used to set $I_F$ = 0.1 A, where $t_1$ = 10 μs, $t_2$ = 7 μs, and $t_3$ = 3 μs.

**Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-to-Drain Diode**




SINGLE-PULSE AVALANCHE ENERGY TEST CIRCUIT




VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration, $t_w$, is increased until peak current $I_{AS}$ = 0.5 A.
Energy test level is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2$ = 30 mJ.

**Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms**

## TYPICAL CHARACTERISTICS

### PEAK AVALANCHE CURRENT vs TIME DURATION OF AVALANCHE

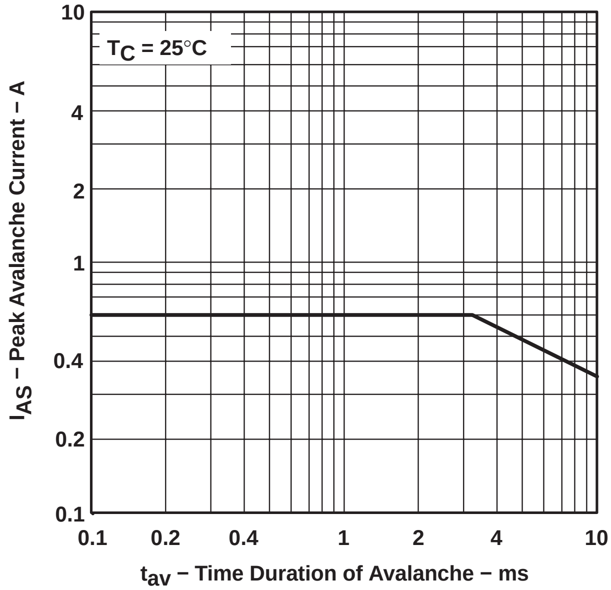



Figure 5

### SUPPLY CURRENT vs FREQUENCY

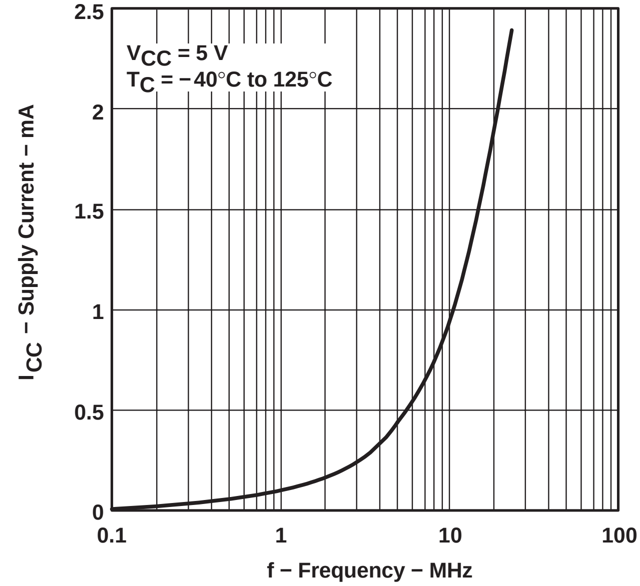



Figure 6

### DRAIN-TO-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

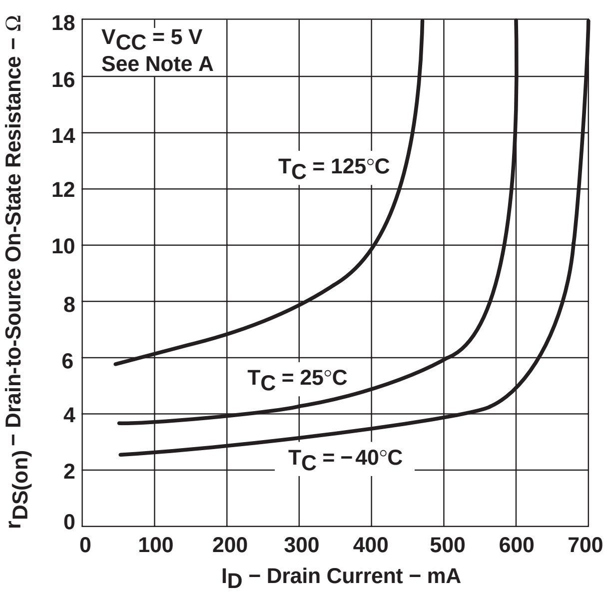



Figure 7

### STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs LOGIC SUPPLY VOLTAGE

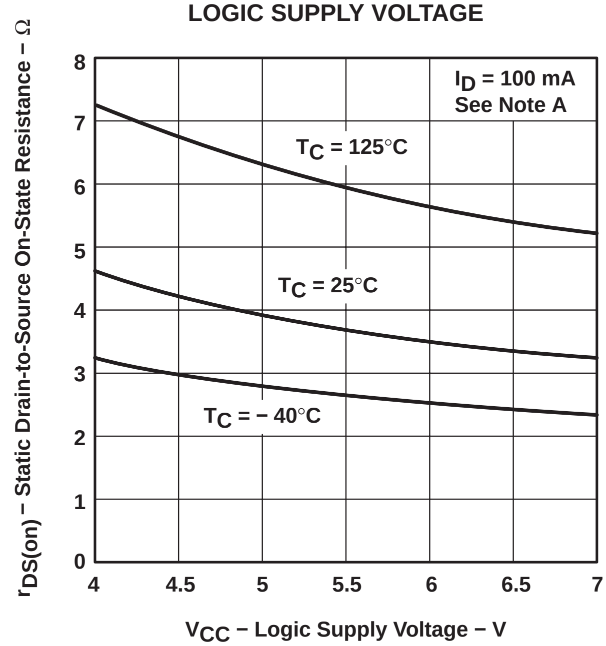



Figure 8

## TYPICAL CHARACTERISTICS

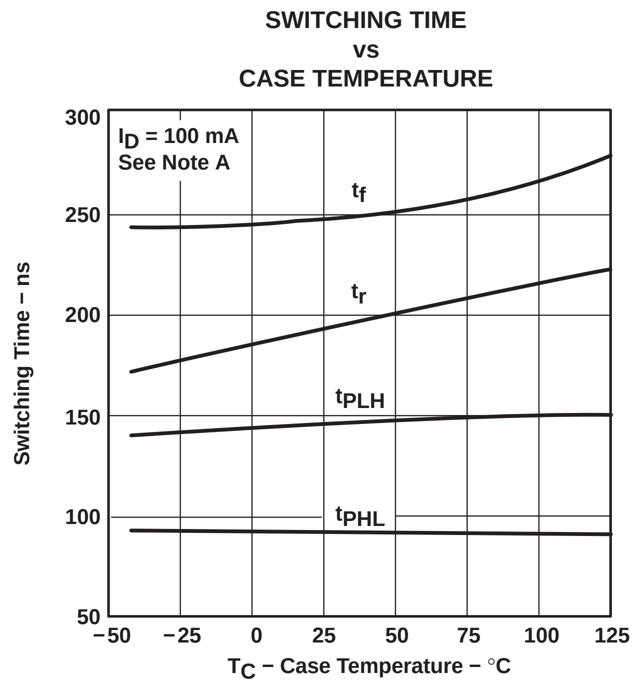



**Figure 9**

NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

## THERMAL INFORMATION

**MAXIMUM CONTINUOUS DRAIN CURRENT OF EACH OUTPUT vs NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY**

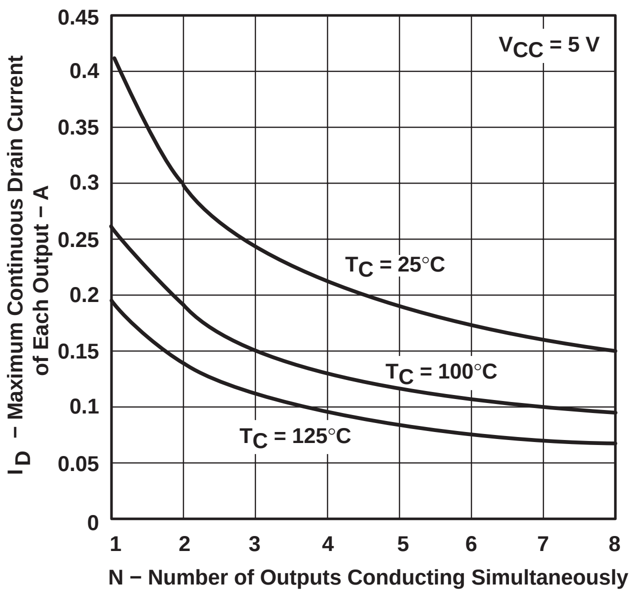



**Figure 10**

**MAXIMUM PEAK DRAIN CURRENT OF EACH OUTPUT vs NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY**

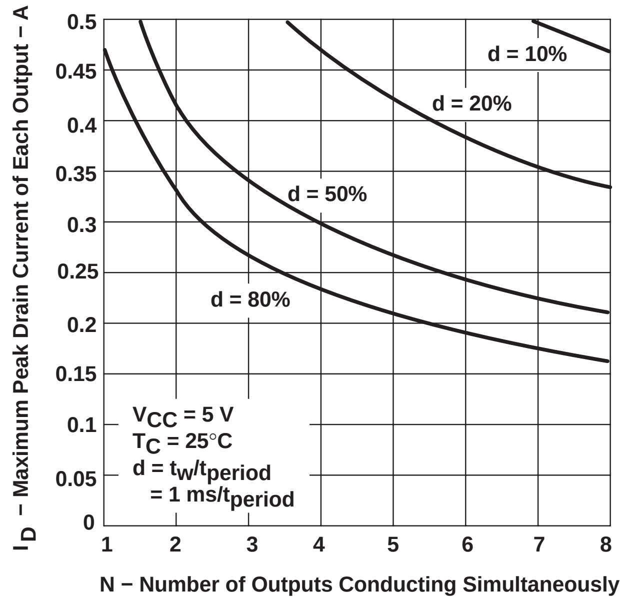



**Figure 11**

## Revision History

| DATE | REV | PAGE | SECTION | DESCRIPTION |
|---|---|---|---|---|
| 5/18/05 | A | 5 | Figure 1 | Changed $\overline{\text{SRCLR}}$ timing diagram |
| 3/2000 | * | | | Original reversion |

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPIC6B596DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TPIC6B596 | Samples |
| TPIC6B596DWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | TPIC6B596 | Samples |
| TPIC6B596DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TPIC6B596 | Samples |
| TPIC6B596DWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | TPIC6B596 | Samples |
| TPIC6B596N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TPIC6B596N | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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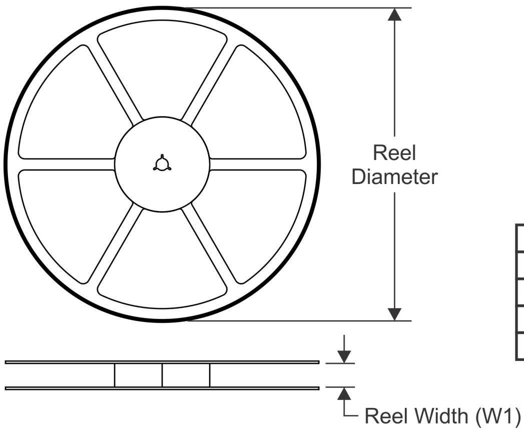
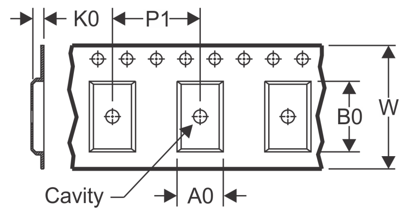
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

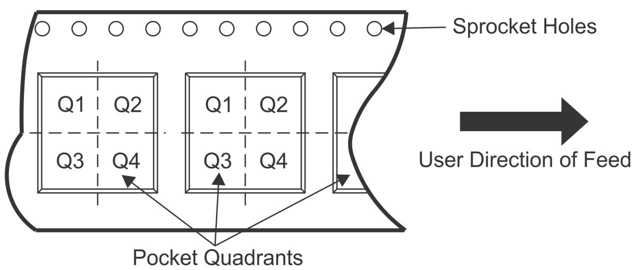



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

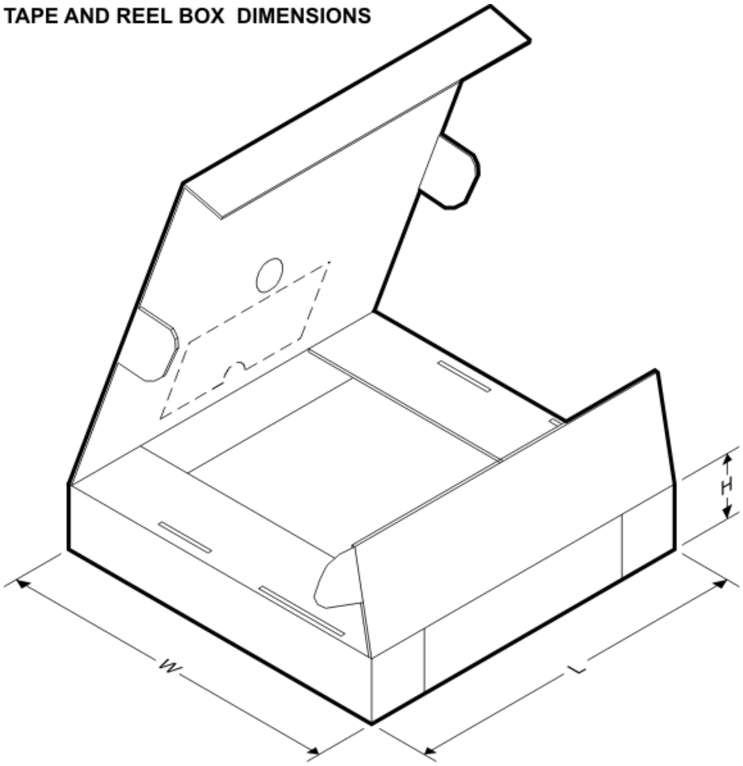
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPIC6B596DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |

## TAPE AND REEL BOX DIMENSIONS

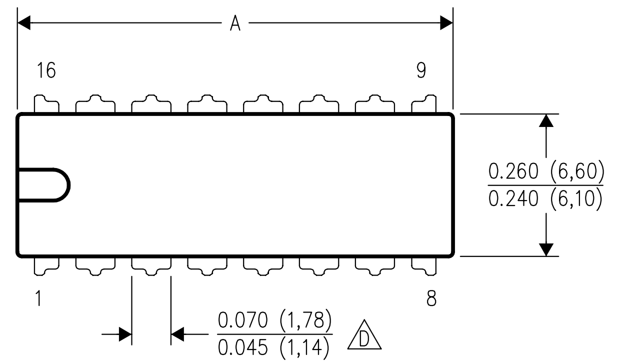



*All dimensions are nominal

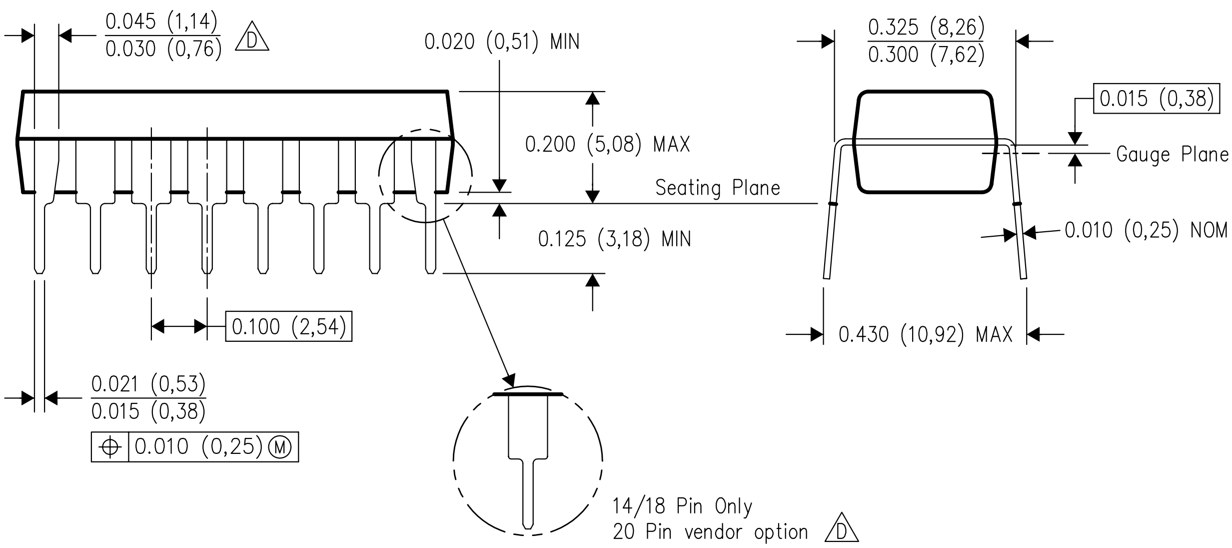
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPIC6B596DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |

## N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

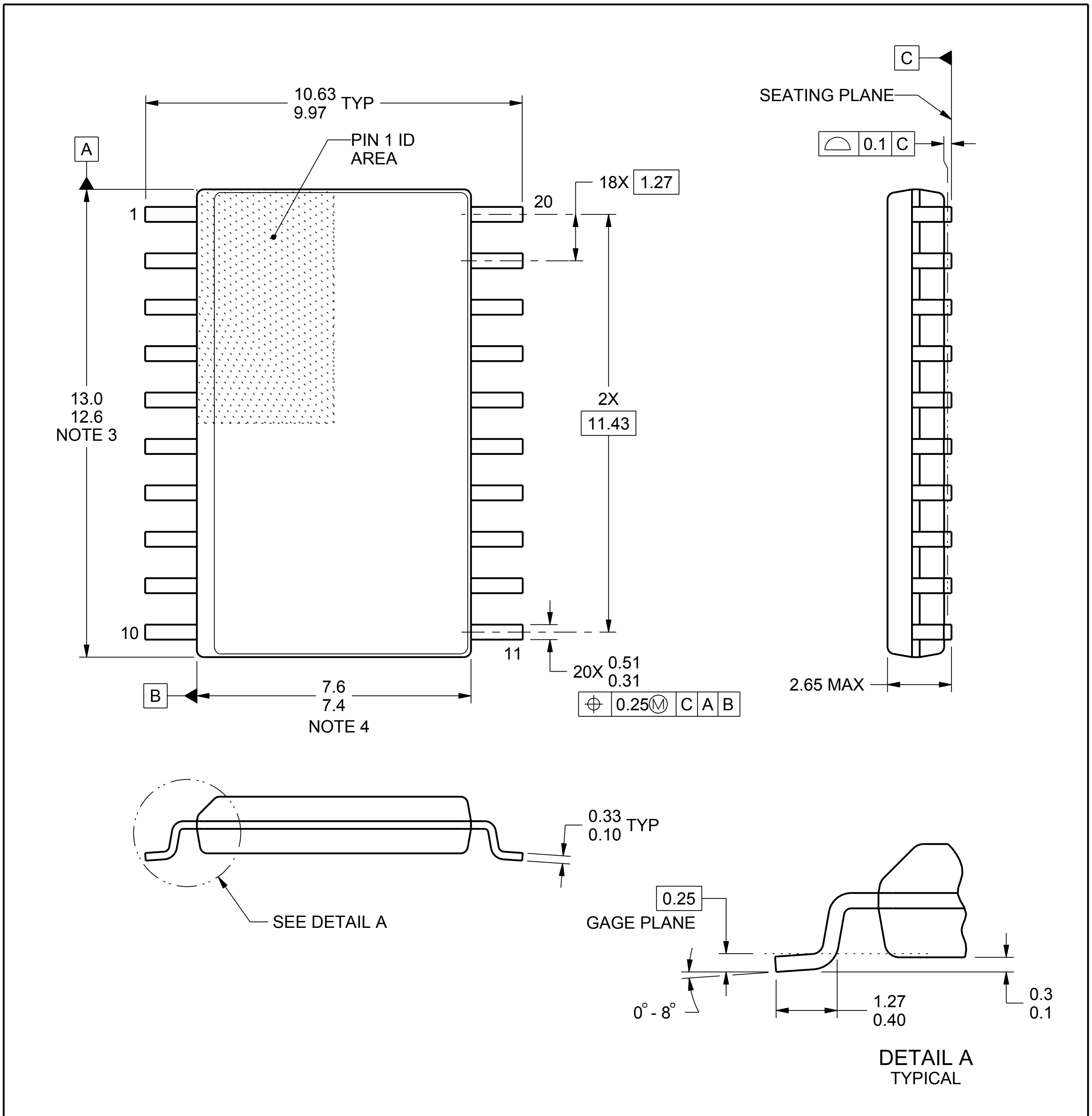



| PINS ** / DIM | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| (C) MS–001 VARIATION | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- (C) Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

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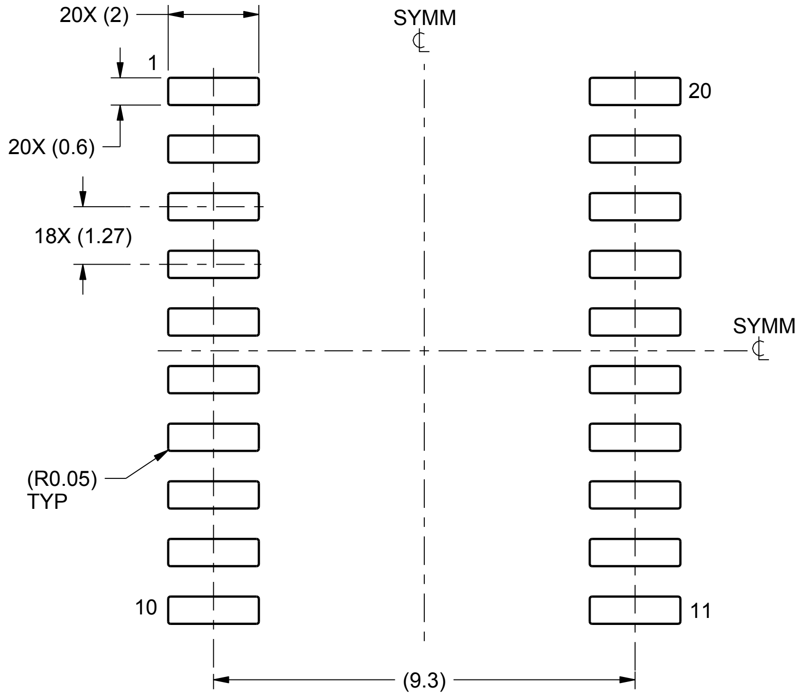
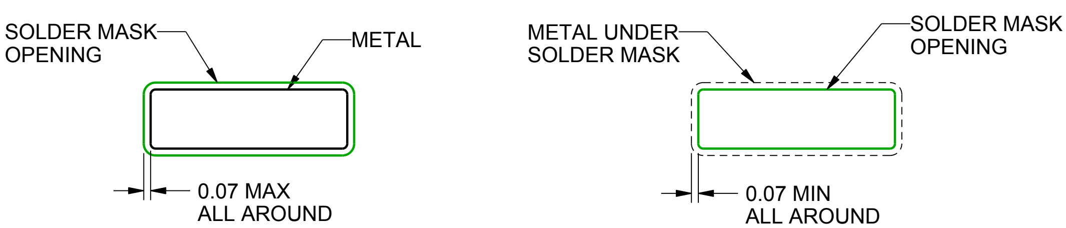
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.




LAND PATTERN EXAMPLE
SCALE:6X




NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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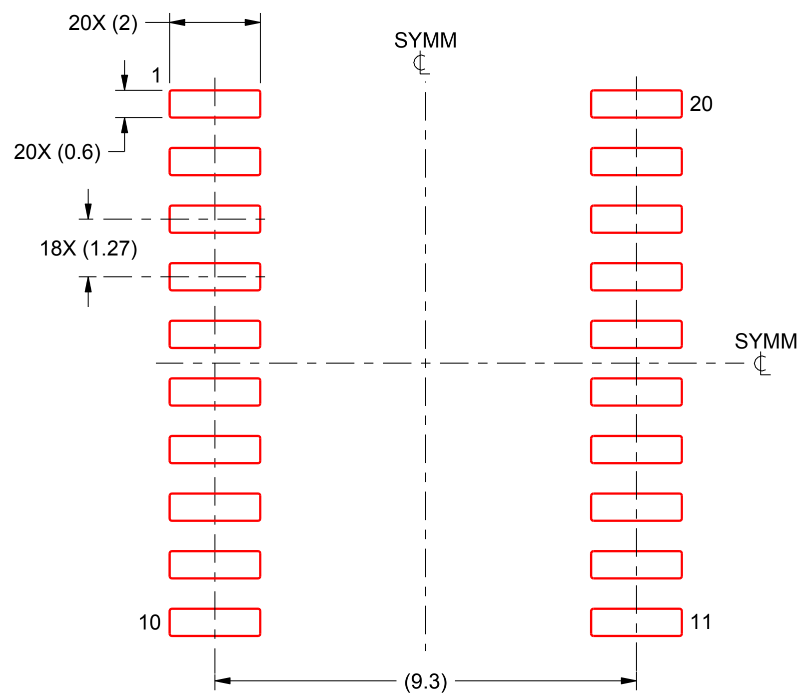
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.