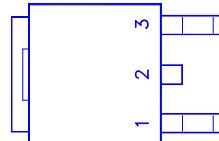
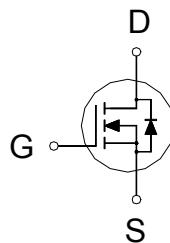


NIKO-SEM

**N-Channel Logic Level Enhancement
Mode Field Effect Transistor** **P1504BDG**
TO-252 (DPAK)
Halogen-Free & Lead-Free

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
40V	15mΩ	40A



1. GATE
2. DRAIN
3. SOURCE

ABSOLUTE MAXIMUM RATINGS ($T_c = 25^\circ C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_c = 25^\circ C$	I_D	40	A
	$T_c = 100^\circ C$		25	
Pulsed Drain Current ¹		I_{DM}	85	
Avalanche Current		I_{AS}	22	A
Avalanche Energy	$L = 0.3\text{mH}$	E_{AS}	72	mJ
Power Dissipation	$T_c = 25^\circ C$	P_D	42	W
	$T_c = 100^\circ C$		17	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	
Lead Temperature ($1/16$ " from case for 10 sec.)		T_L	275	$^\circ C$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$		3	$^\circ C / W$
Junction-to-Ambient	$R_{\theta JA}$		75	$^\circ C / W$

¹Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS ($T_c = 25^\circ C$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	Typ	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	40			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.7	2.0	3.0	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 250	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 32V, V_{GS} = 0V$			1	μA
		$V_{DS} = 30V, V_{GS} = 0V, T_c = 125^\circ C$			10	
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = 10V, V_{GS} = 10V$	85			A

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Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 7V, I_D = 10A$		18	27	$m\Omega$
		$V_{GS} = 10V, I_D = 20A$		12.5	15	
Forward Transconductance ¹	g_{fs}	$V_{DS} = 10V, I_D = 20A$		25		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 10V, f = 1MHz$		1145		pF
Output Capacitance	C_{oss}			255		
Reverse Transfer Capacitance	C_{rss}			95		
Total Gate Charge ²	Q_g	$V_{DS} = 0.5V_{(BR)DSS}, V_{GS} = 10V,$ $I_D = 10A$		23		nC
Gate-Source Charge ²	Q_{gs}			3.6		
Gate-Drain Charge ²	Q_{gd}			3.0		
Turn-On Delay Time ²	$t_{d(on)}$	$V_{DS} = 20V, R_L = 1\Omega$ $I_D \approx 1A, V_{GS} = 10V, R_{GEN} = 6\Omega$		3.2		nS
Rise Time ²	t_r			10.8		
Turn-Off Delay Time ²	$t_{d(off)}$			17.1		
Fall Time ²	t_f			5.3		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_C = 25^\circ C$)						
Continuous Current	I_S				32	A
Forward Voltage ¹	V_{SD}	$I_F = I_S, V_{GS} = 0V$			1.3	V
Reverse Recovery Time	t_{rr}	$I_F = I_S, dI_F/dt = 100A / \mu S$		60		nS
Reverse Recovery Charge	Q_{rr}			43		nC

¹Pulse test : Pulse Width $\leq 300 \mu sec$, Duty Cycle $\leq 2\%$.²Independent of operating temperature.**REMARK: THE PRODUCT MARKED WITH "P1504BDG", DATE CODE or LOT #**

NIKO-SEM

**N-Channel Logic Level Enhancement
Mode Field Effect Transistor**

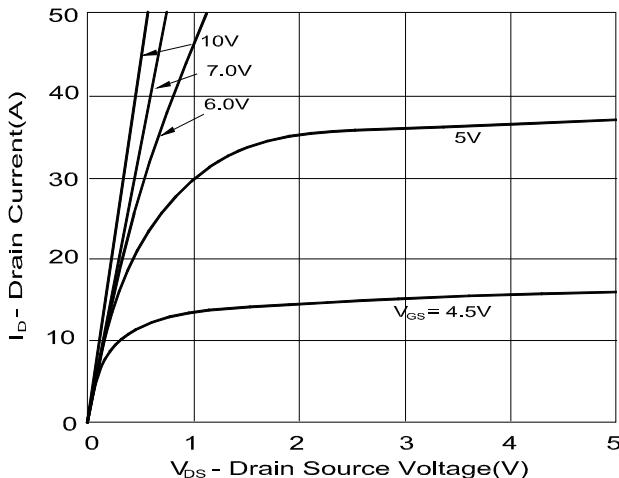
P1504BDG

TO-252 (DPAK)

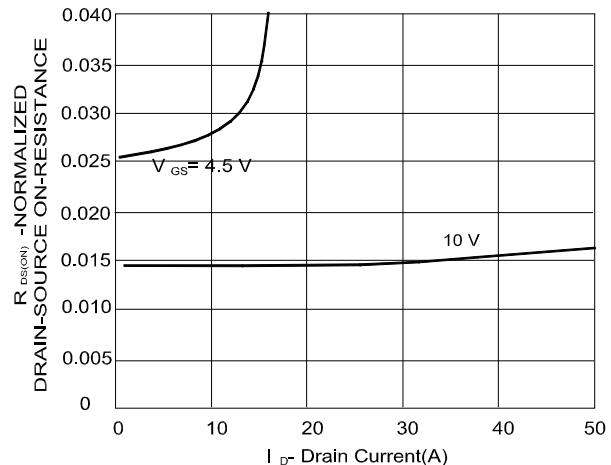
Halogen-Free & Lead-Free

TYPICAL PERFORMANCE CHARACTERISTICS

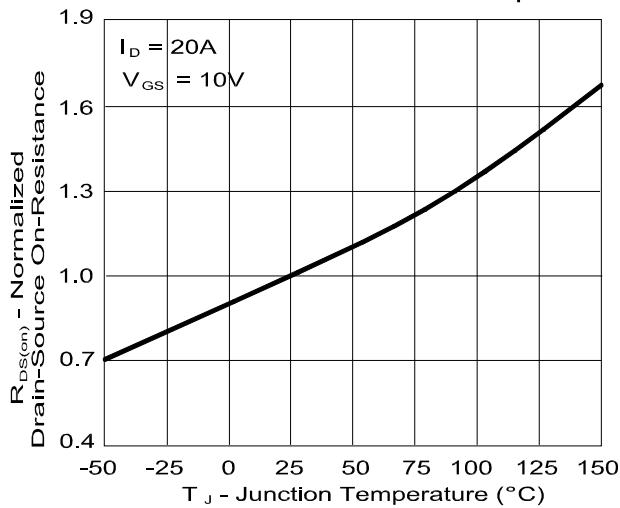
On-Region Characteristics



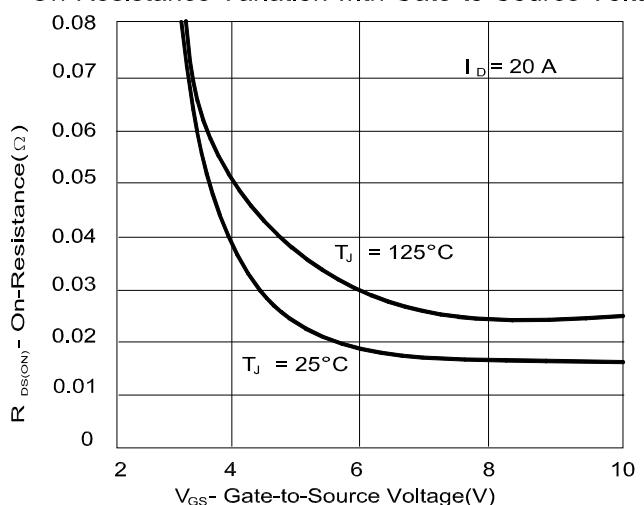
On-Resistance Variation with Drain Current and Gate Voltage



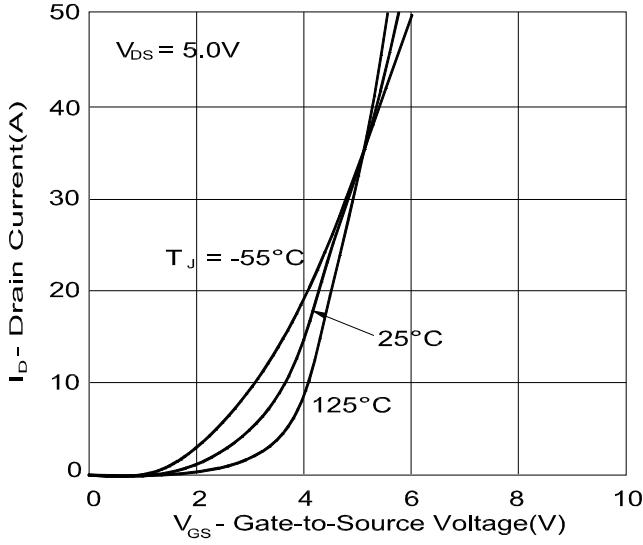
On-Resistance Variation with Temperature



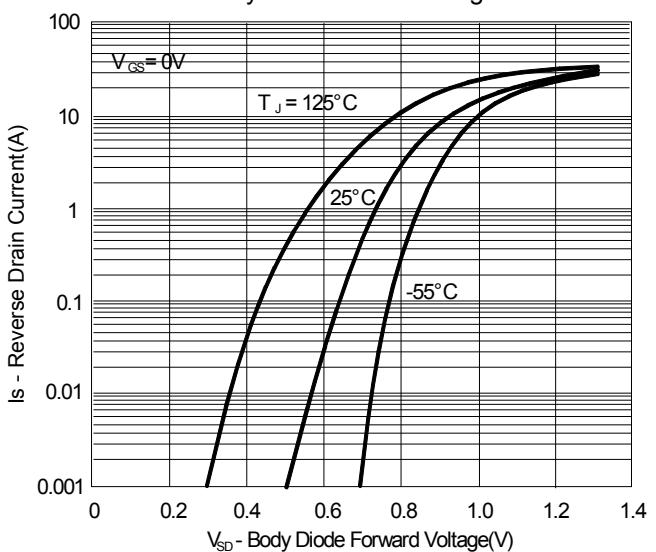
On-Resistance Variation with Gate-to-Source Voltage



Transfer Characteristics

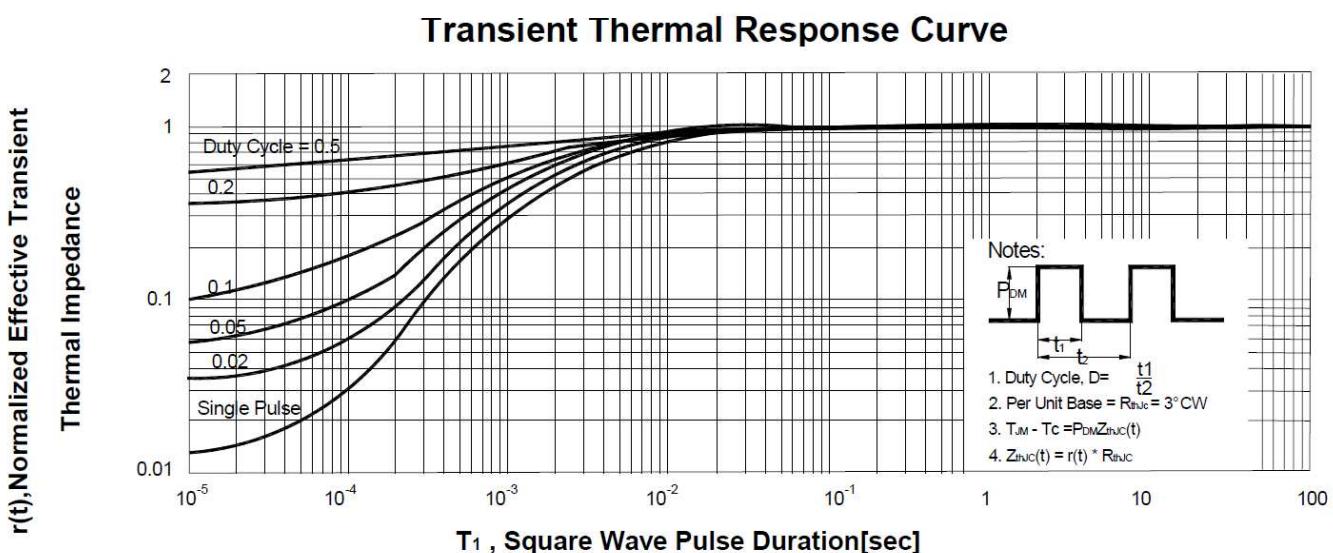
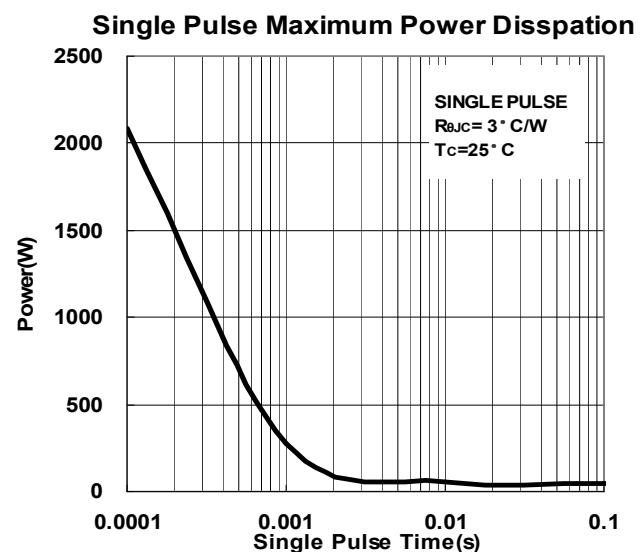
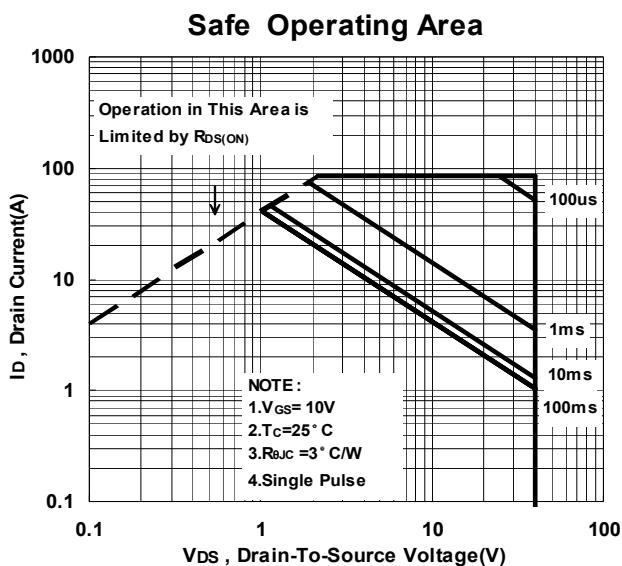
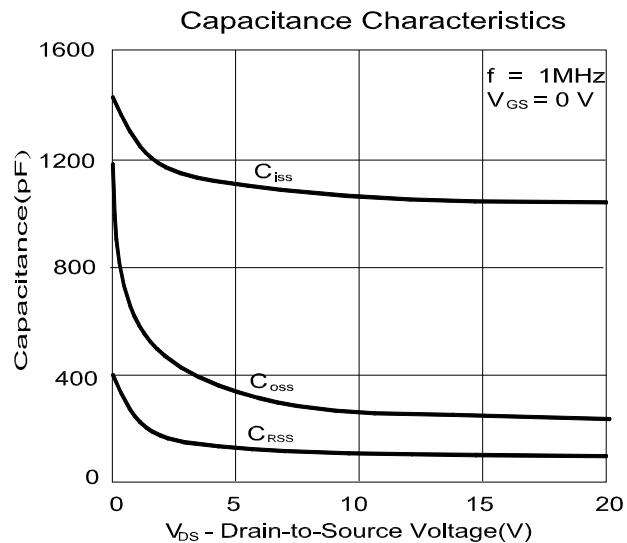
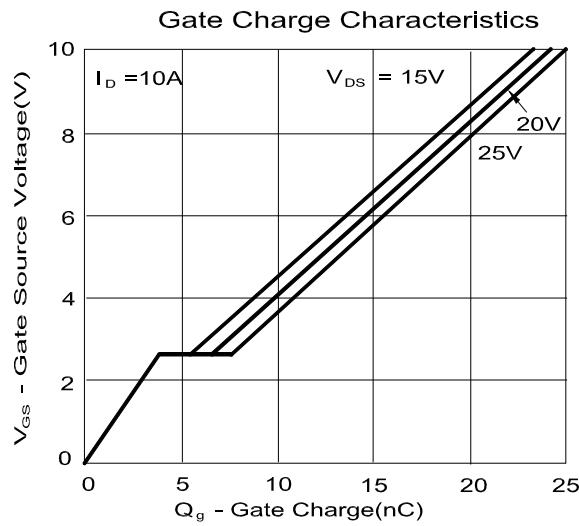


Body Diode Forward Voltage



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NIKO-SEM**N-Channel Logic Level Enhancement P1504BDG**
Mode Field Effect Transistor TO-252 (DPAK)
Halogen-Free & Lead-Free**TO-252 (DPAK) MECHANICAL DATA**

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	8.9	9.5	10.4	H	0.8	1.27	2.03
B	2.19	2.3	2.435	I	6.35	6.6	6.8
C	0.35	0.5	0.65	J	4.8	5.34	5.5
D	0.89		1.5	K	0.5		1.5
E	0.35		0.65	L	0.4	0.76	0.89
F	0.0		0.23	M	3.96		5.18
G	5.4		6.2	N			

