ALPHA & OMEGA SEMICONDUCTOR, INC.

July 2003

AOD412
N-Channel Enhancement Mode Field Effect Transistor

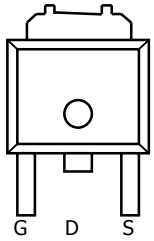
General Description

The AOD412 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate chargeand low gate resistance. This device is ideally suited for use as a high side switch in CPU core power conversion.

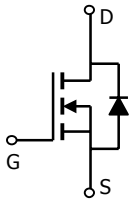
Features

V_{DS} (V) = 30V
I_D = 85A
$R_{DS(ON)}$ < 7.0mΩ (V_{GS} = 10V)
$R_{DS(ON)}$ < 10.5mΩ (V_{GS} = 4.5V)

TO-252
D-PAK



Top View
Drain Connected
to Tab



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [B,G]	T_C=25°C [G]	I_D	85	A
	T_C=100°C [B]		65	
Pulsed Drain Current		I_{DM}	200	
Avalanche Current [C]		I_{AR}	30	A
Repetitive avalanche energy L=0.1mH [C]		E_{AR}	120	mJ
Power Dissipation [B]	T_C=25°C	P_D	100	W
	T_C=100°C		50	
Power Dissipation [A]	T_A=25°C	P_{DSM}	2.5	W
	T_A=70°C		1.6	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	14.2	20	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		39	50	°C/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	0.8	1.5	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=24V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	1.5	2.15	2.5	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	85			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A		5.5	7	mΩ
		T_J=125°C		8.8	11	
		V_{GS}=4.5V, I_D=20A		8.25	10.5	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A		60		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.72	1	V
I_S	Maximum Body-Diode Continuous Current				85	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		1320		pF
C_{oss}	Output Capacitance			533		pF
C_{rss}	Reverse Transfer Capacitance			154		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		0.95		Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=4.5V, V_{DS}=15V, I_D=20A		26		nC
Q_g(4.5V)	Total Gate Charge			13.3		nC
Q_{gs}	Gate Source Charge			3.2		nC
Q_{gd}	Gate Drain Charge			6.6		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=0.75Ω, R_{GEN}=3Ω		7.2		ns
t_r	Turn-On Rise Time			12.5		ns
$t_{D(off)}$	Turn-Off DelayTime			22		ns
t_f	Turn-Off Fall Time			6		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, dI/dt=100A/µs		29.7		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, dI/dt=100A/µs		22.3		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The Power dissipation P_{DSM} is based on steady-state $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C. The value in any a given application depends on the user's specific board design, and the maximum temperature fo 175°C may be used if the PCB or heatsink allows it.
B. The power dissipation P_D is based on $T_{J(MAX)}$=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.
C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175°C.
D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.
G. The maximum current rating is limited by the package current capability.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

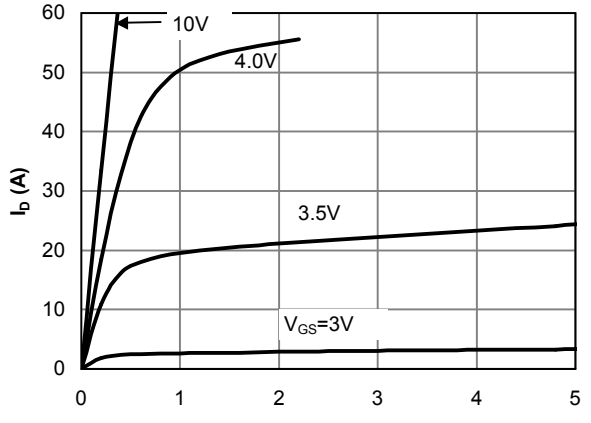


Fig 1: On-Region Characteristics

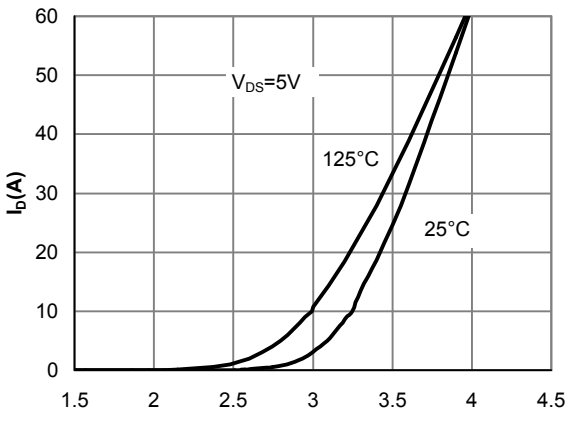


Figure 2: Transfer Characteristics

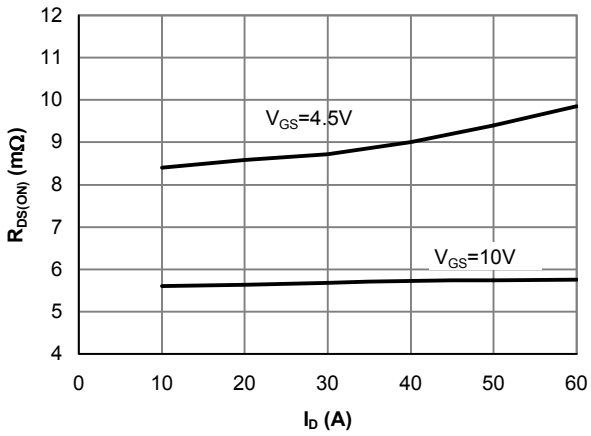


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

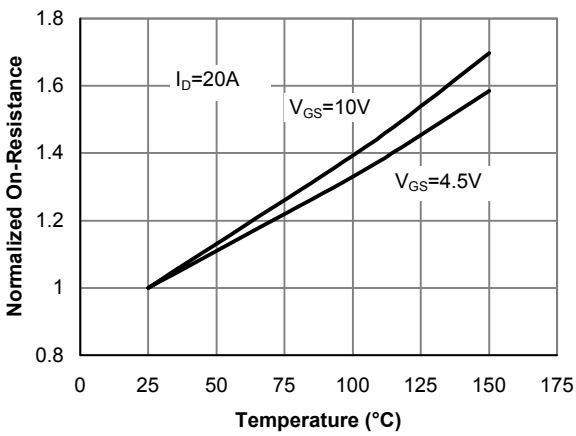


Figure 4: On-Resistance vs. Junction Temperature

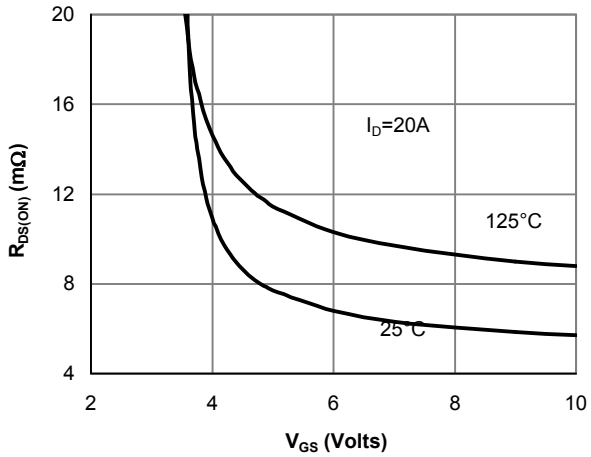


Figure 5: On-Resistance vs. Gate-Source Voltage

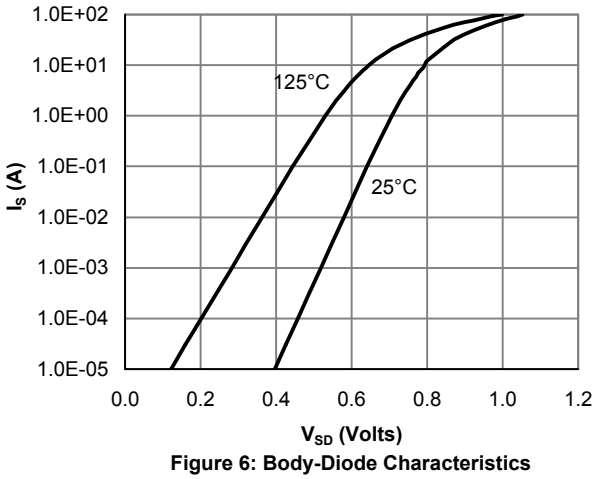


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

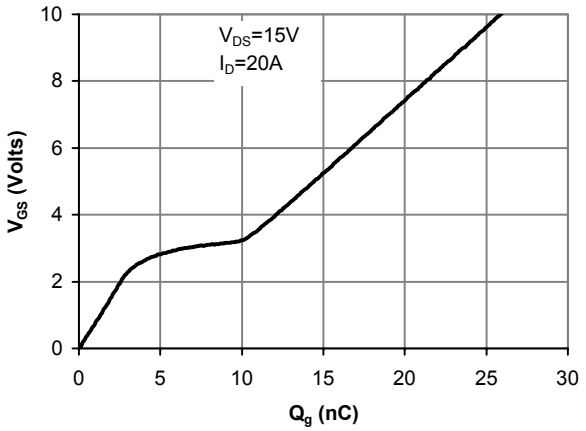


Figure 7: Gate-Charge Characteristics

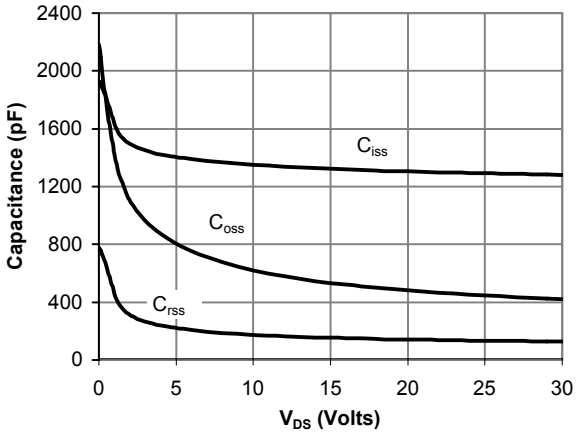


Figure 8: Capacitance Characteristics

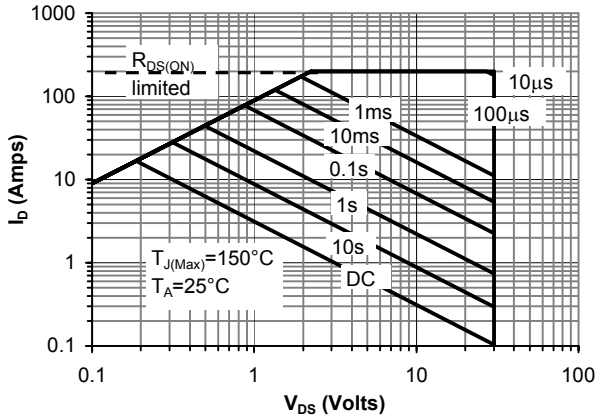


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

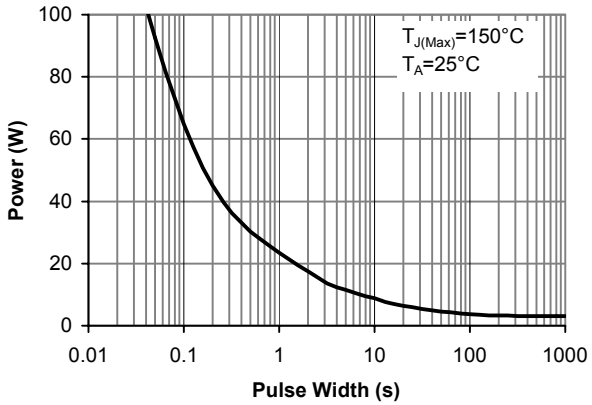


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

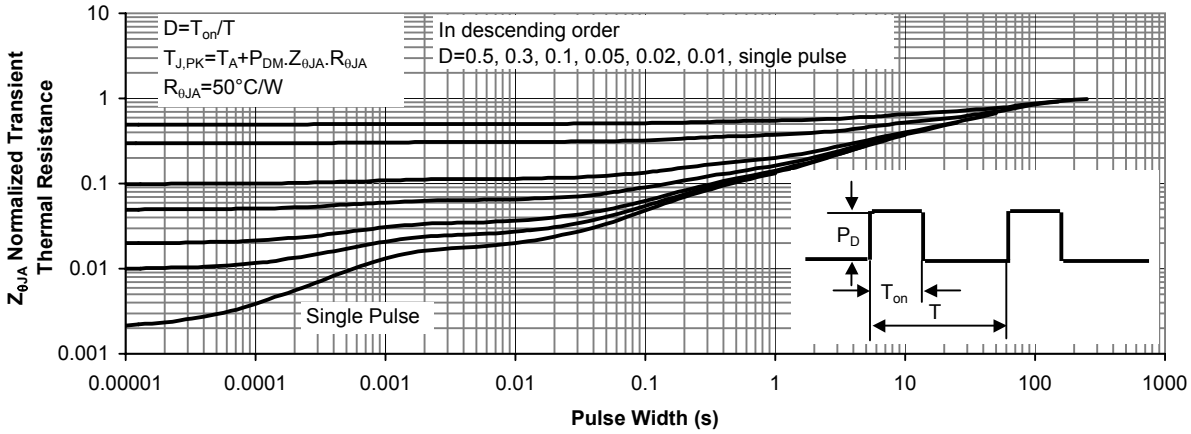


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

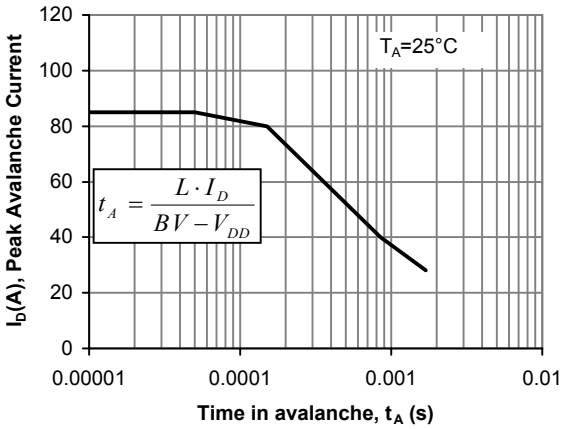


Figure 12: Single Pulse Avalanche capability

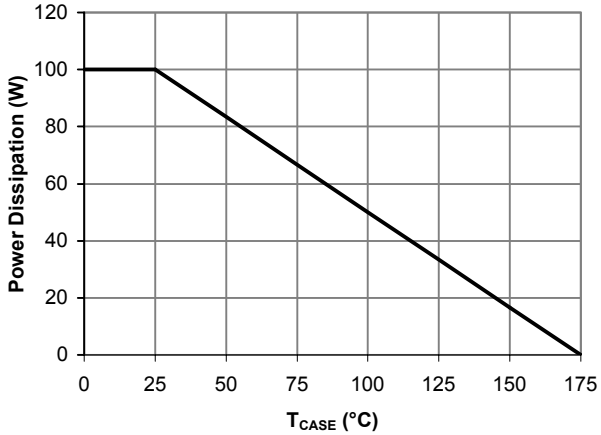


Figure 13: Power De-rating (Note B)

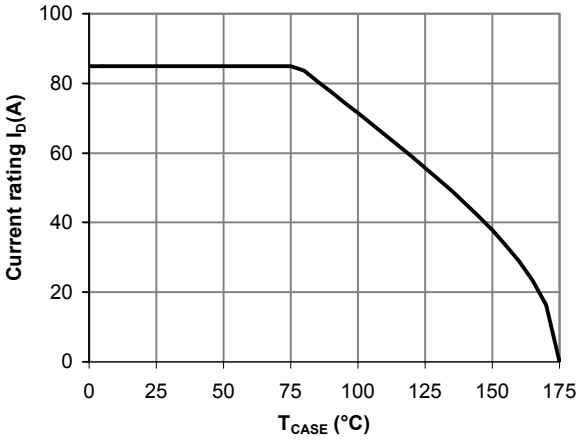
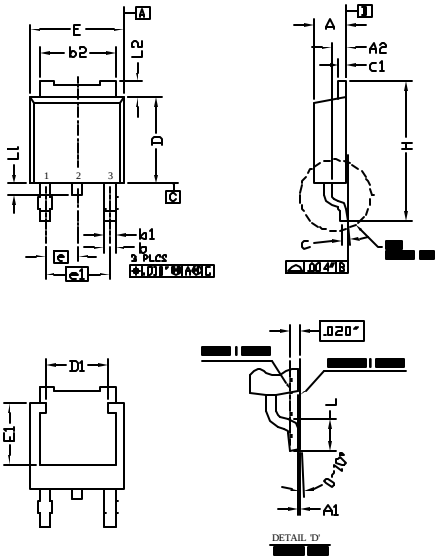


Figure 14: Current De-rating (Note B)

ALPHA & OMEGA
SEMICONDUCTOR, INC.

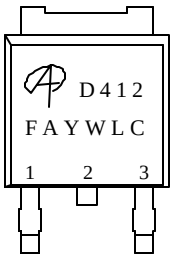
DPAK Package Data
(JEDEC TO-252)



	DIMENSION IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.235	2.286	2.388	0.088	0.090	0.094
A1	0.000	-----	0.102	0.000	-----	0.004
A2	0.889	-----	1.143	0.035	-----	0.045
b	0.686	0.762	0.889	0.027	0.030	0.035
b1	0.889	-----	1.143	0.035	-----	0.045
b2	5.207	4.45	5.461	0.205	-----	0.215
c	0.457	0.508	0.559	0.018	0.020	0.022
c1	0.483	-----	0.584	0.019	-----	0.023
D	5.969	6.096	6.223	0.235	0.240	0.245
D1	4.318	-----	5.334	0.170	-----	0.210
E	6.477	6.604	6.731	0.255	0.260	0.265
E1	4.318	-----	-----	0.170	-----	-----
e	2.286 BSC.			0.090 BSC.		
e1	4.572 BSC.			0.180 BSC.		
H	9.779	-----	10.414	0.385	-----	0.410
L	1.270	-----	2.032	0.050	-----	0.080
L1	0.635	-----	1.016	0.025	-----	0.040
L2	0.889	-----	1.270	0.035	-----	0.050

NOTE
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS
2. DIMENSION L IS MEASURED IN GAGE PLANE
3. TOLERANCE 0.10 mm UNLESS OTHERWISE SPECIFIED
4. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
5. FOLLOWED FROM JEDEC TO-252 (AA)

PACKAGE MARKING DESCRIPTION



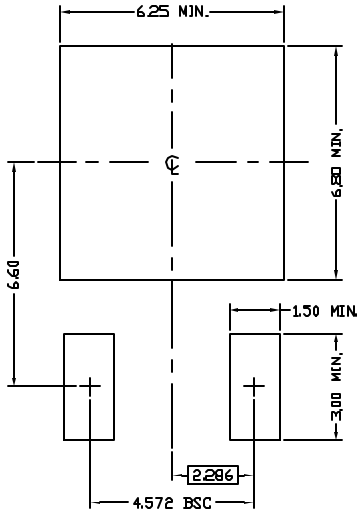
NOTE:

- AOS LOGO
D412 - PART NUMBER CODE.
F - FAB LOCATION
A - ASSEMBLY LOCATION
Y - YEAR CODE
W - WEEK CODE.
L C - ASSEMBLY LOT CODE

DPAK PART NO. CODE

PART NO.	CODE
AOD412	D412

RECOMMENDED LAND PATTERN



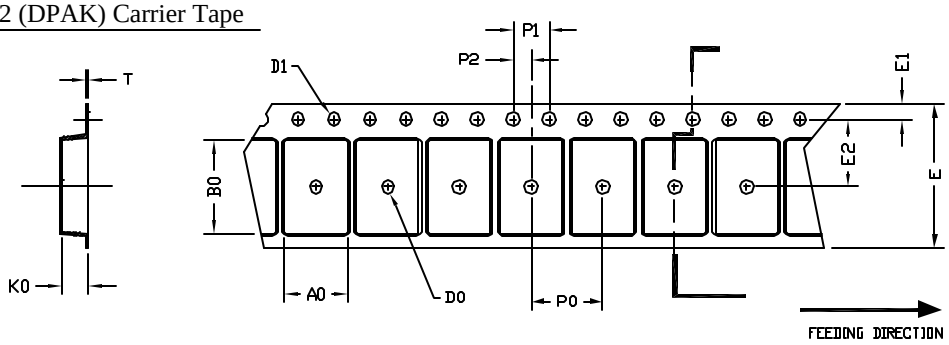
UNIT: mm

Rev. A

ALPHA & OMEGA
SEMICONDUCTOR, INC.

TO-252 (DPAK)
Tape and Reel Data

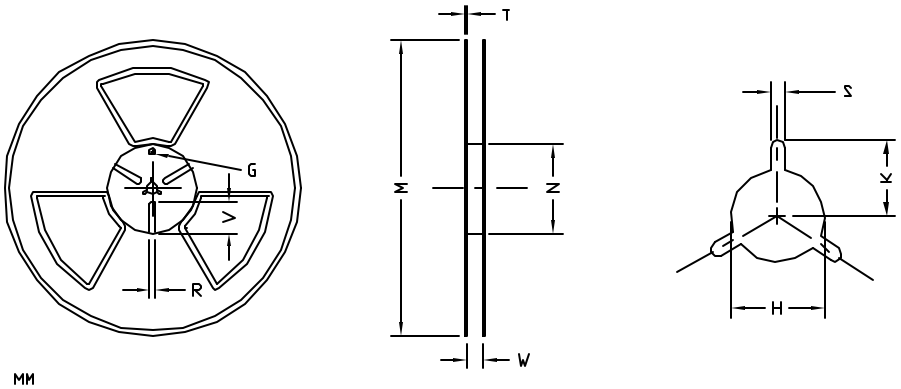
TO-252 (DPAK) Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
TO-252(DPAK) (16 mm)	6.90 ±0.10	10.50 ±0.10	2.70 ±0.10	1.50 ±0.10	1.50 MIN.	16.00 ±0.10	1.75 ±0.10	7.50 ±0.10	8.00 ±0.10	4.00 ±0.10	2.00 ±0.10	0.30 ±0.05

TO-252 (DPAK) Reel



UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	T	H	K	S	G	R	V
16 mm	ø330	ø330.00 ±0.10	ø99.50 ±0.10	17.50 ±0.50	2.30	ø13.50 ±0.10	10.60	2.50 ±0.10	---	---	---

TO-252 (DPAK)

Leader / Trailer & Orientation