

# SN5445, SN7445 BCD-TO-DECIMAL DECODERS/DRIVERS

SDLS110

DECEMBER 1972 - REVISED MARCH 1988

FOR USE AS LAMP, RELAY, OR MOS DRIVERS

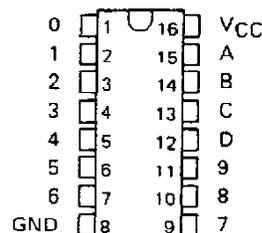
featuring

- Full Decoding of Input Logic
- 80-mA Sink-Current Capability
- All Outputs Are Off for Invalid BCD Input Conditions

SN5445 . . . J OR W PACKAGE

SN7445 . . . N PACKAGE

(TOP VIEW)



FUNCTION TABLE

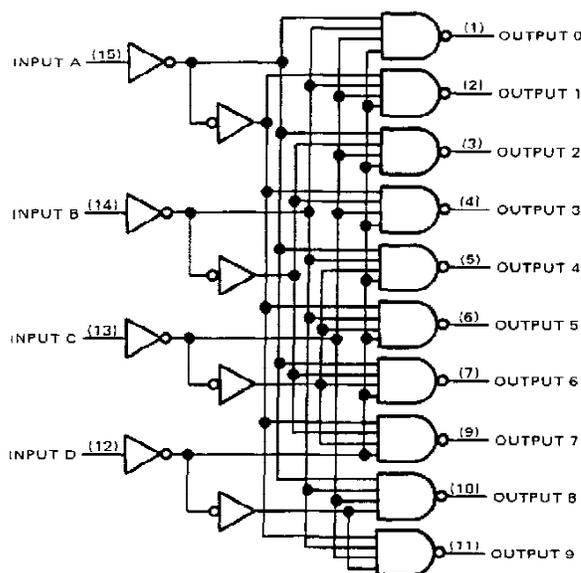
NO.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H

H = high level (off), L = low level (on)

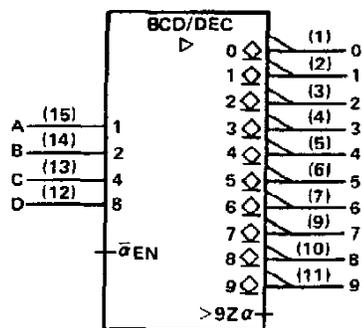
## description

These monolithic BCD-to-decimal decoders/drivers consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remain off for all invalid binary input conditions. These decoders feature TTL inputs and high-performance, n-p-n output transistors designed for use as indicator/relay drivers or as open-collector logic-circuit drivers. Each of the high-breakdown output transistors (30 volts) will sink up to 80 milliamperes of current. Each input is one normalized Series 54/74 load. Inputs and outputs are entirely compatible for use with TTL logic circuits, and the outputs are compatible for interfacing with most MOS integrated circuits. Power dissipation is typically 215 milliwatts.

## logic diagram (positive logic)



## logic symbol



Pin numbers shown are for J, N, and W packages.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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# SN5445, SN7445 BCD-TO-DECIMAL DECODERS/DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	5.5 V
Maximum current into any output (off-state)	1 mA
Operating free-air temperature range: SN5445 Circuits	-55°C to 125°C
SN7445 Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

	SN5445			SN7445			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage			30			30	V
Operating free-air temperature, $T_A$	-55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{IH}$ High-level input voltage		2			V
$V_{IL}$ Low-level input voltage				0.8	V
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}$ , $I_I = -12 \text{ mA}$			-1.5	V
$V_{O(\text{on})}$ On-state output voltage	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = 0.8 \text{ V}$		0.5	0.9	V
				0.4	
$I_{O(\text{off})}$ Off-state output current	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = 0.8 \text{ V}$ , $V_{O(\text{off})} = 30 \text{ V}$			250	$\mu\text{A}$
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}$ , $V_I \approx 5.5 \text{ V}$			1	mA
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}$ , $V_I = 2.4 \text{ V}$			40	$\mu\text{A}$
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}$ , $V_I = 0.4 \text{ V}$			-1.6	mA
$I_{CC}$ Supply current	$V_{CC} = \text{MAX}$ , See Note 2			43	62
		SN5445		43	70
		SN7445			

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡ All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

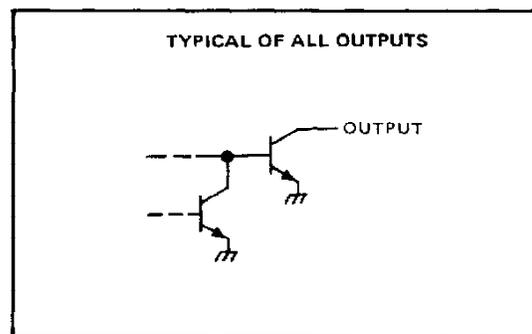
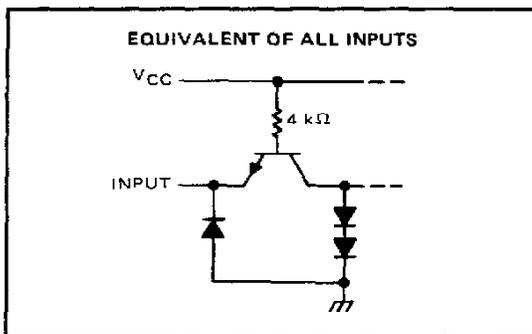
NOTE 2:  $I_{CC}$  is measured with all inputs grounded and outputs open.

## switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ Propagation delay time, low-to-high-level output	$C_L = 15 \text{ pF}$ , $R_L = 100 \Omega$ , See Note 3			50	ns
$t_{PHL}$ Propagation delay time, high-to-low-level output				50	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

## schematics of inputs and outputs



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## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN5445J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN5445J	<a href="#">Samples</a>
SN7445N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN7445N	<a href="#">Samples</a>
SN7445N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN7445N	<a href="#">Samples</a>
SN7445NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN7445N	<a href="#">Samples</a>
SN7445NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN7445N	<a href="#">Samples</a>
SNJ5445J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ5445J	<a href="#">Samples</a>
SNJ5445J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ5445J	<a href="#">Samples</a>
SNJ5445W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ5445W	<a href="#">Samples</a>
SNJ5445W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ5445W	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN5445, SN7445 :**

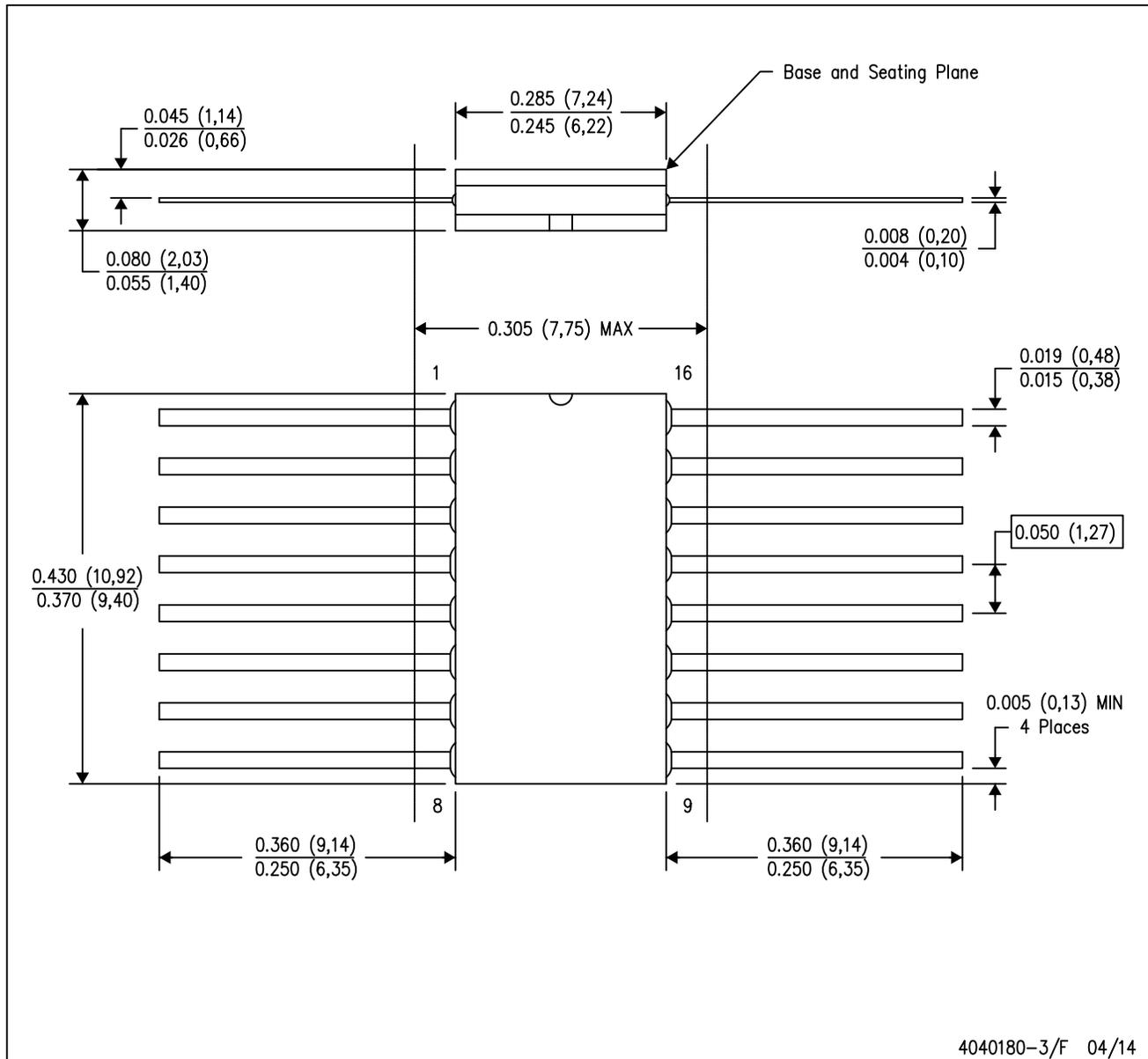
- Catalog: [SN7445](#)
- Military: [SN5445](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK

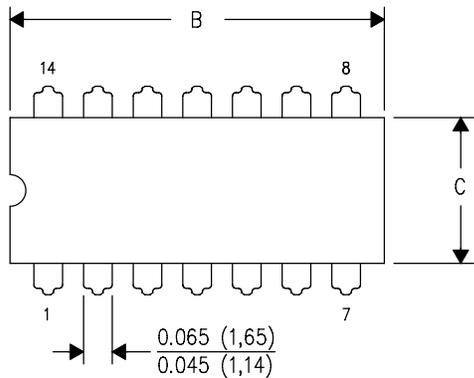


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP2-F16

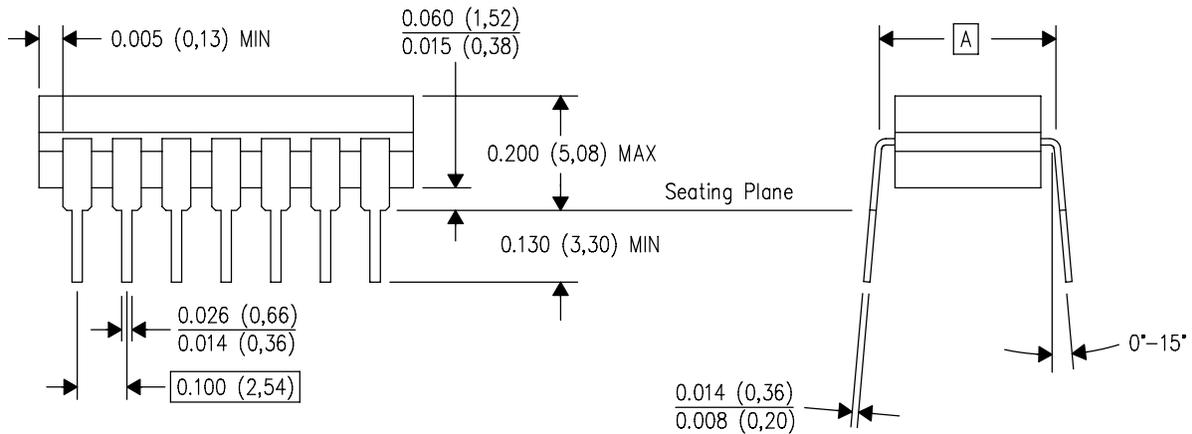
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



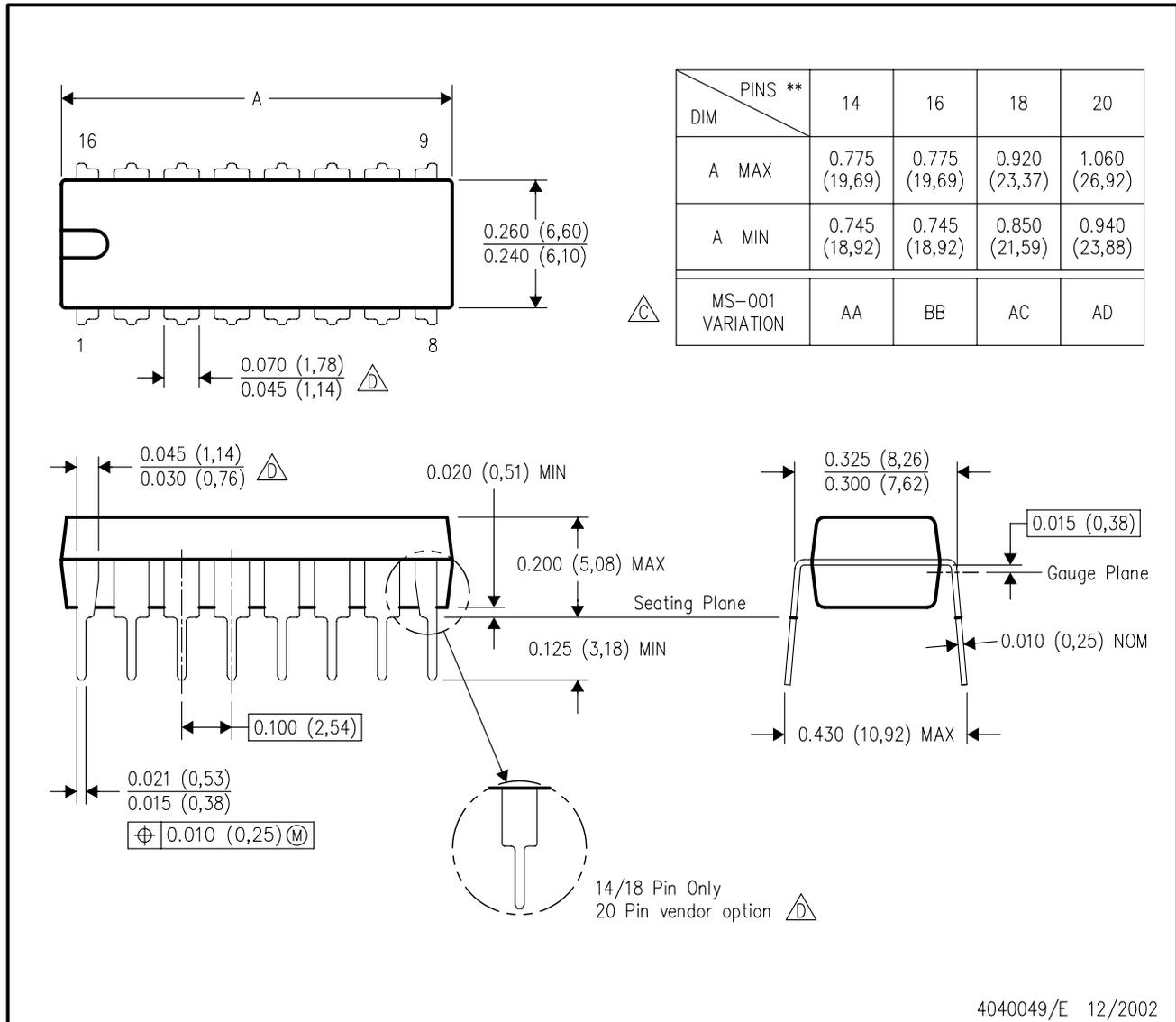
4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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