## 

## +3.3V Multiprotocol 3Tx/3Rx Software-Selectable Control Transceivers

### **General Description**

The MAX3171/MAX3173 are three-driver/three-receiver multiprotocol transceivers that operate from a single +3.3V supply. The MAX3171/MAX3173, along with the MAX3170 and MAX3172/MAX3174, form a complete software-selectable data terminal equipment (DTE) or data communications equipment (DCE) interface port that supports V.28 (RS-232) and V.10/V.11 (RS-449, V.36, EIA-530, EIA-530-A, X.21, RS-423) protocols. The MAX3171/MAX3173 transceivers carry the serial interface control signaling; the MAX3170 transceivers carry the clock and data signals. The MAX3172/MAX3174 have an extra transceiver for applications requiring four transceivers for control signaling.

An internal charge pump and proprietary low-dropout transmitter output stage allow V.28, V.11, and V.10 compliant operation from a single +3.3V supply. A nocable mode is entered when all mode pins (M0, M1, and M2) are pulled high or left unconnected. In nocable mode, supply current decreases to 2mA and all transmitter and receiver outputs are disabled (high impedance). Short-circuit limiting and thermal-shutdown circuits protect the drivers against excessive power dissipation.

The MAX3171 features 10µs deglitching on the V.10/V.11/V.28 receiver inputs. The MAX3173 is available for applications that do not require deglitching on the serial handshake signals.

These parts require only four surface-mount capacitors for charge-pump operation in addition to supply bypassing.

#### **Features**

- ♦ Industry's First +3.3V Multiprotocol Transceiver
- ♦ Certified TBR-1 and TBR-2 Compliant (NET1 and NET2)
- ♦ Supports V.28 (RS-232) and V.10/V.11 (RS-449, V.36, EIA-530, EIA-530-A, X.21, RS-423) Protocols
- ♦ 3V/5V Logic Compatibility
- ♦ Software-Selectable DCE/DTE
- ♦ True Fail-Safe Receiver Operation
- ♦ Available in Small 28-Pin SSOP Package
- ♦ 10µs Receiver Input Deglitching (MAX3171 only)
- ◆ All Transmitter Outputs Fault Protected to ±15V, Tolerate Cable Miswiring

### **Applications**

Data Networking PCI Cards

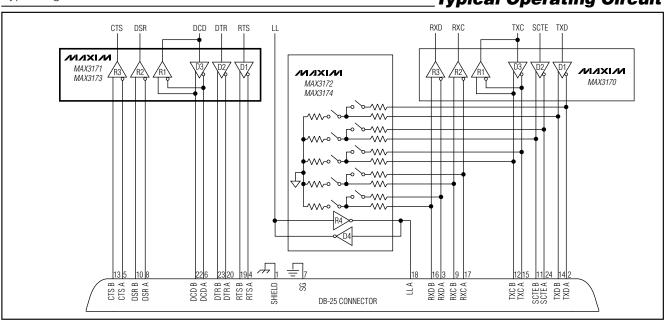
CSU and DSU Telecommunications

### **Ordering Information**

PART	TEMP. RANGE	PIN-PACKAGE		
MAX3171CAI	0°C to +70°C	28 SSOP		
MAX3173CAI	0°C to +70°C	28 SSOP		

Pin Configuration appears at end of data sheet

## Typical Operating Circuit



NIXIN

Maxim Integrated Products

#### **ABSOLUTE MAXIMUM RATINGS**

(All voltages referenced to GND unless Supply Voltages	otherwise noted.)
V <sub>C</sub> C	0.3V to +4V
V+ (Note 1)	0.3V to +7V
V- (Note 1)	+0.3V to -7V
V+ to V- (Note 1)	13V
Logic Input Voltages	
M0, M1, M2, DCE/DTE, T_IN	0.3V to +6V
Logic Output Voltages	
R_OUT	0.3V to (V <sub>CC</sub> + 0.3V)
Short-Circuit Duration	Continuous

Transmitter Outputs		
T_OUT	15V	to +15V
Short-Circuit Duration		60s
Receiver Inputs		
R_IN	15V	to +15V
Continuous Power Dissipation ( $T_A = +7$ )		
28-Pin SSOP (derate 11.1mW/°C abo	ve +70°C)	889mW
Operating Temperature Range		
MAX3171CAI/MAX3173CAI	0°C 1	to +70°C
Storage Temperature Range	65°C to	+150°C
Lead Temperature (soldering, 10s)		+300°C

Note 1: V+ and V- can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### **ELECTRICAL CHARACTERISTICS**

 $(V_{CC} = 3.3V \pm 5\%; C1 = C2 = 1\mu F, C3 = C4 = C5 = 3.3\mu F, and T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $V_{CC} = +3.3V$ ,  $T_A = +25$ °C.) (Note 2)

PARAMETER	SYMBOL	BOL CONDITIONS		TYP	MAX	UNITS		
DC CHARACTERISTICS			<u>.</u>					
		V.11/V.10 modes		220	300			
Supply Current		V.11/V.10 modes (no load)		6	23			
(DCE Mode, Digital Inputs = GND or V <sub>CC</sub> , Transmitter	Icc	V.28 mode		24	40	mA		
Outputs Static)		V.28 mode (no load)		6	23			
,		No-cable mode		2	8			
Internal Power Dissipation		V.11/V.10 modes (no load)		20				
		V.11/V.10 modes (full load)		450		mW		
Internal Power Dissipation	PD	V.28 mode (full load)		40				
		No-cable mode		6.6				
		V.11/V.10 modes (no load)	4.4					
	.,	V.11/V.10 modes (full load)	4.2			.,		
V+ Output Voltage	V+	V.28 mode	5.55			V		
		No-cable mode		4.6				
		V.11/V.10 modes (no load)			-4.0			
V. Outrout Valtage	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	V.11/V.10 modes (full load)			-3.8	.,		
V- Output Voltage	V-	V.28 mode			-5.45	V		
		No-cable mode		-4.2		1		
Charge-Pump Enable Time		Delay until V+ and V- specifications met		1		ms		
LOGIC INPUTS (M0, M1, M2, D	CE/DTE, T_IN	))						
Input High Voltage	VIH		2.0			V		
Input Low Voltage	V <sub>IL</sub>				0.8	V		
		T_IN			±1			
Logic Input Current	I <sub>IH</sub> , I <sub>IL</sub>	M0, M1, M2, DCE/DTE = VCC			±1	μΑ		
		M0, M1, M2, DCE/DTE = GND	30	50	100			

**ELECTRICAL CHARACTERISTICS (continued)** ( $V_{CC} = 3.3V \pm 5\%$ ;  $C1 = C2 = 1\mu F$ ,  $C3 = C4 = C5 = 3.3\mu F$ , and  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $V_{CC}$ 

Duty   Digit   Dig	PARAMETER	SYMBOL		CONDITIONS	MIN	TYP	MAX	UNITS
Output Low Voltage         Vol.         ISINK = 1.6mA   voltage         0.4         V           Rise or Fall Time         It, it         10% to 90%, Figure 4         15         ns           Output Leakage Current (Receiver Output Three-Stated)         R_OUT = GND   R_OUT = Voc   ±1         30 50 100   μA         μβ           TRANSMITTER OUTPUTS         IZ         -0.25V ≤ Vout ≤ +0.25V, power off or no-cable mode   115   voltage	LOGIC OUTPUTS (R_OUT)							
Output Low Voltage         Vol.         Islank = 1.6mA         0.4         V           Rise or Fall Time         tr. tr         10% to 90%, Figure 4         15         ns           Output Leakage Current (Receiver Output Three-Stated)         R_OUT = GND_ROW_ROW_STEPP         30         50         100           TRANSMITTER OUTPUTS	Output High Voltage	VoH	ISOURCE = 1.0	DmA	V <sub>CC</sub> - 1.0	)		V
R_OUT = GND   30   50   100   μA	Output Low Voltage						0.4	V
R_OUT = VCC	Rise or Fall Time	t <sub>r</sub> , t <sub>f</sub>	10% to 90%,	igure 4		15		ns
R_OUT = V <sub>CC</sub>	Output Leakage Current		R_OUT = GN	D	30	50	100	^
Dutput Leakage Current   IZ			R_OUT = Vcc	<u> </u>			±1	μΑ
Data Rate   1/2   No-cable mode	TRANSMITTER OUTPUTS				•			
Data Rate         V.10         115         kbps           Receiver Glitch Rejection (MAX3171 only)         Minimum pulse width passed         5         μβ           Receiver Input Resistance         RIN         10 ∨ VAB ≤ +10V, Va or VB grounded, V.11V/.35, no-cable mode         20         40         μβ           -16V ≤ VAB ≤ +15V, V.28 mode         3         5         7         γΩ         γΩ <t< td=""><td>Output Leakage Current</td><td>IZ</td><td></td><td>•</td><td>-100</td><td></td><td>100</td><td>μΑ</td></t<>	Output Leakage Current	IZ		•	-100		100	μΑ
Data Rate   V.10			V.28			240		
Minimum pulse width passed   5	Data Rate		V.10			115		кррѕ
Minimum pulse width rejected   15   15   15   15   15   15   15   1			V.11			10		Mbps
(MAX3171 only)         Minimum pulse width rejected         15         μs           Receiver Input Resistance         RIN         -10V ≤ VAB ≤ +10V, VA or VB grounded, V.11V.35, no-cable mode         20         40         KΩ           Data Rate         MAX3171         V.10V.28 mode         3         5         7           WAX3173         V.10V.28         64         W.11         64         W.11         MBps           V.11 TRANSMITTER         Unloaded Differential Output Voltage         VODO         R = 1.95kΩ, Figure 1         4.0         6.0         V           Loaded Differential Output Voltage         VODL         R = 50Ω, Figure 1         0.5 × VODO         V           Change in Magnitude of Output Differential Voltage         AVOD         R = 50Ω, Figure 1         0.5 × VODO         V           Common-Mode Output Voltage         VOC         R = 50Ω, Figure 1         3.0         V           Change in Magnitude of Output Common-Mode Voltage         AVOC         R = 50Ω, Figure 1         3.0         V           Short-Circuit Current         Isc         T_OUTA/B = GND         60         150         mA           Rise or Fall Time         t <sub>1</sub> , t <sub>1</sub> 10% to 90%, Figure 2         10         25         ns	Receiver Glitch Rejection		Minimum puls	e width passed	5			
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	•		Minimum puls	e width rejected			15	μs
	Receiver Input Resistance	R <sub>IN</sub>				40		ΚΩ
			-15V ≤ V <sub>A</sub> ≤ +	15V, V.28 mode	3	5	7	
			MAVO171	V.10/V.28		64		
$ \begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	Data Data		IVIAA3171	V.11		64		kbps
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Data нате		MAVO170	V.10/V.28				
Unloaded Differential Output Voltage $V_{ODO}$ $R = 1.95k\Omega$ , Figure 1 $4.0$ $6.0$ $V$ Loaded Differential Output Voltage $V_{ODL}$ $R = 50\Omega$ , Figure 1 $0.5 \times V_{ODO}$ $V$ Change in Magnitude of Output Differential Voltage $\Delta V_{OD}$ $R = 50\Omega$ , Figure 1 $0.2$ $V$ Common-Mode Output Voltage $V_{OC}$ $R = 50\Omega$ , Figure 1 $0.2$ $V$ Change in Magnitude of Output Common-Mode Voltage $\Delta V_{OC}$ $R = 50\Omega$ , Figure 1 $0.2$ $V$ Short-Circuit Current $I_{SC}$ $I_{COUTA/B} = GND$ $60$ $150$ $mA$ Rise or Fall Time $I_{r}$ , $I_{r}$ $10\%$ to $90\%$ , Figure 2 $10$ $25$ $ns$ Transmitter Input to Output $I_{PHL}$ , $I_{PLH}$ Figure 2 $0$ $0$ $0$ $0$ Data Skew $I_{PHL}$ , $I_{PLH}$ Figure 2 $0$ $0$ $0$ $0$ $0$ Output-to-Output Skew $0$ $0$ $0$ $0$ $0$ $0$ $0$ $0$ $0$ $0$ $0$ V11 RECEIVERDifferential Threshold Voltage $0$ </td <td></td> <td></td> <td>IVIAX3173</td> <td>V.11</td> <td>Mbps</td>			IVIAX3173	V.11				Mbps
Voltage VODO R = 1.95k2, Figure 1 4.0 6.0 V   Loaded Differential Output Voltage $V_{ODL}$ R = $50\Omega$ , Figure 1 $0.5 \times V_{ODO}$ V   Change in Magnitude of Output Differential Voltage $V_{OC}$ R = $50\Omega$ , Figure 1 $0.2$ V   Change in Magnitude of Output Voltage $V_{OC}$ R = $50\Omega$ , Figure 1 $0.2$ V   Change in Magnitude of Output Common-Mode Voltage $V_{OC}$ R = $50\Omega$ , Figure 1 $0.2$ V   Short-Circuit Current $V_{OC}$ R = $V_{OC}$ R	V.11 TRANSMITTER							
Voltage $VODL$ $R = SOQ$ , Figure 1 $0.5 \times VODO$ $V$ Change in Magnitude of Output Differential Voltage $VOC$ $R = SOQ$ , Figure 1 $0.2$ $V$ Common-Mode Output Voltage $VOC$ $R = SOQ$ , Figure 1 $0.2$ $V$ Change in Magnitude of Output Common-Mode Voltage $VOC$		V <sub>ODO</sub>	$R = 1.95k\Omega$ , F	igure 1	4.0		6.0	V
Differential Voltage $\Delta VOD$ $R = 50\Omega$ , Figure 1 $0.2$ $V$ Common-Mode Output Voltage $VOC$ $R = 50\Omega$ , Figure 1 $0.2$ $V$ Change in Magnitude of Output Common-Mode Voltage $\Delta VOC$ $R = 50\Omega$ , Figure 1 $0.2$ $V$ Short-Circuit Current $ISC$ $TOUTA/B = GND$ $0.2$ $V$ Rise or Fall Time $ISC$ $IS$	•	V <sub>ODL</sub>	$R = 50\Omega$ , Figu	ire 1	0.5 × V <sub>OI</sub>	00		V
Change in Magnitude of Output Common-Mode Voltage $\Delta V_{OC}$ R = 50Ω, Figure 10.2VShort-Circuit CurrentIsc $T_{-}OUTA/B = GND$ 60150mARise or Fall Time $t_r$ , $t_f$ 10% to 90%, Figure 21025nsTransmitter Input to Output $t_{PHL}$ , $t_{PLH}$ Figure 25080nsData Skew $t_{PHL} - t_{PLH}$ Figure 2210nsOutput-to-Output Skew $t_{SKEW}$ Figure 22nsChannel-to-Channel Skew2nsV.11 RECEIVERDifferential Threshold Voltage $V_{TH}$ $-7V \le V_{CM} \le +7V$ $-200$ $-100$ $-25$ mV		ΔV <sub>OD</sub>	$R = 50\Omega$ , Figu	ire 1			0.2	V
Common-Mode Voltage $AVOC$ $A$	Common-Mode Output Voltage	Voc	$R = 50\Omega$ , Figu	ire 1			3.0	V
Rise or Fall Time $t_r$ , $t_f$ 10% to 90%, Figure 2 10 25 ns Transmitter Input to Output $t_{PHL}$ , $t_{PLH}$ Figure 2 50 80 ns Data Skew $t_{PHL}$ - $t_{PLH}$ Figure 2 2 10 ns Output-to-Output Skew $t_{SKEW}$ Figure 2 2 ns Channel-to-Channel Skew 2 ns $t_{SKEW}$ Figure 2 2 ns $t_{PHL}$ Figur	0 ,	ΔV <sub>OC</sub>	$R = 50\Omega$ , Figu	ire 1			0.2	V
Transmitter Input to Output         t <sub>PHL</sub> , t <sub>PLH</sub> Figure 2         50         80         ns           Data Skew           t <sub>PHL</sub> - t <sub>PLH</sub>           Figure 2         2         10         ns           Output-to-Output Skew         t <sub>SKEW</sub> Figure 2         2         ns           Channel-to-Channel Skew         2         ns           V.11 RECEIVER           Differential Threshold Voltage         V <sub>TH</sub> -7V ≤ V <sub>CM</sub> ≤ +7V         -200         -100         -25         mV	Short-Circuit Current	Isc	T_OUTA/B =	GND		60	150	mA
Transmitter Input to Output $t_{PHL}$ , $t_{PLH}$ Figure 25080nsData Skew $t_{PHL}$ - $t_{PLH}$ Figure 2210nsOutput-to-Output Skew $t_{SKEW}$ Figure 22nsChannel-to-Channel Skew2nsV.11 RECEIVERDifferential Threshold Voltage $V_{TH}$ $-7V \le V_{CM} \le +7V$ $-200$ $-100$ $-25$ mV	Rise or Fall Time		10% to 90%,	igure 2		10	25	ns
Data Skew         I tPHL - tPLH         Figure 2         2         10         ns           Output-to-Output Skew         tSKEW         Figure 2         2         ns           Channel-to-Channel Skew         2         ns           V.11 RECEIVER           Differential Threshold Voltage         VTH         -7V ≤ VCM ≤ +7V         -200         -100         -25         mV	Transmitter Input to Output		Figure 2			50	80	ns
Output-to-Output Skew         t <sub>SKEW</sub> Figure 2         2         ns           Channel-to-Channel Skew         2         ns           V.11 RECEIVER           Differential Threshold Voltage         V <sub>TH</sub> -7V ≤ V <sub>CM</sub> ≤ +7V         -200         -100         -25         mV	Data Skew					2	10	ns
Channel-to-Channel Skew         2         ns           V.11 RECEIVER           Differential Threshold Voltage         V <sub>TH</sub> -7V ≤ V <sub>CM</sub> ≤ +7V         -200         -100         -25         mV	Output-to-Output Skew	tskew	Figure 2			2		ns
Differential Threshold Voltage $V_{TH}$ $-7V \le V_{CM} \le +7V$ $-200$ $-100$ $-25$ mV	Channel-to-Channel Skew					2		ns
	V.11 RECEIVER				•			
Input Hysteresis $\Delta V_{TH}$ $-7V \le V_{CM} \le +7V$ 5 15 mV	Differential Threshold Voltage	V <sub>TH</sub>	-7V ≤ V <sub>CM</sub> ≤ +	-7V	-200	-100	-25	mV
	Input Hysteresis	$\Delta V_{TH}$	-7V ≤ V <sub>CM</sub> ≤ +	-7V	5	15		mV

### **ELECTRICAL CHARACTERISTICS (continued)**

 $(V_{CC} = 3.3V \pm 5\%; C1 = C2 = 1\mu F, C3 = C4 = C5 = 3.3\mu F, and T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $V_{CC} = +3.3V, T_A = +25$ °C.) (Note 2)

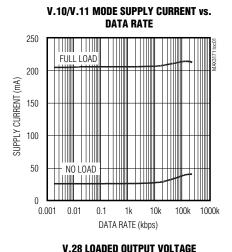
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
5		MAX3171	5	10	15	μs
Receiver Input to Output	tphL, tpLH	MAX3173		60	120	ns
5 . 0		MAX3171		0.5	4	μs
Data Skew	I tehl - tehl I	MAX3173		5	16	ns
V.10 TRANSMITTER						
Unloaded Output Voltage	V <sub>ODO</sub>	$R_L = 3.9k\Omega$ , Figure 3	±4.0	±4.4	±6.0	V
Loaded Output Voltage Swing	V <sub>ODL</sub>	$R_L = 450\Omega$ , Figure 3	0.9 × V <sub>ODO</sub>			V
Short-Circuit Current	Isc	T_OUTA = GND		±100	±150	mA
Transmitter Rise or Fall Time	t <sub>r</sub> , t <sub>f</sub>	$R_L = 450\Omega$ , $C_L = 100$ pF, Figure 3		2		μs
Transmitter Input to Output	tphl, tplh	$R_L = 450\Omega$ , $C_L = 100$ pF, Figure 3		2		μs
Data Skew	I t <sub>PHL</sub> - t <sub>PLH</sub> I	$R_L = 450\Omega$ , $C_L = 100$ pF, Figure 3		50		ns
V.10 RECEIVER						
Threshold Voltage	V <sub>TH</sub>		+25	+100	+300	mV
Input Hysteresis	$\Delta V_{TH}$			15		mV
Receiver Input to Output	tou tou	MAX3171, Figure 4	5	10	15	μs
	t <sub>PHL</sub> , t <sub>PLH</sub>	MAX3173, Figure 4		60	120	ns
Data Skew	I tehl - tehl I :	MAX3171, Figure 4		0.5	4	μs
Data Skew		MAX3173, Figure 4		5	16	ns
V.28 TRANSMITTER						
Output Voltage Swing	Vo	All transmitters loaded with $R_L = 3k\Omega$	±5.0	±5.4		V
Catput Voltago Cwing		No load			±6.5	
Short-Circuit Current	Isc	T_OUTA = GND		±25	±60	mA
Output Slew Rate	SR	$R_L = 3k\Omega$ , $C_L = 2500pF$ , measured from +3V to -3V or from -3V to +3V, Figure 3	4		30	V/µs
Output Siew hate	Sn	$R_L = 7k\Omega$ , $C_L = 150pF$ , measured from +3V to -3V or from -3V to +3V, Figure 3	6		30	ν/μ5
Transmitter Input to Output	tphL, tpLH	Figure 3		1		μs
Data Skew	I tpHL - tpLH I	Figure 3		100		ns
V.28 RECEIVER						
Input Threshold Low	VIL				0.8	V
Input Threshold High	VIH		2.0			V
Input Hysteresis	V <sub>HYS</sub>			0.5		V
Propagation Delay	tpLH, tpHL	MAX3171, Figure 4	5	10	15	
i Topayallon Delay		MAX3173, Figure 4		200		μs
Data Skew	I tour tour	MAX3171, Figure 4	0.5		4.0	μs
Daid SNEW	tphl - tplh	MAX3173, Figure 4		100		ns

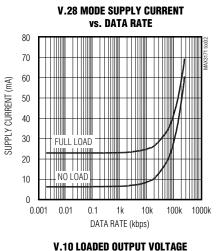
Note 2: V+ and V- are also used to supply the MAX3172/MAX3174. The MAX3171/MAX3173 are tested with additional current load on V+ and V- to capture the effect of loading from the MAX3172/MAX3174 in all operation modes.

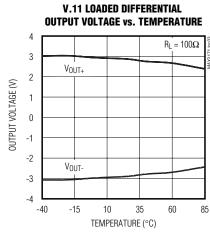
4 \_\_\_\_\_\_*\_\_\_\_/VI/XI/V*I

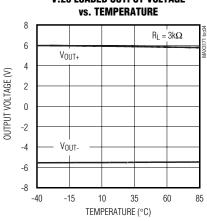
### Typical Operating Characteristics

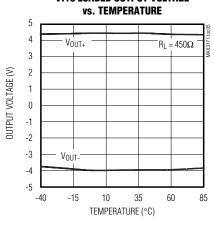
 $(V_{CC} = +3.3V, C1 = C2 = 1.0\mu F, C3 = C4 = C5 = 3.3\mu F, T_A = +25^{\circ}C, unless otherwise noted.)$ 

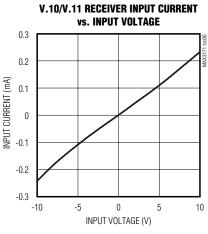


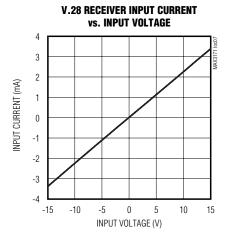


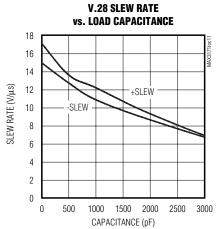


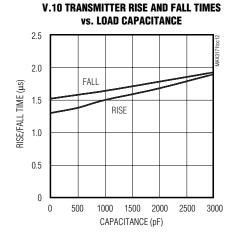






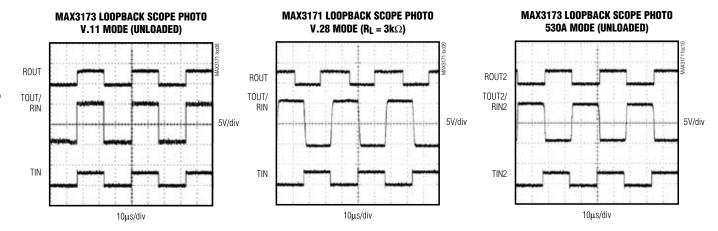






## \_Typical Operating Characteristics (continued)

 $(V_{CC} = +3.3V, C1 = C2 = 1.0\mu F, C3 = C4 = C5 = 3.3\mu F, T_A = +25^{\circ}C, unless otherwise noted.)$ 



### **Test Circuits**

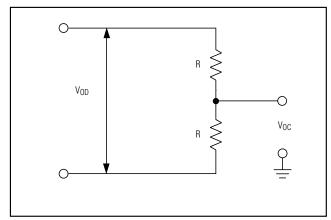


Figure 1. V.11 DC Test Circuit

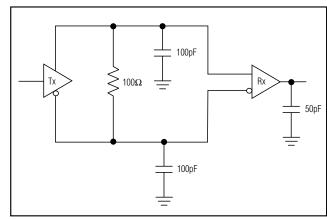
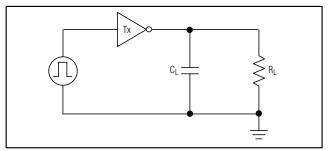


Figure 2. V.11 AC Test Circuit

### **Test Circuits (continued)**



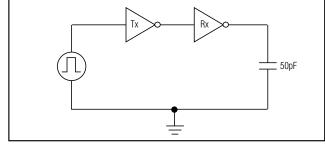


Figure 3. V.10/V.28 Driver Test Circuit

Figure 4. V.10/V.28 Receiver Test Circuit

## **Pin Description**

PIN	NAME	FUNCTION
1	V+	Positive Supply Generated by the Charge Pump (connect to V+ pin of MAX3172/MAX3174). Bypass V+ to ground with a 3.3µF ceramic capacitor.
2	C2+	Positive Terminal of the Inverting Charge-Pump Capacitor. Connect C2+ to C2- with a 1µF ceramic capacitor.
3	C2-	Negative Terminal of the Inverting Charge-Pump Capacitor. Connect C2+ to C2- with a 1µF ceramic capacitor.
4	V-	Negative Supply Generated by the Charge Pump (connect to V- pin of MAX3172/MAX3174). Bypass V- to ground with a 3.3µF ceramic capacitor.
5, 6, 7	T_IN	Transmitter CMOS Inputs (T1IN, T2IN, T3IN)
8, 9, 10	R_OUT	Receiver CMOS Outputs (R1OUT, R2OUT, R3OUT)
11, 12, 13	M_	Mode Select Inputs (M0, M1, M2). Internally pulled up to V <sub>CC</sub> . See Table 1 for detailed information.
14	DCE/DTE	DCE/ $\overline{\rm DTE}$ Mode Select Input. Logic level high selects DCE interface; logic level low selects DTE interface. Internally pulled up to VCC.
15, 18	R_INB	Noninverting Receiver Inputs (R3INB, R2INB)
16, 17	R_INA	Inverting Receiver Inputs (R3INA, R2INA)
19	T3OUTB/R1INB	Noninverting Transmitter Output/Noninverting Receiver Input
20	T3OUTA/R1INA	Inverting Transmitter Output/Inverting Receiver Input
21, 23	T_OUTB	Noninverting Transmitter Outputs (T2OUTB, T1OUTB)
22, 24	T_OUTA	Inverting Transmitter Outputs (T2OUTA, T1OUTA)
25	C1-	Negative Terminal of the Voltage-Doubler Charge-Pump Capacitor. Connect C1+ to C1- with a 1µF ceramic capacitor.
26	GND	Ground
27	V <sub>CC</sub>	+3.3V Supply Voltage (±5%). Bypass V <sub>CC</sub> to ground with a 3.3μF ceramic capacitor.
28	C1+	Positive Terminal of the Voltage-Doubler Charge-Pump Capacitor. Connect C1+ to C1- with a 1µF ceramic capacitor.

**Table 1. Mode Selection** 

PROTOCOL		LOGIC INPUTS			TRANSMITTERS			RECEIVERS		
	M2	M1	МО	DCE/DTE	T1	T2	Т3	R1	R2	R3
V.11	0	0	0	0	V.11	V.11	Z	V.11	V.11	V.11
RS-530A	0	0	1	0	V.11	V.10	Z	V.11	V.10	V.11
RS-530	0	1	0	0	V.11	V.11	Z	V.11	V.11	V.11
X.21	0	1	1	0	V.11	V.11	Z	V.11	V.11	V.11
V.35	1	0	0	0	V.28	V.28	Z	V.28	V.28	V.28
RS-449/V.36	1	0	1	0	V.11	V.11	Z	V.11	V.11	V.11
V.28/RS-232	1	1	0	0	V.28	V.28	Z	V.28	V.28	V.28
No cable	1	1	1	0	Z	Z	Z	Z	Z	Z
V.11	0	0	0	1	V.11	V.11	V.11	Z	V.11	V.11
RS-530A	0	0	1	1	V.11	V.10	V.11	Z	V.10	V.11
RS-530	0	1	0	1	V.11	V.11	V.11	Z	V.11	V.11
X.21	0	1	1	1	V.11	V.11	V.11	Z	V.11	V.11
V.35	1	0	0	1	V.28	V.28	V.28	Z	V.28	V.28
RS-449/V.36	1	0	1	1	V.11	V.11	V.11	Z	V.11	V.11
V.28/RS-232	1	1	0	1	V.28	V.28	V.28	Z	V.28	V.28
No cable	1	1	1	1	Z	Z	Z	Z	Z	Z

Z = High impedance

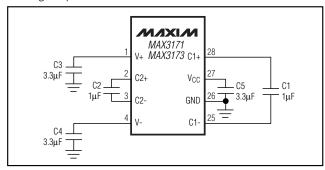


Figure 5. Charge-Pump Connections

### **Detailed Description**

The MAX3171/MAX3173 are three-driver/three-receiver multiprotocol transceivers that operate from a single +3.3V supply. The MAX3171/MAX3173, along with the MAX3170 and MAX3172/MAX3174, form a complete software-selectable DTE or DCE interface port that supports the V.28 (RS-232), V.10/V.11 (RS-449, V.36, EIA-530, EIA-530-A, X.21, RS-423), and V.35 protocols. The MAX3171/MAX3173 carry the control signals, while the MAX3170 transceiver carries the high-speed clock and data signals. The MAX3172/MAX3174 provide termination for the clock and data signals and have an extra transceiver for applications requiring four transceivers for control handshaking.

The MAX3171/MAX3173 feature a 2mA no-cable mode, true fail-safe operation, and thermal shutdown circuitry. Thermal shutdown protects the drivers against excessive power dissipation. When activated, the thermal shutdown circuitry places the driver outputs into a high-impedance state.

#### **Mode Selection**

The state of mode select pins M0, M1, and M2 determines which serial interface protocol is selected (Table 1). The state of the DCE/DTE input determines whether the transceivers will be configured as a DTE serial port or a DCE serial port. When the DCE/DTE input is logic HIGH, driver T3 is activated and receiver R1 is disabled. When the DCE/DTE input is logic LOW, driver T3 is disabled and receiver R1 is activated. M0, M1, M2, and DCE/DTE are internally pulled up to VCC to ensure logic HIGH if left unconnected.

The MAX3171/MAX3173's mode can be selected through software control of the M0, M1, M2, and DCE/DTE inputs. Alternatively, the mode can be selected by shorting the appropriate combination of mode control inputs to GND (the inputs left floating will be internally pulled up to V<sub>CC</sub>). If the M0, M1, and M2 mode inputs are all unconnected, the MAX3171/MAX3173 will enter no-cable mode.

#### **No-Cable Mode**

The MAX3171/MAX3173 enter no-cable mode when the mode select pins are left unconnected or tied HIGH (M0 = M1 = M2 = 1). In this mode, the multiprotocol drivers and receivers are disabled and the supply current is less than 8mA. The receiver outputs enter a high-impedance state in no-cable mode, which allows these output lines to be shared with other receivers (the receiver outputs have an internal pullup resistor to pull the outputs HIGH if not driven). Also, in no-cable mode, the transmitter outputs enter a high-impedance state, so these output lines can be shared with other devices.

#### **Dual Charge-Pump Voltage Converter**

The MAX3171/MAX3173 internal power supply consists of a regulated dual charge pump that provides positive and negative output voltages from a +3.3V supply. The charge pump operates in discontinuous mode: If the output voltage is less than the regulated voltage, the charge pump is enabled; if the output voltage exceeds the regulated voltage, the charge pump is disabled. Each charge pump requires a flying capacitor (C1, C2) and a reservoir capacitor (C3, C4) to generate the V+ and V- supplies. See Figure 5 for charge-pump connections.

The charge pump is designed to supply V+ and V-power to the MAX3172/MAX3174 in addition to the MAX3171/MAX3173 internal transceivers. Connect the MAX3172/MAX3174 V+ and V- terminals to the MAX3171/MAX3173 V+ and V- terminals, respectively.

#### Fail-Safe

The MAX3171/MAX3173 guarantee a logic HIGH receiver output when the receiver inputs are shorted or open, or when they are connected to a terminated transmission line with drivers disabled. The V.11 receiver threshold is set between -25mV and -200mV to guarantee fail-safe operation. If the differential receiver input voltage (B - A) is  $\geq$  -25mV, R\_OUT is logic HIGH. In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to 0 by the termination. With the MAX3171/MAX3173 receiver thresholds, this results in R\_OUT logic HIGH with a 25mV (min) noise margin.

The V.10 receiver threshold is set between +25mV and +300mV. If the V.10 receiver input voltage is  $\leq$  +25mV, ROUT is logic HIGH. The V.28 receiver threshold is set between 0.8V and 2.0V. If the receiver input voltage is  $\leq$  0.8V, ROUT is logic HIGH. In the case of a terminated bus with transmitters disabled, the V.10/V.28 receiver's input voltage is pulled to ground by the termination. With the MAX3172/MAX3174 receiver thresholds, this results in R\_OUT logic HIGH.

### **Applications Information**

#### **Capacitor Selection**

The capacitors used for the charge pumps, as well as the supply bypassing, should have a low-ESR and low-temperature coefficient. Multilayer ceramic capacitors with an X7R dielectric offer the best combination of performance, size, and cost. The flying capacitors (C1, C2) should have a value of  $1\mu F$ , while the reservoir capacitors (C3, C4) and bypass capacitor (C5) should have a minimum value of  $3.3\mu F$  (Figure 5). To reduce the ripple present on the transmitter outputs, capacitors C3, C4, and C5 can be increased. Do not increase the value of C1 and C2.

#### **Local Loopback Control Signal**

For applications that require the use of local loopback (LL) signal routing, an extra transceiver is available for use on the MAX3172/MAX3174 multiprotocol termination network device.

#### Cable-Selectable Mode

Figure 6 shows a cable-selectable mulitprotocol interface. The mode control lines (M0, M1, M2, and DCE/DTE) are wired to the DB-25 connector. To select the serial interface mode, the appropriate combinations of M0, M1, M2, and DCE/DTE are grounded within the cable wiring. The control lines that are not grounded are pulled high by the internal pullups on the MAX3170. The serial interface protocol of the MAX3171/MAX3173 (MAX3170 and MAX3172/MAX3174) is now selected based on the cable connected to the DB-25 interface.

### V.11 (RS-422) Interface

As shown in Figure 7, the V.11 protocol is a fully balanced differential interface. The V.11 driver generates  $\pm 2V$  (min) between nodes A and B when  $100\Omega$  (min) resistance is presented at the load. The V.11 receiver is sensitive to  $\pm 200$ mV differential signals at the receiver inputs A' and B'. The V.11 receiver input must comply with the impedance curve of Figure 8 and reject common-mode signals up to  $\pm 7V$  developed across the cable (referenced from C to C' in Figure 7).

The MAX3171/MAX3173 V.11 mode receiver has a differential threshold between -200mV and -25mV to ensure that the receiver has proper fail-safe operation (see Fail-Safe). To aid in rejecting system noise, the MAX3171/MAX3173 V.11 receiver has a 15mV (typ) hysteresis. Switch S3 in Figure 9 is open in V.11 mode to disable the V.28  $5k\Omega$  termination at the inverting receiver input. Because the control signals are slow (64kbps),  $100\Omega$  termination resistance is generally not required for the MAX3171/MAX3173.

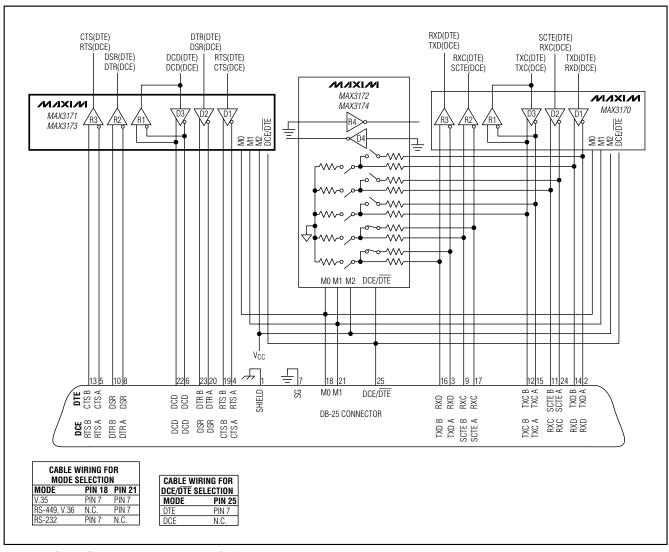


Figure 6. Cable-Selectable Multiprotocol DCE/DTE Port

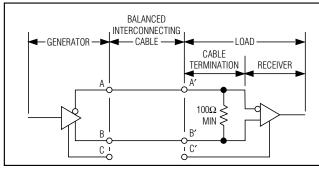


Figure 7. Typical V.11 Interface

#### V.10 Interface

The V.10 interface (Figure 10) is an unbalanced single-ended interface capable of driving a 450 $\Omega$  load. The V.10 driver generates a  $\pm 4V$  (min)  $V_{ODO}$  voltage across A' and C' when unloaded and a minimum of  $\pm 0.9 \times V_{ODO}$  voltage with a 450 $\Omega$  load. The V.10 receiver input trip threshold is defined between +300mV and -300mV with the input impedance characteristic shown in Figure 8.

The MAX3171/MAX3173 V.10 mode receiver has a threshold between +25mV and +300mV to ensure that the receiver has proper fail-safe operation (see *Fail-*

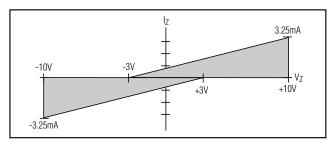


Figure 8. Receiver Input Impedance Curve

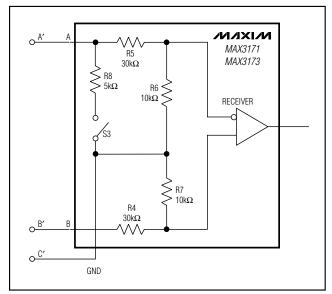


Figure 9. V.11 Termination and Internal Resistance Networks

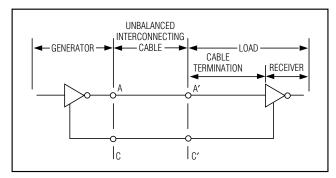


Figure 10. Typical V.10/V.28 Interface

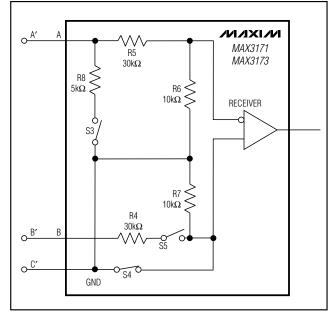


Figure 11. V.10 Internal Resistance Network

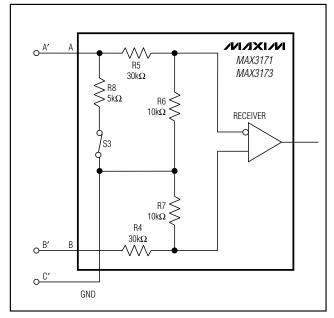


Figure 12. V.28 Termination and Internal Resistance Networks

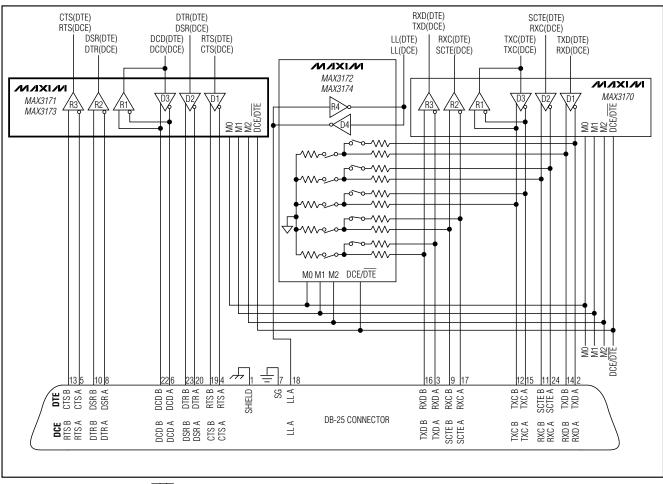


Figure 13. Multiprotocol DCE/DTE Port

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Safe). To aid in rejecting system noise, the MAX3171/MAX3173 V.10 receiver has 15mV (typ) hysteresis. Switch S3 in Figure 11 is open in V.10 mode to disable the 5k $\Omega$  V.28 termination at the receiver input. Switch S4 is closed, and switch S5 is open to internally ground the receiver B input.

#### V.28 Interface

The V.28 interface is an unbalanced single-ended interface (Figure 12). The V.28 generator provides  $\pm 5$ V (min) across the load impedance between A' and C'. The V.28 standard specifies input trip points at  $\pm 3$ V.

The MAX3171/MAX3173 V.28 mode receiver has a threshold between +0.8V and +2.0V to ensure that the receiver has proper fail-safe operation (see *Fail-Safe*). To aid in rejecting system noise, the MAX3171/MAX3173 V.28 receiver has a 500mV (typ) hysteresis. Switch S3 in

Figure 12 is closed in V.28 mode to enable the  $5\text{k}\Omega$  V.28 termination at the receiver input.

#### **Receiver Glitch Rejection**

To facilitate operation in an unterminated or otherwise noisy system, the MAX3171 features 10µs of receiver input glitch rejection in V.10, V.11, and V.28 modes. The glitch rejection circuitry blocks the reception of high-frequency noise (tg < 5µs) while receiving a low-frequency signal (tg > 15µs), allowing glitch-free operation in unterminated systems at up to 64kbps. The MAX3173 does not have this feature and can be operated at data rates up to 240kbps if properly terminated.

#### **DTE vs. DCE Operation**

Figure 13 shows a DCE or DTE controller-selectable interface. The DCE/DTE input switches the port's mode of operation. A logic high selects DCE, which enables

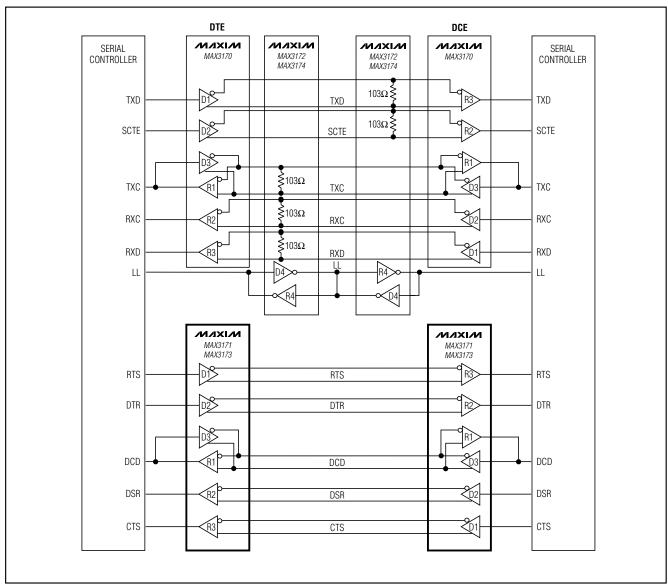


Figure 14. DCE-to-DTE X.21 Interface

driver 3 on the MAX3171/MAX3173, driver 3 on the MAX3170, and driver 4 on the MAX3172/MAX3174. A logic low selects DTE, which enables receiver 1 on the MAX3171/MAX3173, receiver 1 on the MAX3170, and receiver 4 on the MAX3172/MAX3174.

This application requires only one DB-25 connector. See Figure 13 for complete signal routing in DCE and DTE modes. For example, driver 3 routes the DCD (DCE) signal to pins 22 and 6 in DCE mode, while in DTE mode, receiver 1 routes pins 22 and 6 to DCD (DTE).

#### Complete Multiprotocol X.21 Interface

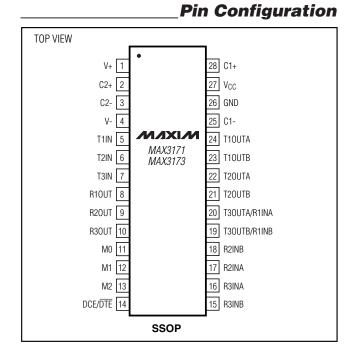
Figure 14 shows a complete DCE-to-DTE interface operating in X.21 mode. The MAX3171/MAX3173 generate the control signals, and the MAX3170 is used to generate the clock and data signals. The MAX3172/MAX3174 generate local loopback and are used to terminate the clock and data signals to support the V.11 protocol for cable termination. The control signals do not need external termination.

#### **Compliance Testing**

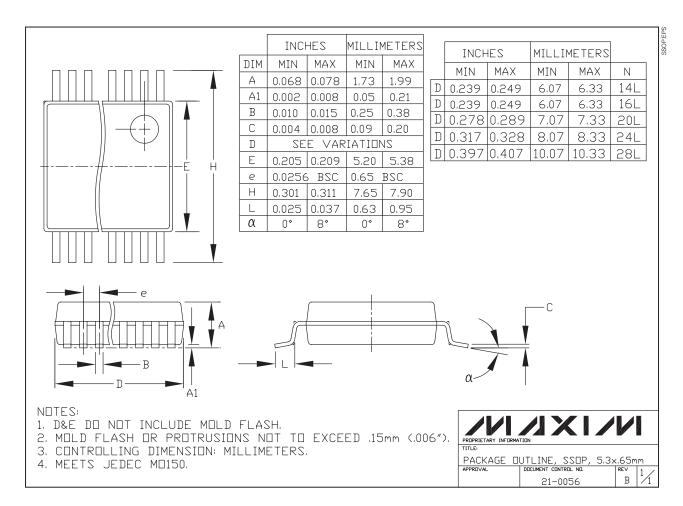
A European Standard EN 45001 test report is available for the MAX3170–MAX3174 chipset. A copy of the test report will be available from Maxim.

### \_Chip Information

TRANSISTOR COUNT: 1763
PROCESS: BICMOS



### **Package Information**



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