TPS7A8300 2-A, 6-μV$_{RMS}$, RF, LDO Voltage Regulator

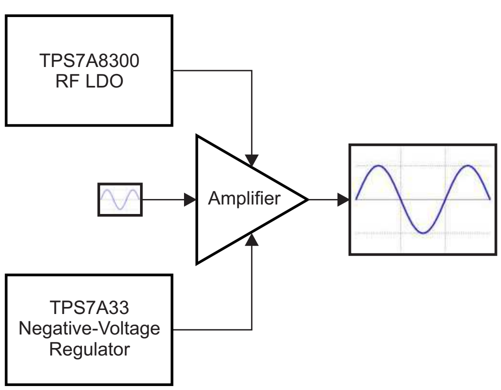
1 Features

- Ultralow Dropout: 125 mV Maximum at 2 A
- Output Voltage Noise: 6 μV$_{RMS}$
- Power-Supply Ripple Rejection:
  - 40 dB at 1 MHz
- Input Voltage Range:
  - Without BIAS: 1.4 V to 6.5 V
  - With BIAS: 1.1 V to 6.5 V
- Two Output Voltage Modes:
  - ANY-OUT™ Version (User-Programmable Output via PCB Layout):
    - No External Resistor Required
    - Output Voltage Range: 0.8 V to 3.95 V
  - Adjustable Version:
    - Output Voltage Range: 0.8 V to 5.0 V
- 1.0% Accuracy Over Line, Load, and Temperature
- Stable with a 22-μF Output Ceramic Capacitor
- Programmable Soft-Start Output
- Power-Good (PG) Output
- Available Packages:
  - 5-mm × 5-mm VQFN-20
  - 3.5-mm × 3.5-mm VQFN-20

2 Applications

- RF, IF Components: VCO, ADC, DAC, LVDS
- Wireless Infrastructure: SerDes, FPGA, DSP™
- Test and Measurement
- Instrumentation, Medical, and Audio

Application Example



3 Description

The TPS7A8300 is a low-noise (6 μV$_{RMS}$), low-dropout voltage regulator (LDO) capable of sourcing a 2-A load with only 125 mV of maximum dropout.

The TPS7A8300 output voltages are fully user-adjustable (up to 3.95 V) using a printed circuit board (PCB) layout without the need of external resistors, thus reducing overall component count. For higher output voltage applications, the device achieves output voltages up to 5 V with the use of external resistors. The device supports very low input voltages (down to 1.1 V) with the use of an additional BIAS rail.

With very high accuracy (1% over line, load, and temperature), remote sensing, and soft-start capabilities to reduce inrush current, the TPS7A8300 is ideal for powering high-current, low-voltage devices such as high-end microprocessors and field-programmable gate arrays (FPGAs).

The TPS7A8300 is designed to power-up noise-sensitive components in high-speed communication applications. The very low-noise, 6-μV$_{RMS}$ device output and high broad-bandwidth PSRR (40 dB at 1 MHz) minimizes phase noise and clock jitter in high-frequency signals. These features maximize performance of clocking devices, analog-to-digital converters (ADCs), and digital-to-analog converters (DACs).

For applications where positive and negative low-noise rails are required, consider TI's TPS7A33 family of negative high-voltage, ultralow-noise linear regulators.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7A8300	VQFN (20)	5.00 mm × 5.00 mm
	VQFN (20)	3.50 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (August 2014) to Revision F	Page
• Added title to page 1 graphic	1
• Updated *ESD Ratings* table to current standards	5
• Changed Figure 52: changed connection of EN pin	21
• Changed *Enable (EN) and Undervoltage Lockout (UVLO)* section: updated wording for better clarity on use of the Enable (EN) pin	25

Changes from Revision D (February 2013) to Revision E	Page
• Changed format to meet latest data sheet standards; added new sections, and moved existing sections	1
• Changed first *ANY-OUT* sub-bullet of fifth Features bullet	1
• Changed eighth Features bullet: broke *Soft-Start Output* and *PG Output* into two separate Features bullets	1
• Changed first sentence of second paragraph in *Description* section	1
• Changed RGW and RGR drawings: removed spacing between number and unit in pins 5 to 7 and 9 to 11	4
• Changed first row of *Pin Functions* table: deleted spacing between number and unit in pin names	4
• Added capacitor value to BIAS pin description in *Pin Functions* table	4
• Changed 87% to 89% in the PG pin description of the *Pin Functions* table	4
• Changed thermal pad description in *Pin Functions* table	4
• Changed conditions statements for *Absolute Maximum Ratings* and *Recommended Operating Conditions* tables	5
• Added *Recommended Operating Conditions* table	5
• Changed the *Typical Characteristics* section: changed all curve titles and conditions	8
• Changed title of Figure 11	8
• Added *Overview* section	17
• Changed second paragraph of *Overview* section: changed *that can be groups, as follows* to *including*	17
• Changed functional block diagram footnote	17
• Added *Feature Description* section	18
• Changed *adjustable version* to *adjustable configuration* in first paragraph of *Adjustable Operation* section	19

Changes from Revision C (July 2013) to Revision D **Page**

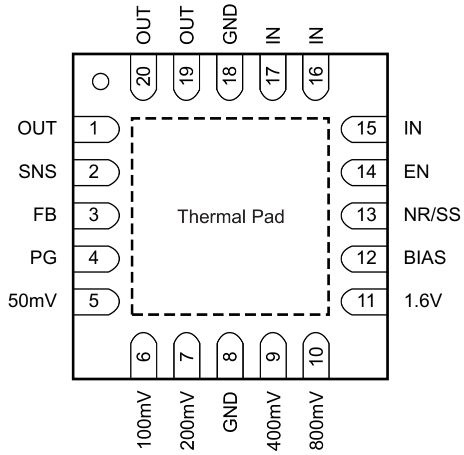
Changes from Revision B (July 2013) to Revision C **Page**

Changes from Revision A (June 2013) to Revision B **Page**

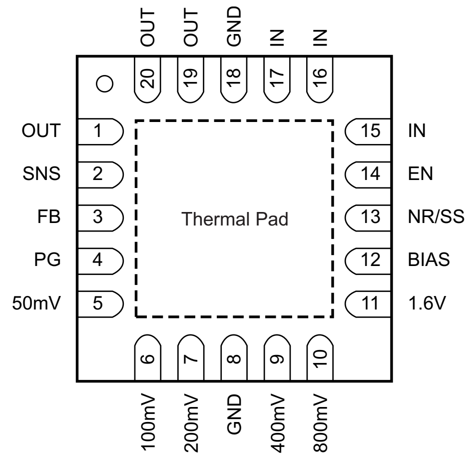
Changes from Original (May 2013) to Revision A **Page**

5 Pin Configurations and Functions

RGW Package
5-mm × 5-mm VQFN-20
Top View



RGR Package
3.5-mm × 3.5-mm VQFN-20
Top View



Pin Functions

PIN			DESCRIPTION
NAME	NO.	I/O	
50mV, 100mV, 200mV, 400mV, 800mV, 1.6V	5, 6, 7, 9, 10, 11	I	Output voltage setting pins. Connect these pins to ground or leave floating. Connecting these pins to ground increases the output voltage by the value of the pin name; multiple pins can be simultaneously connected to GND to select the desired output voltage. Leave these pins floating (open) when not in use. See the *ANY-OUT Programmable Output Voltage* section for more details.
BIAS	12	I	BIAS supply voltage pin for the use of 1.1 V ≤ V_{IN} ≤ 1.4 V and to connect a 10-µF capacitor between this pin and ground.
EN	14	I	Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low disables the device. See the *Start-Up* section for more details.
FB	3	I	Output voltage feedback pin connected to the error amplifier. Although not required, a 10-nF feed-forward capacitor from FB to OUT (as close to the device as possible) is recommended for low-noise applications to maximize ac performance. The use of a feed-forward capacitor may disrupt PG (power good) functionality. See the *ANY-OUT Programmable Output Voltage* and *Adjustable Operation* sections for more details.
GND	8, 18	—	Ground pin. These pins must be externally shorted for the RGR package option.
IN	15-17	I	Input supply voltage pin. A 10-µF input ceramic capacitor is required. See the *Input and Output Capacitor Requirements (C_{IN} and C_{OUT})* section for more details.
OUT	1, 19, 20	O	Regulated output pin. A 22-µF or larger ceramic capacitor is required for stability (a 10-µF minimum effective capacitance is required). See the *Input and Output Capacitor Requirements (C_{IN} and C_{OUT})* section for more details.
PG	4	O	Active-high power-good pin. An open-drain output indicates when the output voltage reaches 89% of the target. The use of a feed-forward capacitor may disrupt PG (power good) functionality. See the *Power-Good Function* section for more details.
SNS	2	I	Output voltage sense input pin. Connect this pin only if the ANY-OUT feature is used. See the *ANY-OUT Programmable Output Voltage* and *Adjustable Operation* sections for more details.
NR/SS	13	—	Noise-reduction and soft-start pin. Connecting an external capacitor between this pin and ground reduces reference voltage noise and also enables the soft-start function. Although not required, a capacitor is recommended for low-noise applications to connect a 10-nF capacitor from NR/SS to GND (as close to the device as possible) to maximize ac performance. See the *Noise-Reduction and Soft-Start Capacitor ($C_{NR/SS}$)* section for more details.
Thermal Pad	Pad	—	Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND.

6 Specifications

6.1 Absolute Maximum Ratings

over junction temperature range (unless otherwise noted) [1]

		MIN	MAX	UNIT
Voltage	IN, BIAS, PG, EN	–0.3	7.0	V
	IN, BIAS, PG, EN (5% duty cycle)	–0.3	7.5	
	SNS, OUT	–0.3	V_{IN} + 0.3 [2]	
	NR/SS, FB	–0.3	3.6	
	50mV, 100mV, 200mV, 400mV, 800mV, 1.6V	–0.3	V_{OUT} + 0.3	
Current	OUT	Internally limited		A
	PG (sink current into device)		5	mA
Operating junction temperature, T_J		–55	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is V_{IN} + 0.3 V or 7.0 V, whichever is smaller.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 [2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input supply voltage range	1.1	6.5	V
V_{BIAS}	Bias supply voltage range [1]	3.0	6.5	V
I_{OUT}	Output current	0	2	A
T_J	Operating junction temperature	–40	125	°C

(1) BIAS supply is required when the V_{IN} supply is below 1.4 V. Conversely, no BIAS supply is needed when the V_{IN} supply is higher than or equal to 1.4 V.

6.4 Thermal Information

THERMAL METRIC [1]		TPS7A8300 RGW (QFN) 20 PINS	TPS7A8300 RGR (QFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.6	35.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30.0	47.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.0	12.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.0	12.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.6	1.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over operating temperature range (T_J = –40°C to 125°C), {1.1 V ≤ V_{IN} < 1.4 V and 3.0 V ≤ V_{BIAS} ≤ 6.5 V} or {V_{IN} ≥ 1.4 V and V_{BIAS} open}(1), V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.3 V(2), $V_{OUT(TARGET)}$ = 0.8 V, OUT connected to 50 Ω to GND(3), V_{EN} = 1.1 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up to V_{IN} with 100 kΩ, unless otherwise noted.
Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input supply voltage range		1.1		6.5	V
V_{BIAS}	Bias supply voltage range(1)		3.0		6.5	V
$V_{(REF)}$	Reference voltage	$V_{(REF)} = V_{(FB)} = V_{(NR/SS)}$		0.8		V
$V_{UVLO1(IN)}$	Input supply UVLO with BIAS	V_{IN} increasing		1.02	1.085	V
$V_{HYS1(IN)}$	$V_{UVLO1(IN)}$ hysteresis			320		mV
$V_{UVLO2(IN)}$	Input supply UVLO without BIAS	V_{IN} increasing		1.31	1.39	V
$V_{HYS2(IN)}$	$V_{UVLO2(IN)}$ hysteresis			253		mV
$V_{UVLO(BIAS)}$	Bias supply UVLO	V_{BIAS} increasing		2.83	2.9	V
$V_{HYS(BIAS)}$	$V_{UVLO(BIAS)}$ hysteresis			290		mV
V_{OUT}	Output voltage range	Using voltage setting pins (50mV, 100mV, 200mV, 400mV, 800mV, and 1.6V)	0.8 – 1.0%		3.95 + 1.0%	V
		Using external resistors	0.8 – 1.0%		5.0 + 1.0%	V
	Output voltage accuracy(4)(5)	0.8 V ≤ V_{OUT} ≤ 5 V, 5 mA ≤ I_{OUT} ≤ 2 A	–1.0%		1.0%	
		V_{IN} = 1.5 V, V_{OUT} = 1.2 V, 5 mA ≤ I_{OUT} ≤ 1.2 A	–1.0%		1.0%	
$\Delta V_{O(\Delta VI)}$	Line regulation	I_{OUT} = 5 mA, 1.4 V ≤ V_{IN} ≤ 6.5 V		0.003		%/V
$\Delta V_{O(\Delta IO)}$	Load regulation	5 mA ≤ I_{OUT} ≤ 2 A		0.0001		%/A
$V_{(DO)}$	Dropout voltage	V_{IN} ≥ 1.4 V and V_{BIAS} open, 0.8 V ≤ V_{OUT} ≤ 5.0 V, I_{OUT} = 2 A, V_{FB} = 0.8 V – 3%			200	mV
		V_{IN} = 1.1 V, V_{BIAS} = 5.0 V, $V_{OUT(TARGET)}$ = 0.8 V, I_{OUT} = 2 A, V_{FB} = 0.8 V – 3%			125	mV
$I_{(LIM)}$	Output current limit	V_{OUT} forced at 0.9 × $V_{OUT(TARGET)}$, V_{IN} = $V_{OUT(TARGET)}$ + 300 mV	2.1	3.4	4.2	A
$I_{(GND)}$	GND pin current	Minimum load, V_{IN} = 6.5 V, no V_{BIAS} supply, I_{OUT} = 5 mA		2.8	4	mA
		Maximum load, V_{IN} = 1.4 V, no V_{BIAS} supply, I_{OUT} = 2 A		3.7	5	mA
		Shutdown, PG = (open), V_{IN} = 6.5 V, no V_{BIAS} supply, $V_{(EN)}$ = 0.5 V			2.5	µA
$I_{(EN)}$	EN pin current	V_{IN} = 6.5 V, no V_{BIAS} supply, $V_{(EN)}$ = 0 V and 6.5 V	–0.1		0.1	µA
$I_{(BIAS)}$	BIAS pin current	V_{IN} = 1.1 V, V_{BIAS} = 6.5 V, $V_{OUT(TARGET)}$ = 0.8 V, I_{OUT} = 2 A		2.3	3.5	mA
$V_{IL(EN)}$	EN pin low-level input voltage (disable device)		0		0.5	V
$V_{IH(EN)}$	EN pin high-level input voltage (enable device)		1.1		6.5	V

(1) BIAS supply is required when the V_{IN} supply is below 1.4 V. Conversely, no BIAS supply is needed when the V_{IN} supply is higher than or equal to 1.4 V.
(2) $V_{OUT(TARGET)}$ is the calculated V_{OUT} target value from the output voltage setting pins: 50mV, 100mV, 200mV, 400mV, 800mV, and 1.6V in a fixed configuration. In an adjustable configuration, $V_{OUT(TARGET)}$ is the expected V_{OUT} value set by the external feedback resistors.
(3) This 50-Ω load is disconnected when the test conditions specify an I_{OUT} value.
(4) When the device is connected to external feedback resistors at the FB pin, external resistor tolerances are not included.
(5) The device is not tested under conditions where V_{IN} > V_{OUT} + 2.5 V and I_{OUT} = 2 A, because the power dissipation is higher than the maximum rating of the package. Also, this accuracy specification does not apply on any application condition that exceeds the power dissipation limit of the package under test.

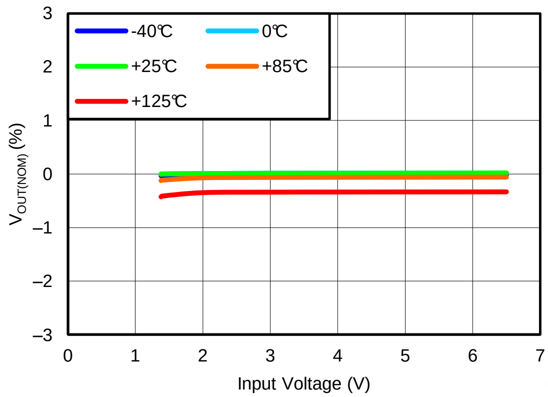
Electrical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), {1.1 V ≤ V_{IN} < 1.4 V and 3.0 V ≤ V_{BIAS} ≤ 6.5 V} or {V_{IN} ≥ 1.4 V and V_{BIAS} open}[1], V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.3 V[2], $V_{OUT(TARGET)}$ = 0.8 V, OUT connected to 50 Ω to GND[3], V_{EN} = 1.1 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up to V_{IN} with 100 kΩ, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT(PG)}$	PG pin threshold	For the direction PG↓ with decreasing V_{OUT}	0.82 V_{OUT}	0.872 V_{OUT}	0.93 V_{OUT}	V
$V_{hys(PG)}$	PG pin hysteresis	For PG↑		0.02 V_{OUT}		V
$V_{OL(PG)}$	PG pin low-level output voltage	V_{OUT} < $V_{IT(PG)}$, I_{PG} = –1 mA (current into device)			0.4	V
$I_{lkg(PG)}$	PG pin leakage current	V_{OUT} > $V_{IT(PG)}$, $V_{(PG)}$ = 6.5 V			1	µA
$I_{(NR/SS)}$	NR/SS pin charging current	$V_{NR/SS}$ = GND, V_{IN} = 6.5 V	4.0	6.2	9.0	µA
I_{FB}	FB pin leakage current	V_{IN} = 6.5 V	–100		100	nA
PSRR	Power-supply ripple rejection	f = 1 MHz, V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} = 2 A, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF		40		dB
V_n	Output noise voltage	BW = 10 Hz to 100 kHz, V_{IN} = 1.4 V, V_{OUT} = 0.8 V, I_{OUT} = 1.5 A, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF		6		μV_{RMS}
T_{sd}	Thermal shutdown temperature	Shutdown, temperature increasing		160		°C
		Reset, temperature decreasing		140		
T_J	Operating junction temperature		–40		125	°C

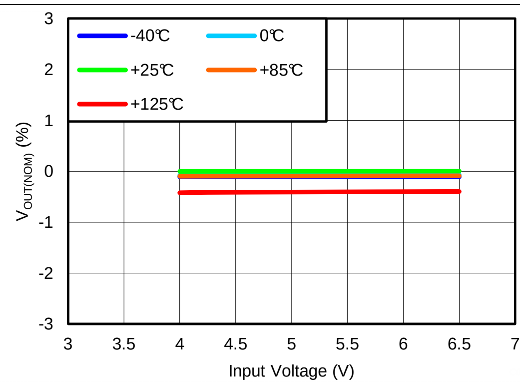
6.6 Typical Characteristics

At T_J = 25°C, {1.1 V ≤ V_{IN} < 1.4 V and 3.0 V ≤ V_{BIAS} ≤ 6.5 V} or {V_{IN} ≥ 1.4 V and V_{BIAS} open} (6), V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.3 V, $V_{OUT(TARGET)}$ = 0.8 V, OUT connected to 50 Ω to GND, V_{EN} = 1.1 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 10 nF, and PG pin pulled up to V_{IN} with 100 kΩ, unless otherwise noted.



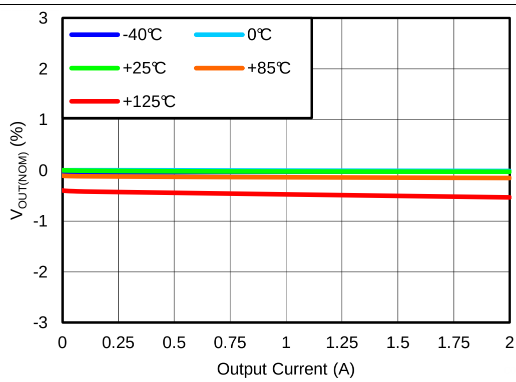
$V_{OUT(TARGET)}$ = 0.8 V, I_{OUT} = 5 mA, V_{BIAS} = Open

Figure 1. Minimum ANY-OUT V_{OUT} Line Regulation



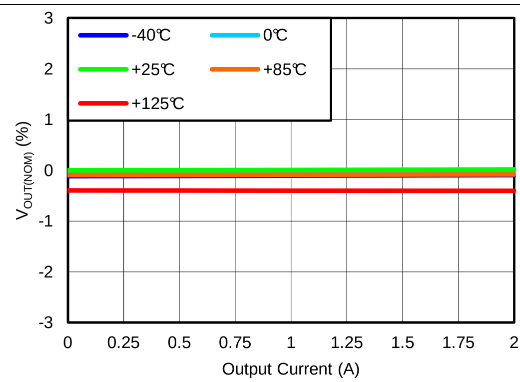
$V_{OUT(TARGET)}$ = 3.95 V, I_{OUT} = 5 mA, V_{BIAS} = Open

Figure 2. Maximum ANY-OUT V_{OUT} Line Regulation



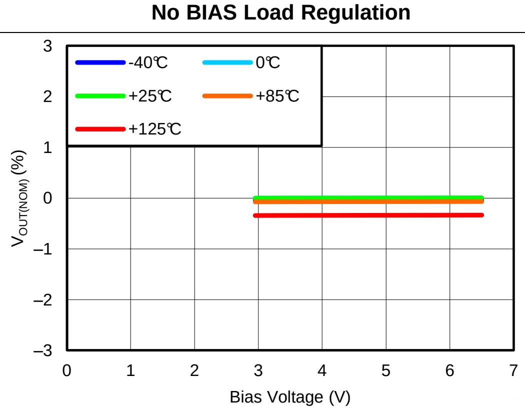
$V_{OUT(TARGET)}$ = 0.8 V, V_{IN} = 1.4 V, V_{BIAS} = Open

Figure 3. Minimum ANY-OUT V_{OUT}, Minimum V_{IN}, No BIAS Load Regulation



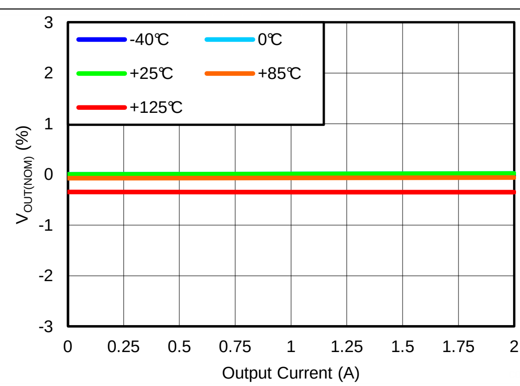
$V_{OUT(TARGET)}$ = 3.95 V, V_{IN} = 4.25 V, V_{BIAS} = Open

Figure 4. Maximum ANY-OUT V_{OUT} Load Regulation



$V_{OUT(TARGET)}$ = 0.8 V, V_{IN} = 1.1 V, I_{OUT} = 5 mA

Figure 5. Minimum ANY-OUT V_{OUT}, Minimum V_{IN} BIAS Line Regulation



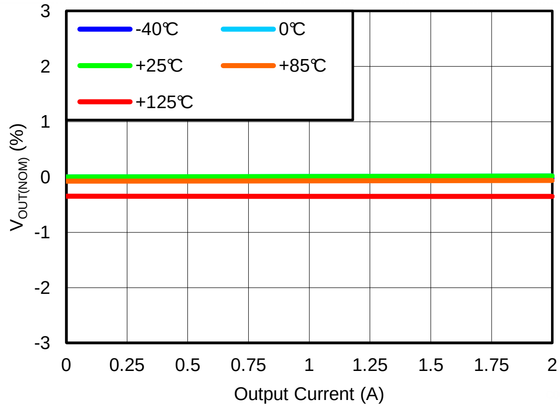
$V_{OUT(TARGET)}$ = 0.8 V, V_{IN} = 1.1 V, V_{BIAS} = 3 V

Figure 6. Minimum ANY-OUT V_{OUT}, V_{IN}, and BIAS Load Regulation

(6) BIAS supply is required when the V_{IN} supply is below 1.4 V. Conversely, no BIAS supply is needed when the V_{IN} supply is higher than or equal to 1.4 V.

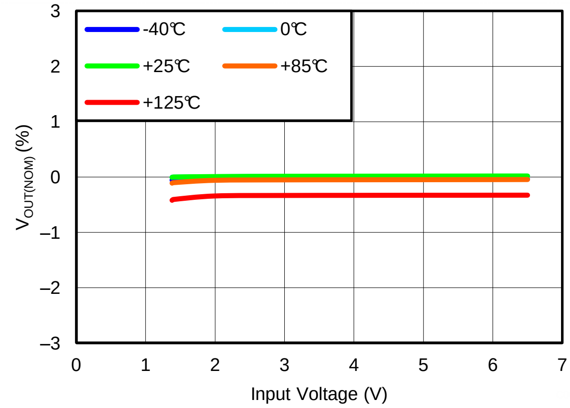
Typical Characteristics (continued)

At T_J = 25°C, {1.1 V ≤ V_{IN} < 1.4 V and 3.0 V ≤ V_{BIAS} ≤ 6.5 V} or {V_{IN} ≥ 1.4 V and V_{BIAS} open} (1), V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.3 V, $V_{OUT(TARGET)}$ = 0.8 V, OUT connected to 50 Ω to GND, V_{EN} = 1.1 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 10 nF, and PG pin pulled up to V_{IN} with 100 kΩ, unless otherwise noted.



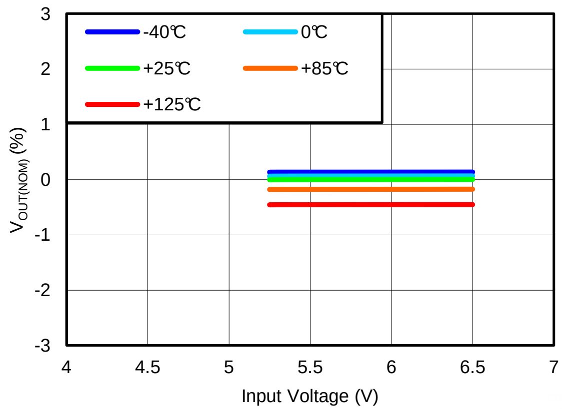
$V_{OUT(TARGET)}$ = 0.8 V, V_{IN} = 1.1 V, V_{BIAS} = 6.5 V

Figure 7. Minimum Adjustable V_{OUT}, Minimum V_{IN}, Maximum BIAS Load Regulation



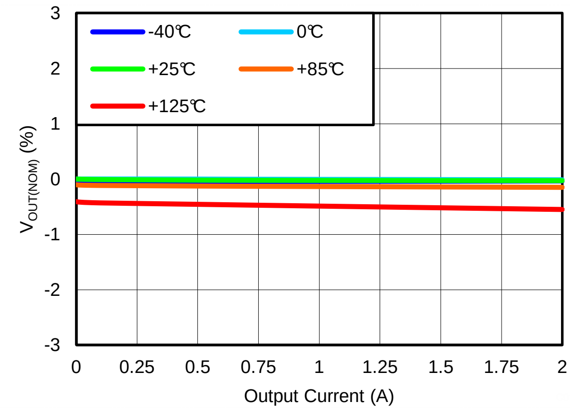
$V_{OUT(TARGET)}$ = 0.8 V, I_{OUT} = 5 mA, V_{BIAS} = Open

Figure 8. Minimum Adjustable V_{OUT}, No BIAS Line Regulation



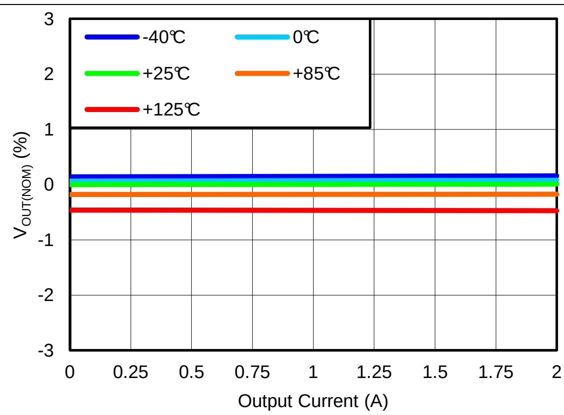
$V_{OUT(TARGET)}$ = 5 V, I_{OUT} = 5 mA, V_{BIAS} = Open

Figure 9. Maximum Adjustable V_{OUT}, No BIAS Line Regulation



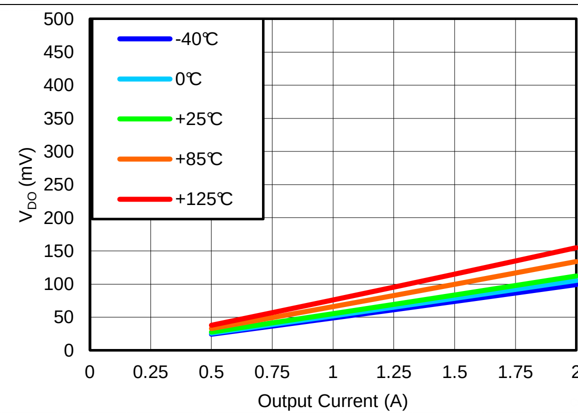
$V_{OUT(TARGET)}$ = 0.8 V, V_{IN} = 1.4 V, V_{BIAS} = Open

Figure 10. Minimum Adjustable V_{OUT}, Minimum V_{IN}, No BIAS Load Regulation



$V_{OUT(TARGET)}$ = 5 V, V_{IN} = 5.3 V, V_{BIAS} = Open

Figure 11. Maximum Adjustable V_{OUT} Load Regulation

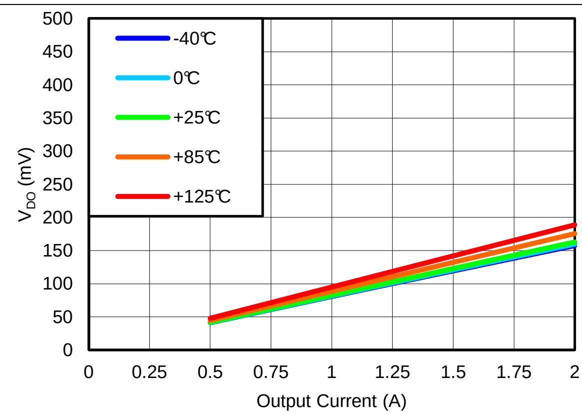


V_{IN} = 1.4 V, ANY-OUT, V_{BIAS} = Open, No BIAS

Figure 12. Minimum V_{IN} Dropout Voltage vs Output Current

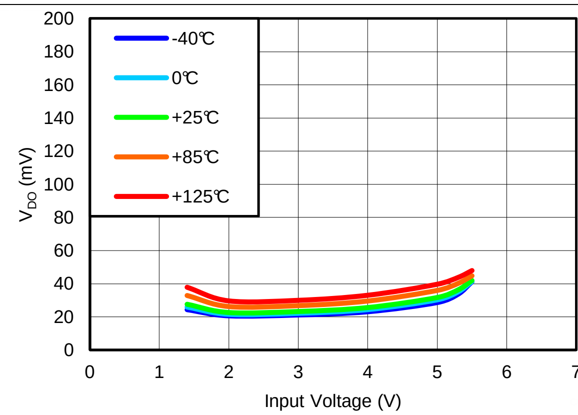
Typical Characteristics (continued)

At T_J = 25°C, {1.1 V ≤ V_{IN} < 1.4 V and 3.0 V ≤ V_{BIAS} ≤ 6.5 V} or {V_{IN} ≥ 1.4 V and V_{BIAS} open} [(1)], V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.3 V, $V_{OUT(TARGET)}$ = 0.8 V, OUT connected to 50 Ω to GND, V_{EN} = 1.1 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 10 nF, and PG pin pulled up to V_{IN} with 100 kΩ, unless otherwise noted.



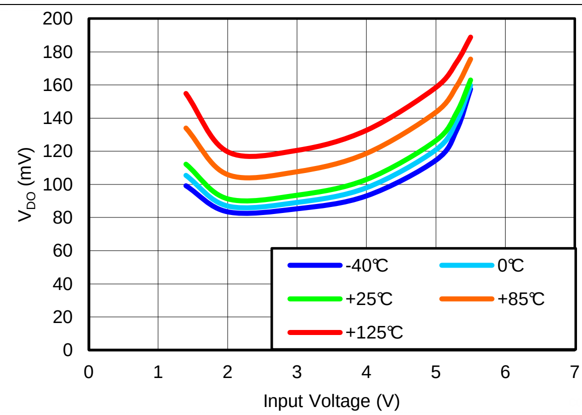
V_{IN} = 5.5 V, ANY-OUT, V_{BIAS} = Open,

Figure 13. Dropout Voltage vs Output Current



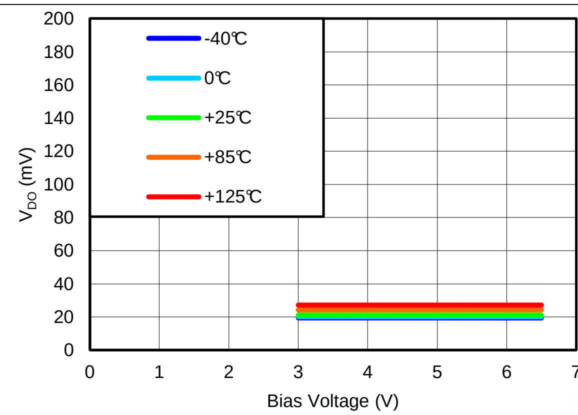
V_{BIAS} = Open, I_{OUT} = 0.5 A, ANY-OUT

Figure 14. Dropout Voltage vs Input Voltage



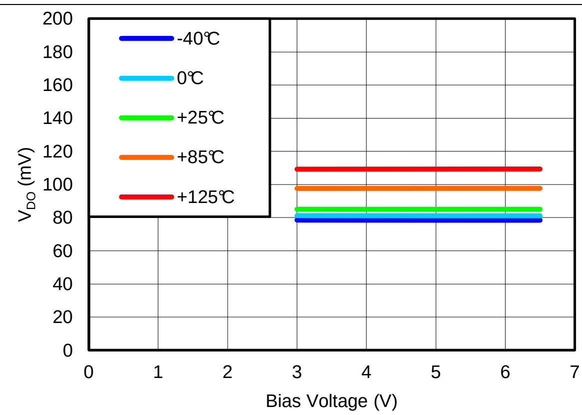
V_{BIAS} = Open, I_{OUT} = 2 A, ANY-OUT

Figure 15. Dropout Voltage vs Input Voltage



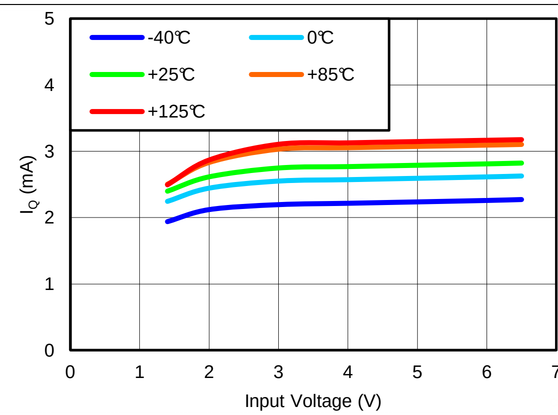
V_{IN} = 1.1 V, ANY-OUT, I_{OUT} = 0.5 A

Figure 16. Dropout Voltage vs Bias Voltage



V_{IN} = 1.1 V, ANY-OUT, I_{OUT} = 2 A

Figure 17. Minimum V_{IN} Dropout Voltage vs Bias Voltage

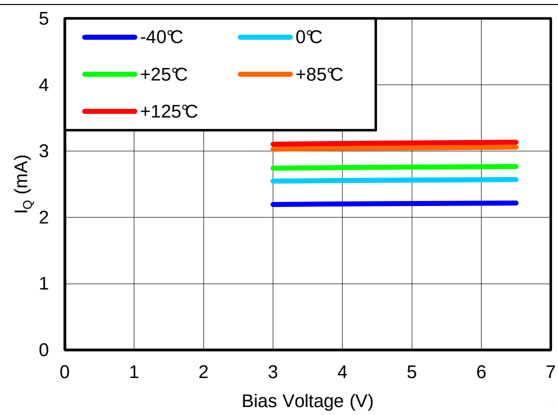


$V_{OUT(TARGET)}$ = 0.8 V, I_{OUT} = 5 mA, V_{BIAS} = Open

Figure 18. Minimum ANY-OUT V_{OUT}, No BIAS Quiescent Current vs Input Voltage

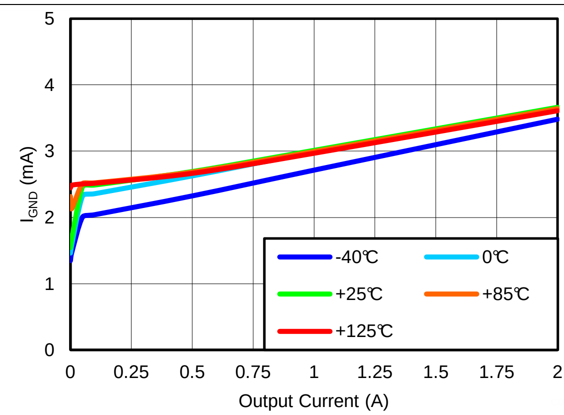
Typical Characteristics (continued)

At T_J = 25°C, {1.1 V ≤ V_{IN} < 1.4 V and 3.0 V ≤ V_{BIAS} ≤ 6.5 V} or {V_{IN} ≥ 1.4 V and V_{BIAS} open} (1), V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.3 V, $V_{OUT(TARGET)}$ = 0.8 V, OUT connected to 50 Ω to GND, V_{EN} = 1.1 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 10 nF, and PG pin pulled up to V_{IN} with 100 kΩ, unless otherwise noted.



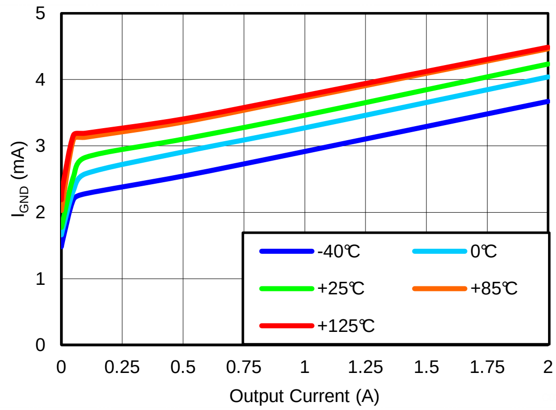
$V_{OUT(TARGET)}$ = 0.8 V, I_{OUT} = 5 mA, V_{IN} = 1.1 V

Figure 19. Minimum ANY-OUT V_{OUT}, Minimum V_{IN} Quiescent Current vs Bias Voltage



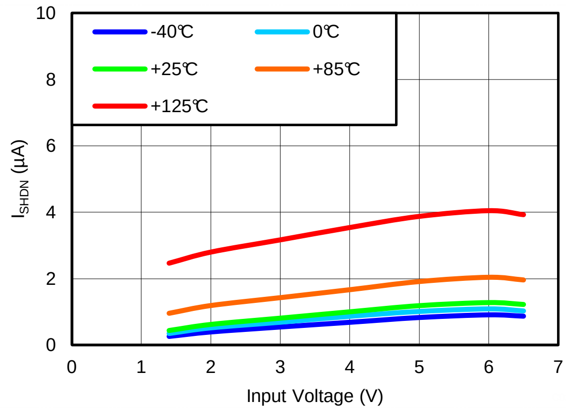
$V_{OUT(TARGET)}$ = 0.8 V, V_{IN} = 1.4 V, V_{BIAS} = Open

Figure 20. Minimum ANY-OUT V_{OUT}, Minimum V_{IN}, No BIAS Quiescent Current vs Output Current



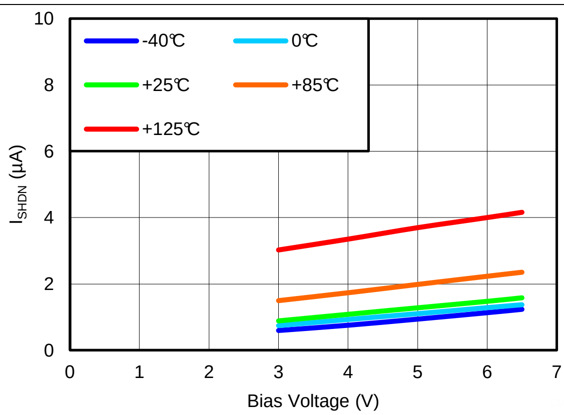
$V_{OUT(TARGET)}$ = 0.8 V, V_{IN} = 1.1 V, V_{BIAS} = 3 V

Figure 21. Minimum ANY-OUT V_{OUT}, V_{IN}, and BIAS Quiescent Current vs Output Current



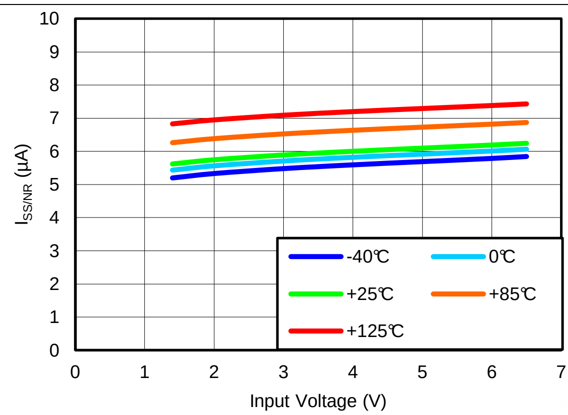
$V_{OUT(TARGET)}$ = 0.8 V, V_{BIAS} = Open

Figure 22. Minimum ANY-OUT V_{OUT}, No BIAS Shutdown Current vs Input Voltage



$V_{OUT(TARGET)}$ = 0.8 V, V_{IN} = 1.1 V

Figure 23. Minimum ANY-OUT V_{OUT}, Minimum V_{IN} Shutdown Current vs Bias Voltage

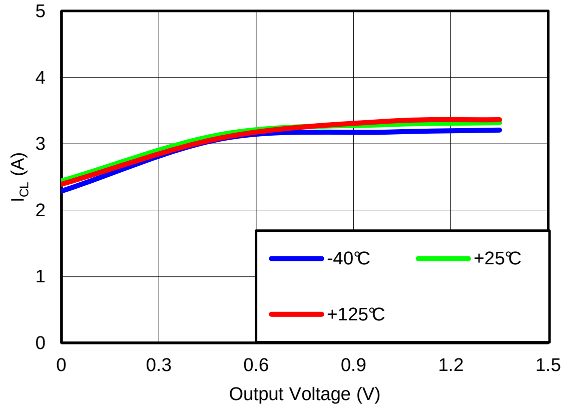


$V_{OUT(TARGET)}$ = 0.8 V, V_{BIAS} = Open

Figure 24. Minimum ANY-OUT V_{OUT}, No BIAS Soft-Start Current vs Input Voltage

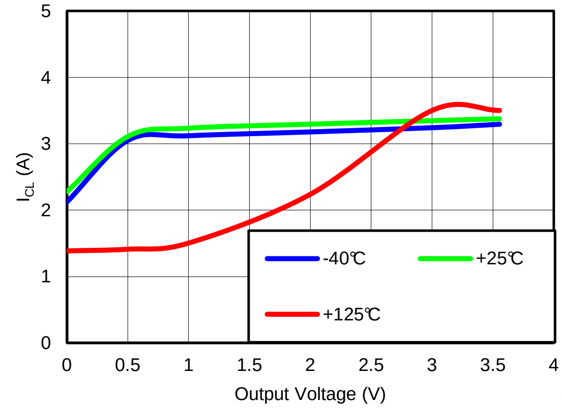
Typical Characteristics (continued)

At T_J = 25°C, {1.1 V ≤ V_{IN} < 1.4 V and 3.0 V ≤ V_{BIAS} ≤ 6.5 V} or {V_{IN} ≥ 1.4 V and V_{BIAS} open} [(1)], V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.3 V, $V_{OUT(TARGET)}$ = 0.8 V, OUT connected to 50 Ω to GND, V_{EN} = 1.1 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 10 nF, and PG pin pulled up to V_{IN} with 100 kΩ, unless otherwise noted.



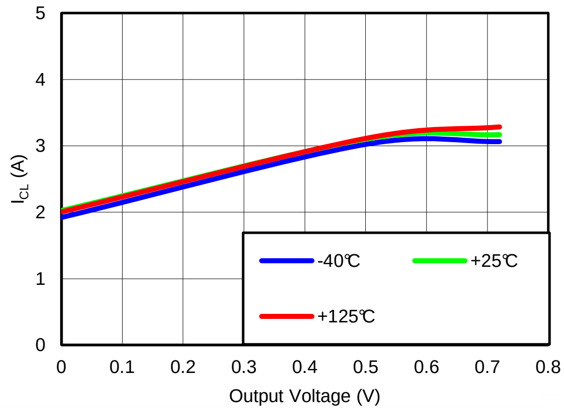
V_{IN} = 1.8 V, ANY-OUT, V_{BIAS} = Open, $V_{OUT(TARGET)}$ = 1.5 V

Figure 25. Current Limit vs Output Voltage



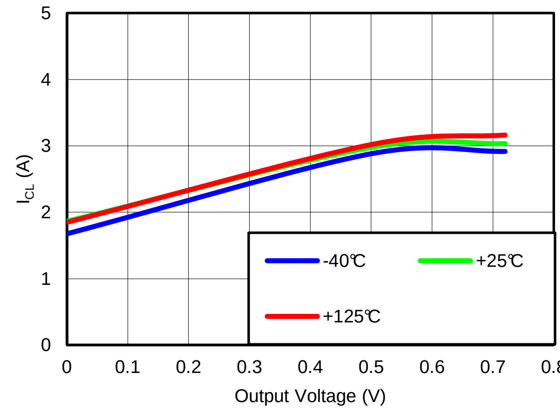
$V_{OUT(TARGET)}$ = 3.95 V, V_{IN} = 4.25 V, V_{BIAS} = Open

Figure 26. Maximum ANY-OUT V_{OUT} Current Limit vs Output Voltage



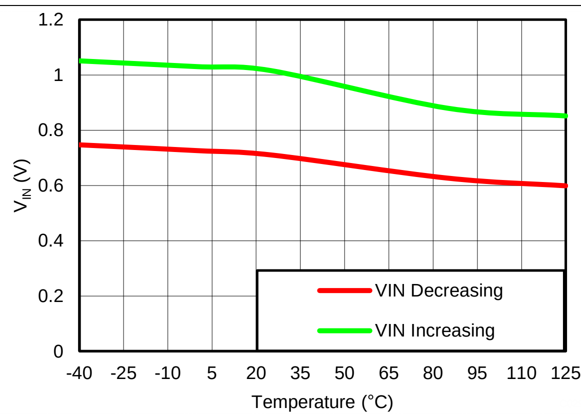
$V_{OUT(TARGET)}$ = 0.8 V, V_{IN} = 1.1 V, V_{BIAS} = 3 V

Figure 27. Minimum ANY-OUT V_{OUT}, V_{IN}, and BIAS Current Limit vs Output Voltage



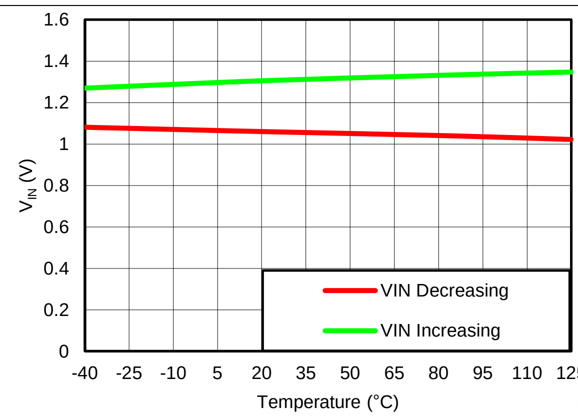
$V_{OUT(TARGET)}$ = 0.8 V, V_{IN} = 1.1 V, V_{BIAS} = 6.5 V

Figure 28. Minimum ANY-OUT V_{OUT}, Minimum V_{IN}, Maximum BIAS Current Limit vs Output Voltage



$V_{OUT(TARGET)}$ = 0.8 V, V_{BIAS} = 3.0 V

Figure 29. Minimum ANY-OUT V_{OUT}, Minimum BIAS Input UVLO Threshold vs Temperature

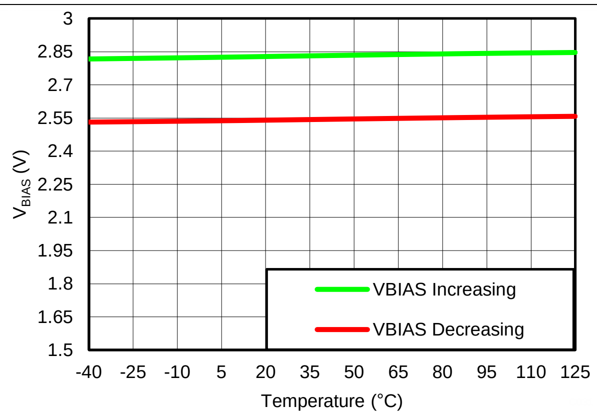


$V_{OUT(TARGET)}$ = 0.8 V, V_{BIAS} = Open

Figure 30. Minimum ANY-OUT V_{OUT}, No BIAS Input UVLO Threshold vs Temperature

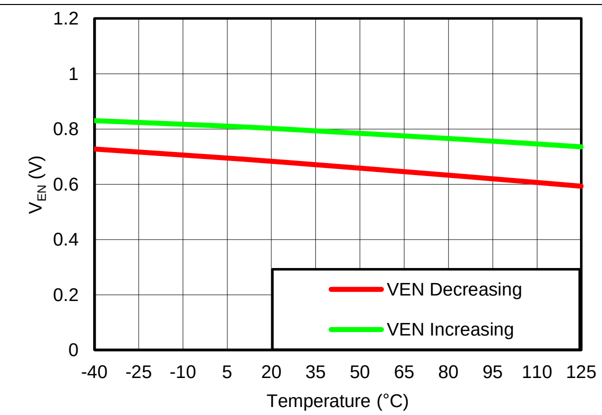
Typical Characteristics (continued)

At T_J = 25°C, {1.1 V ≤ V_{IN} < 1.4 V and 3.0 V ≤ V_{BIAS} ≤ 6.5 V} or {V_{IN} ≥ 1.4 V and V_{BIAS} open} [(1)], V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.3 V, $V_{OUT(TARGET)}$ = 0.8 V, OUT connected to 50 Ω to GND, V_{EN} = 1.1 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 10 nF, and PG pin pulled up to V_{IN} with 100 kΩ, unless otherwise noted.



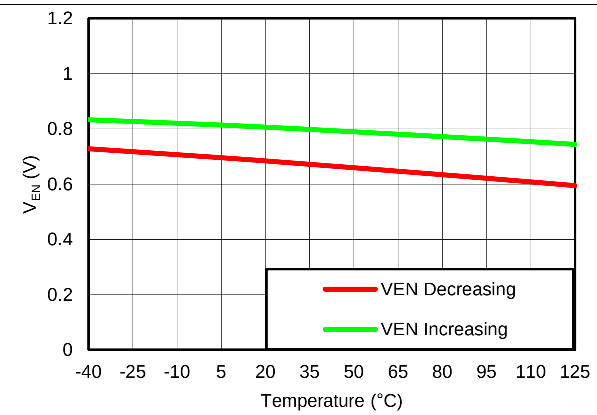
$V_{OUT(TARGET)}$ = 0.8 V, V_{IN} = 1.1 V

Figure 31. Minimum ANY-OUT V_{OUT}, Minimum V_{IN} BIAS UVLO Threshold vs Temperature



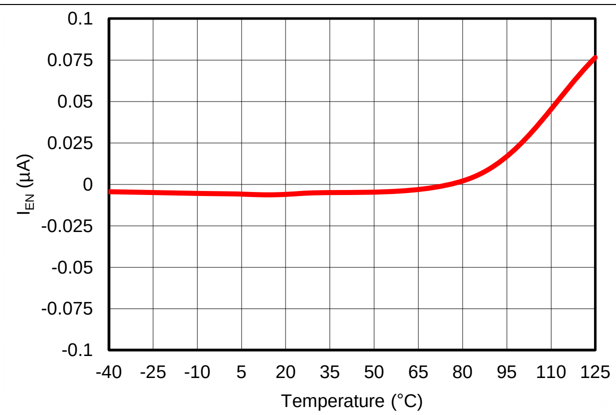
$V_{OUT(TARGET)}$ = 0.8 V, V_{IN} = 1.4 V, V_{BIAS} = Open

Figure 32. Minimum ANY-OUT V_{OUT}, Minimum V_{IN}, No BIAS Enable Threshold vs Temperature



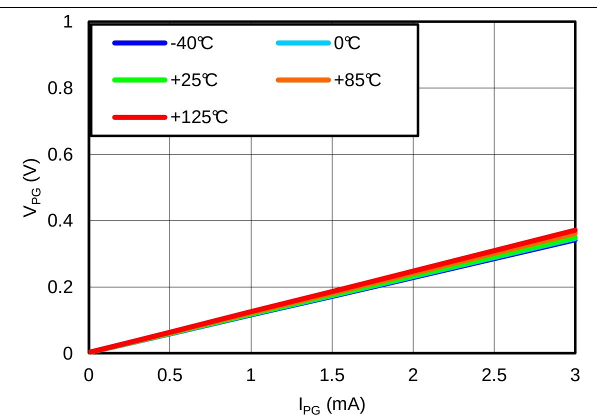
$V_{OUT(TARGET)}$ = 0.8 V, V_{IN} = 6.5 V, V_{BIAS} = Open

Figure 33. Minimum ANY-OUT V_{OUT}, Maximum V_{IN} Enable Threshold vs Temperature



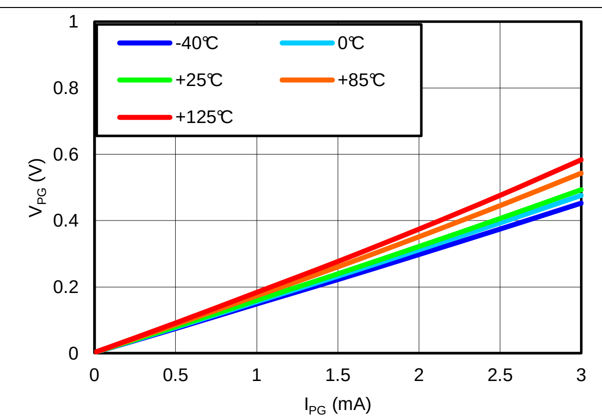
$V_{OUT(TARGET)}$ = 0.8 V, V_{IN} = V_{EN} = 6.5 V, V_{BIAS} = Open

Figure 34. Minimum ANY-OUT V_{OUT}, Maximum V_{IN} Enable Current vs Temperature



V_{IN} = 6.5 V, $V_{OUT(TARGET)}$ = 0.8 V, V_{BIAS} = Open

Figure 35. Minimum ANY-OUT V_{OUT}, Maximum V_{IN}, No BIAS PG Low Voltage vs PG Current

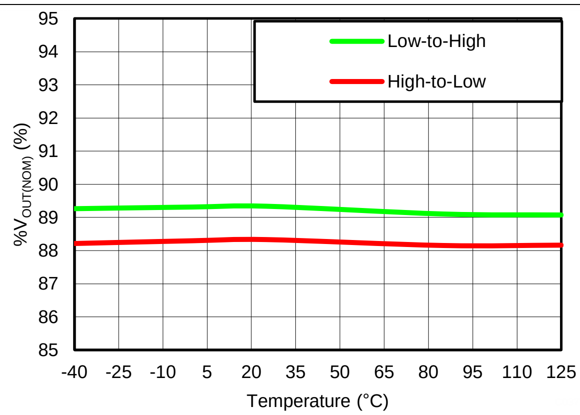


$V_{OUT(TARGET)}$ = 0.8 V, V_{IN} = 1.4 V, V_{BIAS} = Open

Figure 36. Minimum ANY-OUT V_{OUT}, Minimum V_{IN}, No BIAS PG Low Voltage vs PG Current

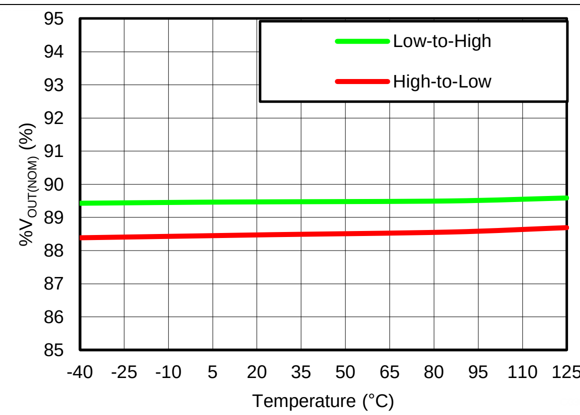
Typical Characteristics (continued)

At T_J = 25°C, {1.1 V ≤ V_{IN} < 1.4 V and 3.0 V ≤ V_{BIAS} ≤ 6.5 V} or {V_{IN} ≥ 1.4 V and V_{BIAS} open} [(1)], V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.3 V, $V_{OUT(TARGET)}$ = 0.8 V, OUT connected to 50 Ω to GND, V_{EN} = 1.1 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 10 nF, and PG pin pulled up to V_{IN} with 100 kΩ, unless otherwise noted.



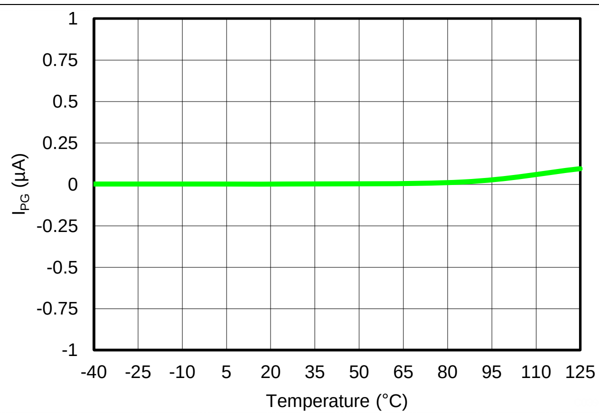
$V_{OUT(TARGET)}$ = 0.8 V, V_{IN} = 6.5 V, V_{BIAS} = Open

Figure 37. Minimum ANY-OUT V_{OUT}, Maximum V_{IN} PG Threshold vs Temperature



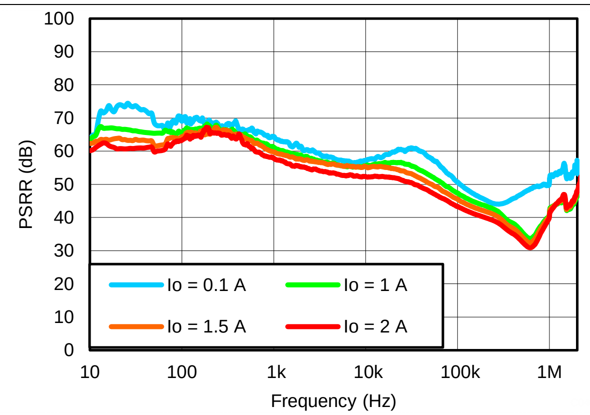
$V_{OUT(TARGET)}$ = 0.8 V, V_{IN} = 1.4 V, V_{BIAS} = Open

Figure 38. Minimum ANY-OUT V_{OUT}, Maximum V_{IN}, No BIAS PG Threshold vs Temperature



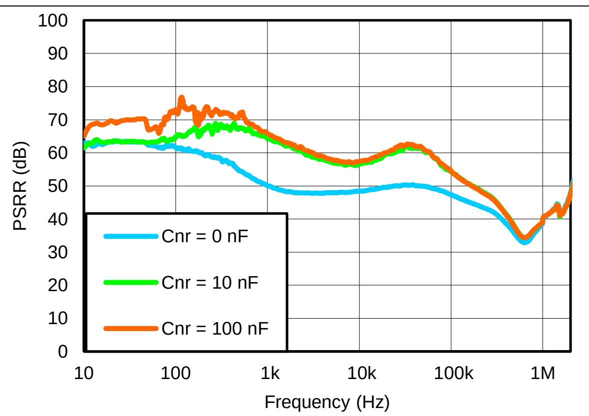
$V_{OUT(TARGET)}$ = 0.8 V, V_{IN} = V_{PG} = 6.5 V, V_{BIAS} = Open

Figure 39. Minimum ANY-OUT V_{OUT}, Maximum V_{IN} PG Current vs Temperature



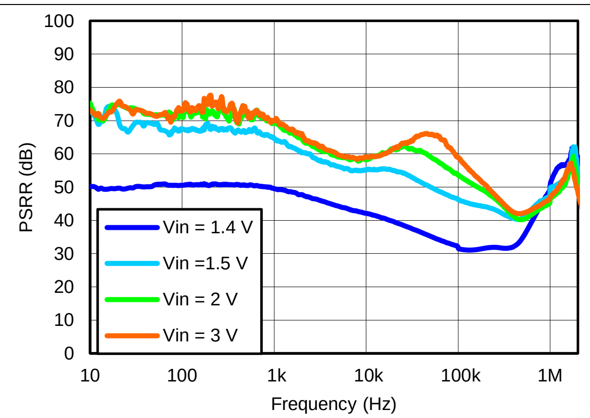
$V_{OUT(TARGET)}$ = 3.3 V, ANY-OUT, V_{IN} = V_{EN} = 3.8 V, V_{BIAS} = Open, C_{OUT} = 22 µF, $C_{NR/SS}$ = C_{FF} = 10 nF

Figure 40. Power-Supply Rejection vs Output Current



$V_{OUT(TARGET)}$ = 3.3 V, ANY-OUT, V_{IN} = V_{EN} = 3.8 V, V_{BIAS} = Open, I_{OUT} = 1.5 A, C_{OUT} = 22 µF, C_{FF} = 10 nF

Figure 41. Power-Supply Rejection vs $C_{NR/SS}$

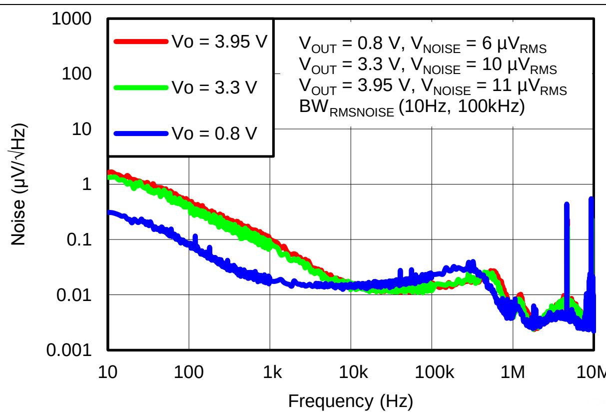


$V_{OUT(TARGET)}$ = 1.2 V, ANY-OUT, V_{BIAS} = Open, I_{OUT} = 1.5 A, C_{OUT} = 22 µF, $C_{NR/SS}$ = C_{FF} = 10 nF

Figure 42. Power-Supply Rejection vs Input Voltage

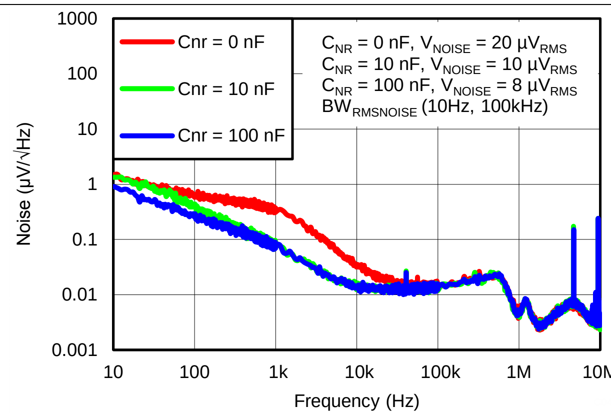
Typical Characteristics (continued)

At T_J = 25°C, {1.1 V ≤ V_{IN} < 1.4 V and 3.0 V ≤ V_{BIAS} ≤ 6.5 V} or {V_{IN} ≥ 1.4 V and V_{BIAS} open} (1), V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.3 V, $V_{OUT(TARGET)}$ = 0.8 V, OUT connected to 50 Ω to GND, V_{EN} = 1.1 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 10 nF, and PG pin pulled up to V_{IN} with 100 kΩ, unless otherwise noted.



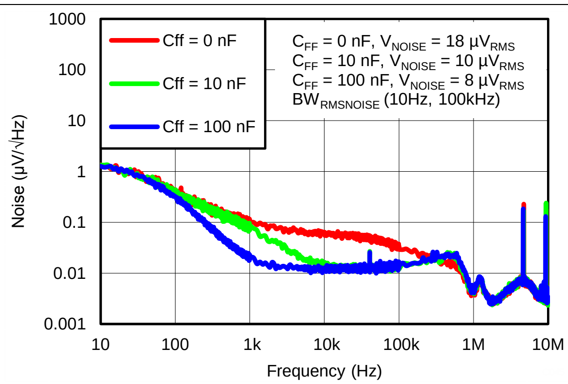
V_{IN} = $V_{OUT(TARGET)}$ + 0.5 V, ANY-OUT, V_{BIAS} = Open, I_{OUT} = 1.5 A, C_{OUT} = 22 µF, $C_{NR/SS}$ = C_{FF} = 10 nF

Figure 43. Spectral Noise Density vs Output Voltage



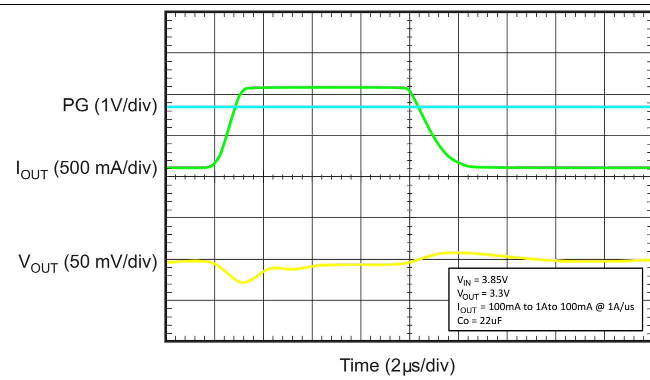
V_{IN} = 3.8 V, $V_{OUT(TARGET)}$ = 3.3 V, ANY-OUT, V_{BIAS} = Open, I_{OUT} = 1.5 A, C_{OUT} = 22 µF, C_{FF} = 10 nF

Figure 44. Spectral Noise Density vs $C_{NR/SS}$



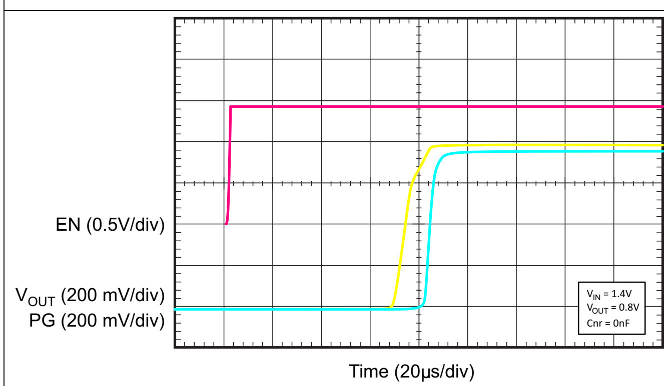
V_{IN} = 3.8 V, $V_{OUT(TARGET)}$ = 3.3 V, ANY-OUT, V_{BIAS} = Open, I_{OUT} = 1.5 A, C_{OUT} = 22 µF, $C_{NR/SS}$ = 10 nF

Figure 45. Spectral Noise Density vs C_{FF}



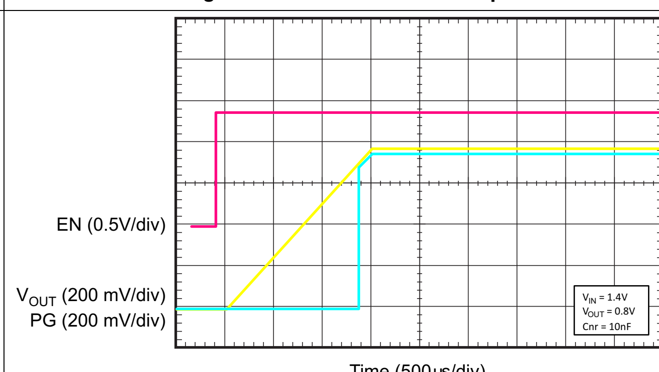
V_{IN} = 3.85 V, V_{OUT} = 3.3 V, I_{OUT} = 100 mA to 1 A to 100 mA at 1 A/µs, C_O = 22 µF

Figure 46. Load Transient Response



V_{IN} = 1.4 V, V_{OUT} = 0.8 V, $C_{NR/SS}$ = 0 nF

Figure 47. Start-Up ($C_{NR/SS}$ = 0 nF)

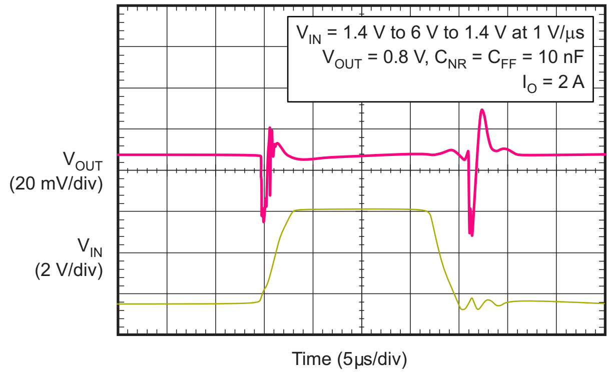


V_{IN} = 1.4 V, V_{OUT} = 0.8 V, $C_{NR/SS}$ = 10 nF

Figure 48. Start-Up

Typical Characteristics (continued)

At T_J = 25°C, {1.1 V ≤ V_{IN} < 1.4 V and 3.0 V ≤ V_{BIAS} ≤ 6.5 V} or {V_{IN} ≥ 1.4 V and V_{BIAS} open} (1), V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.3 V, $V_{OUT(TARGET)}$ = 0.8 V, OUT connected to 50 Ω to GND, V_{EN} = 1.1 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 10 nF, and PG pin pulled up to V_{IN} with 100 kΩ, unless otherwise noted.



V_{IN} = 1.4 V to 6 V to 1.4 V at 1 V/µs,
V_{OUT} = 0.8 V, I_{OUT} = 2 A, $C_{NR/SS}$ = C_{FF} = 10 nF

Figure 49. Line Transient

7 Detailed Description

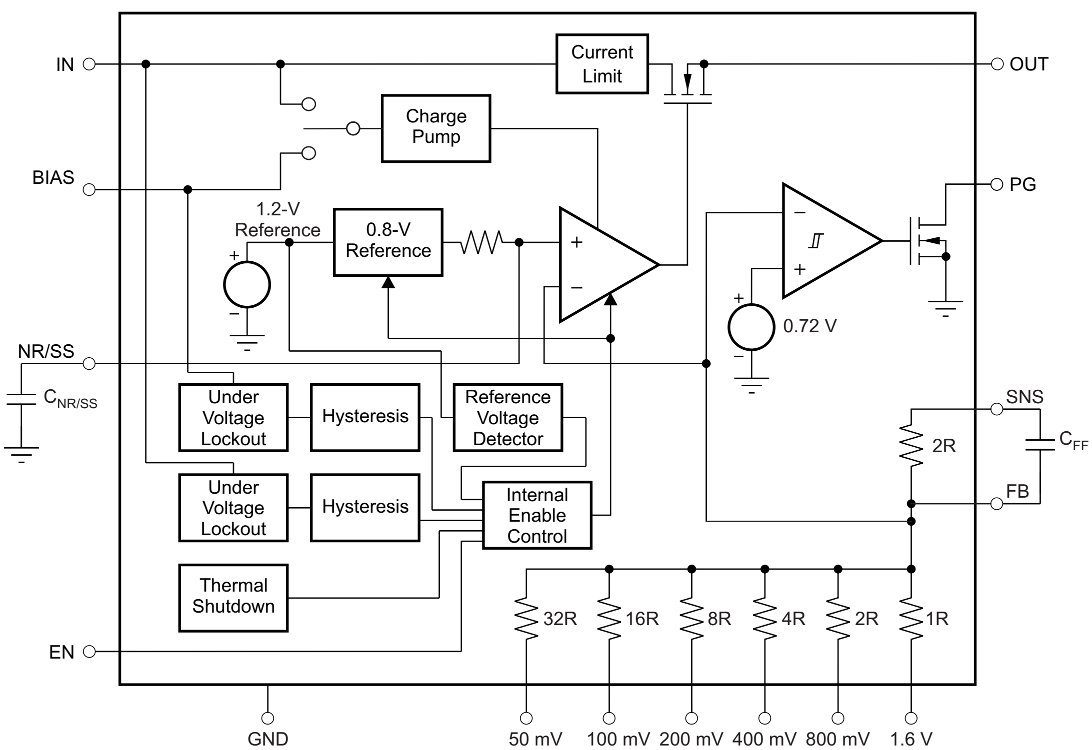
7.1 Overview

The TPS7A8300 is a low-noise, high PSRR, low-dropout regulator capable of sourcing a 2-A load with only 125 mV of maximum dropout. The TPS7A8300 can operate down to 1.1-V input voltage and 0.8-V output voltage. This combination of low noise, high PSRR, and low output voltage makes the device an ideal low dropout (LDO) regulator to power a multitude of loads from noise-sensitive communication components in high-speed communication applications to high-end microprocessors or field-programmable gate arrays (FPGAs).

The TPS7A8300 block diagram contains several features, including:

- A 2-A, low-dropout regulator with an internal charge pump,
- Low-noise, 0.8-V reference,
- Internal protection circuitry, such as undervoltage lockout (UVLO), foldback current limit, and thermal shutdown,
- Programmable soft-start,
- Power-good output, and
- An integrated resistance network (ANY-OUT) with a 50-mV minimum resolution.

7.2 Functional Block Diagram



NOTE: 32R = 193.6 kΩ (that is, 1R = 6.05 kΩ).

7.3 Feature Description

7.3.1 ANY-OUT Programmable Output Voltage

The TPS7A8300 does not require external resistors to set output voltage, which is typical of adjustable low-dropout voltage regulators (LDOs). However, the TPS7A8300 uses pins 5, 6, 7, 9, 10, and 11 to program the regulated output voltage. Each pin is either connected to ground (active) or left open (floating). ANY-OUT programming is set by Equation 1 as the sum of the internal reference voltage (V_{REF} = 0.8 V) plus the accumulated sum of the respective voltages assigned to each active pin; that is, 50mV (pin 5), 100mV (pin 6), 200mV (pin 7), 400mV (pin 9), 800mV (pin 10), or 1.6V (pin 11). Table 1 summarizes these voltage values associated with each active pin setting for reference. By leaving all program pins open, or floating, the output is thereby programmed to the minimum possible output voltage equal to V_{REF}.

$$V_{OUT} = V_{REF} + (\Sigma \text{ ANY-OUT Pins to Ground}) \quad (1)$$

Table 1. ANY-OUT Programmable Output Voltage

ANY-OUT PROGRAM PINS (Active Low)	ADDITIVE OUTPUT VOLTAGE LEVEL
Pin 5 (50mV)	50 mV
Pin 6 (100mV)	100 mV
Pin 7 (200mV)	200 mV
Pin 9 (400mV)	400 mV
Pin 10 (800mV)	800 mV
Pin 11 (1.6V)	1.6 V

Table 2 provides a full list of target output voltages and corresponding pin settings. The voltage setting pins have a binary weight; therefore, the output voltage can be programmed to any value from 0.8 V to 3.95 V in 50-mV steps.

There are several alternative ways to set the output voltage. The program pins can be driven using external general-purpose input/output pins (GPIOs), manually connected to ground using 0-Ω resistors (or left open), or hardwired by the given layout of the printed circuit board (PCB) to set the ANY-OUT voltage.

NOTE

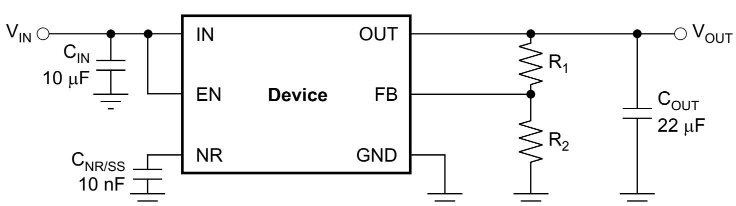
For output voltages greater than 3.95 V, use a traditional adjustable configuration (see the *Adjustable Operation* section).

Table 2. User-Configurable Output Voltage Settings

$V_{OUT(TARGET)}$ (V)	50mV	100mV	200mV	400mV	800mV	1.6V	$V_{OUT(TARGET)}$ (V)	50mV	100mV	200mV	400mV	800mV	1.6V
0.80	Open	Open	Open	Open	Open	Open	2.40	Open	Open	Open	Open	Open	GND
0.85	GND	Open	Open	Open	Open	Open	2.45	GND	Open	Open	Open	Open	GND
0.90	Open	GND	Open	Open	Open	Open	2.50	Open	GND	Open	Open	Open	GND
0.95	GND	GND	Open	Open	Open	Open	2.55	GND	GND	Open	Open	Open	GND
1.00	Open	Open	GND	Open	Open	Open	2.60	Open	Open	GND	Open	Open	GND
1.05	GND	Open	GND	Open	Open	Open	2.65	GND	Open	GND	Open	Open	GND
1.10	Open	GND	GND	Open	Open	Open	2.70	Open	GND	GND	Open	Open	GND
1.15	GND	GND	GND	Open	Open	Open	2.75	GND	GND	GND	Open	Open	GND
1.20	Open	Open	Open	GND	Open	Open	2.80	Open	Open	Open	GND	Open	GND
1.25	GND	Open	Open	GND	Open	Open	2.85	GND	Open	Open	GND	Open	GND
1.30	Open	GND	Open	GND	Open	Open	2.90	Open	GND	Open	GND	Open	GND
1.35	GND	GND	Open	GND	Open	Open	2.95	GND	GND	Open	GND	Open	GND
1.40	Open	Open	GND	GND	Open	Open	3.00	Open	Open	GND	GND	Open	GND
1.45	GND	Open	GND	GND	Open	Open	3.05	GND	Open	GND	GND	Open	GND
1.50	Open	GND	GND	GND	Open	Open	3.10	Open	GND	GND	GND	Open	GND
1.55	GND	GND	GND	GND	Open	Open	3.15	GND	GND	GND	GND	Open	GND
1.60	Open	Open	Open	Open	GND	Open	3.20	Open	Open	Open	Open	GND	GND
1.65	GND	Open	Open	Open	GND	Open	3.25	GND	Open	Open	Open	GND	GND
1.70	Open	GND	Open	Open	GND	Open	3.30	Open	GND	Open	Open	GND	GND
1.75	GND	GND	Open	Open	GND	Open	3.35	GND	GND	Open	Open	GND	GND
1.80	Open	Open	GND	Open	GND	Open	3.40	Open	Open	GND	Open	GND	GND
1.85	GND	Open	GND	Open	GND	Open	3.45	GND	Open	GND	Open	GND	GND
1.90	Open	GND	GND	Open	GND	Open	3.50	Open	GND	GND	Open	GND	GND
1.95	GND	GND	GND	Open	GND	Open	3.55	GND	GND	GND	Open	GND	GND
2.00	Open	Open	Open	GND	GND	Open	3.60	Open	Open	Open	GND	GND	GND
2.05	GND	Open	Open	GND	GND	Open	3.65	GND	Open	Open	GND	GND	GND
2.10	Open	GND	Open	GND	GND	Open	3.70	Open	GND	Open	GND	GND	GND
2.15	GND	GND	Open	GND	GND	Open	3.75	GND	GND	Open	GND	GND	GND
2.20	Open	Open	GND	GND	GND	Open	3.80	Open	Open	GND	GND	GND	GND
2.25	GND	Open	GND	GND	GND	Open	3.85	GND	Open	GND	GND	GND	GND
2.30	Open	GND	GND	GND	GND	Open	3.90	Open	GND	GND	GND	GND	GND
2.35	GND	GND	GND	GND	GND	Open	3.95	GND	GND	GND	GND	GND	GND

7.3.2 Adjustable Operation

The TPS7A8300 can be used either with the internal ANY-OUT network or using external resistors. Using the ANY-OUT network allows the TPS7A8300 to be programmed from 0.8 V to 3.95 V. To extend this range of output voltage operation to 5.0 V, external resistors must be used. This configuration is referred to as the adjustable configuration of the TPS7A8300 throughout this document. Regardless whether the internal resistor network or whether external resistors are used, the nominal output voltage of the device is set by two resistors, as shown in Figure 50. Using an internal resistor ensures a 1% matching and minimizes both the number of external components and layout footprint.



Where: $\frac{V_{OUT}}{R_1 + R_2} \geq 5\ \mu A$, and

$$R_1 = R_2\left(\frac{V_{OUT}}{V_{REF}} - 1\right)$$

Figure 50. Adjustable Operation for Maximum AC Performance

R_1 and R_2 can be calculated for any output voltage range using Equation 2. This resistive network must provide a current equal to or greater than 5 µA for optimum noise performance.

$$R_1 = R_2\left(\frac{V_{OUT}}{V_{REF}} - 1\right), \quad \text{where } \frac{|V_{REF(max)}|}{R_2} > 5\ \mu A \tag{2}$$

If greater voltage accuracy is required, take into account the output voltage offset contributions resulting from the feedback pin current (I_{FB}) and use 0.1% tolerance resistors.

Table 3 shows the resistor combination required to achieve a few of the most common rails using commercially-available, 0.1%-tolerance resistors to maximize nominal voltage accuracy while abiding to the formula shown in Equation 2.

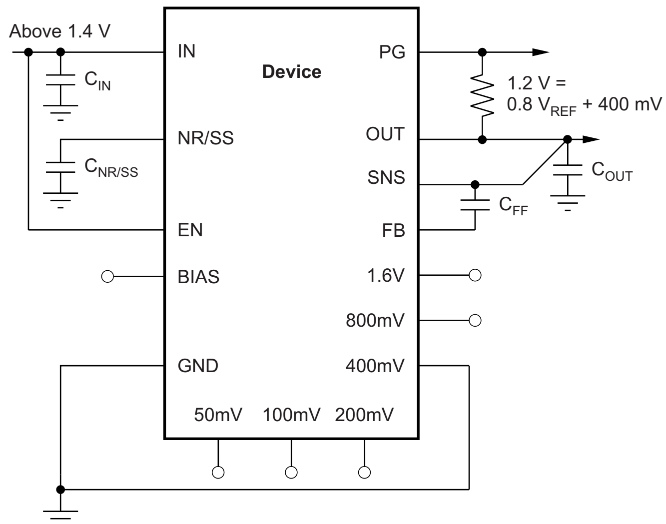
Table 3. Recommended Feedback-Resistor Values

$V_{OUT(TARGET)}$ (V)	FEEDBACK RESISTOR VALUES (1)	
	R_1 (kΩ)	R_2 (kΩ)
1.00	2.55	10.2
1.20	5.9	11.8
1.50	9.31	10.7
1.80	18.7	15
1.90	15.8	11.5
2.50	24.3	11.5
3.00	31.6	11.5
3.30	35.7	11.5
5.00	105	20

(1) R_1 is connected from OUT to FB; R_2 is connected from FB to GND.

7.3.3 ANY-OUT Operation

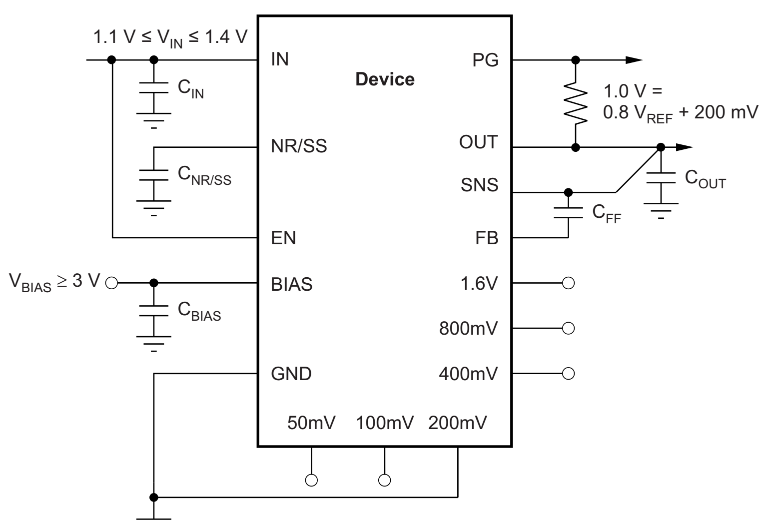
Considering the use of the ANY-OUT internal network (where the unit resistance of 1R is equal to 6.05 kΩ) the output voltage is set by grounding the appropriate control pins, as shown in Figure 51. When grounded, all control pins add a specific voltage on top of the internal reference voltage (V_{REF} = 0.8 V). The output voltage can be equated with Equation 4. Figure 51 and Figure 52 show a 1.2-V and 1-V output voltage, respectively, that provide an example of the circuit usage with and without BIAS voltage. These schematics are described in more detail in the *Typical Application* section.



Typical Application
V_{IN} ≥ 1.4 V

Figure 51. ANY-OUT Configuration Circuit (1.4-V Input, 1.2-V Output, No External BIAS)

$$V_{OUT(NOM)} = V_{REF} + 0.4\ V = 0.8\ V + 0.4\ V = 1.2\ V \quad (3)$$



Typical Application
1.1 V ≤ V_{IN} < 1.4 V

Figure 52. ANY-OUT Configuration Circuit (1.1-V Input, 1.0-V Output, 3-V BIAS Voltage)

$$V_{OUT(NOM)} = V_{REF} + 0.2\ V = 0.8\ V + 0.2\ V = 1.0\ V \quad (4)$$

7.3.4 2-A LDO with an Internal Charge Pump

The TPS7A8300 can be used either with the internal resistor network provided, or with the external component as a traditional adjustable LDO. Regardless of the implementation, the TPS7A8300 provides excellent regulation to 1% accuracy, excellent dropout voltage, and high output current capability.

If the input voltage is below 1.4 V, an external BIAS voltage must be supplied to maintain the dropout characteristics. The input voltage or the BIAS voltage is fed through to a internal charge pump to power the internal error amplifier providing the regulation.

7.3.4.1 Dropout Voltage (V_{DO})

Generally speaking, the dropout voltage often refers to the voltage difference between the input and output voltage ($V_{DO} = V_{IN} – V_{OUT}$). However, in the , V_{DO} is defined as the $V_{IN} – V_{OUT}$ voltage at the rated current (I_{RATED}), where the main current pass-FET is fully on in the ohmic region of operation and is characterized by the classic $R_{DS(ON)}$ of the FET. V_{DO} indirectly specifies a minimum input voltage above the nominal programmed output voltage at which the output voltage is expected to remain within its accuracy boundary. If the input falls below this V_{DO} limit ($V_{IN} < V_{OUT} + V_{DO}$), then the output voltage decreases in order to follow the input voltage.

Dropout voltage is always determined by the $R_{DS(ON)}$ of the main pass-FET. Therefore, if the LDO operates below the rated current, then the V_{DO} for that current scales accordingly. The $R_{DS(ON)}$ for the TPS7A8300 can be calculated using Equation 5:

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (5)$$

7.3.4.2 Output Voltage Accuracy

Output voltage accuracy specifies minimum and maximum output voltage error, relative to the expected nominal output voltage stated as a percent. This accuracy error includes the errors introduced by the internal reference and the load and line regulation across the full range of rated load and line operating conditions over temperature, unless otherwise specified by the Electrical Characteristics. Output voltage accuracy also accounts for all variations between manufacturing lots.

7.3.4.3 Internal Charge Pump

The internal charge pump ensures proper operation without requiring an external BIAS voltage down to +1.4-V input voltage. Below a 1.4-V input voltage, a BIAS input voltage between 3.0 V and 6.5 V is required. Dropout plots in the ohmic region of the pass-FET are illustrated in the *Typical Characteristics* section (Figure 12 through Figure 17).

7.3.5 Low-Noise, 0.8-V Reference

The TPS7A8300 includes a low-noise reference ensuring minimal noise during operation because the internal reference is normally the dominant term in noise analysis. Further noise reduction can be achieved using the NR/SS pin and by adding an external C_{FF} between the SNS pin and the FB pin.

7.3.6 Internal Protection Circuitry

7.3.6.1 Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit monitors the input and bias voltage (V_{IN} and V_{BIAS}, respectively) to prevent the device from turning on before V_{IN} and V_{BIAS} rise above the lockout voltage. The UVLO circuit also causes a shutdown when V_{IN} and V_{BIAS} fall below the lockout voltage.

7.3.6.2 Internal Current Limit ($I_{(LIM)}$)

The internal current limit circuit is used to protect the LDO against high-load current faults or shorting events. The LDO is not designed to operate in a steady-state current limit. During a current-limit event, the LDO sources constant current. Therefore, the output voltage falls when load impedance decreases. Note also that if a current limit occurs and the resulting output voltage is low, excessive power may be dissipated across the LDO, resulting in a thermal shutdown of the output.

A foldback feature limits the short-circuit current to protect the regulator from damage under all load conditions. If OUT is forced below 0 V before EN goes high and the load current required exceeds the foldback current limit, the device does not start up. In applications that function with both a positive and negative voltage supply, there are several ways to ensure proper start-up:

- Enable the TPS7A8300 first and disable the device last.
- Delaying the EN voltage with respect to the IN voltage allows the internal pull-down resistor to discharge any residual voltage at OUT. If a faster discharge rate is required, use an external resistor from OUT to GND.

7.3.6.3 Thermal Protection

The TPS7A8300 contains a thermal shutdown protection circuit to turn off the output current when excessive heat is dissipated in the LDO. Thermal shutdown occurs when the thermal junction temperature (T_J) of the main pass-FET exceeds 160°C (typical). Thermal shutdown hysteresis assures that the LDO resets again (turns on) when the temperature falls to 140°C (typical). The thermal time-constant of the semiconductor die is fairly short, and thus the output cycles on and off at a high rate when thermal shutdown is reached until the power dissipation is reduced.

For reliable operation, limit the junction temperature to a maximum of 125°C. To estimate the thermal margin in a given layout, increase the ambient temperature until the thermal protection shutdown is triggered using worst-case load and highest input voltage conditions. For good reliability, thermal shutdown occurs at least 45°C above the maximum expected ambient temperature condition for the application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A8300 is designed to protect against thermal overload conditions. The circuitry is not intended to replace proper heat sinking. Continuously running the TPS7A8300 into thermal shutdown degrades device reliability.

7.3.7 Programmable Soft-Start

Soft-start refers to the ramp-up characteristic of the output voltage during LDO turn-on after EN and UVLO exceed the respective threshold voltage. The noise-reduction capacitor ($C_{NR/SS}$) serves a dual purpose of both governing output noise reduction and programming the soft-start ramp during turn-on. See the *Application and Implementation* section on implementing a soft-start.

7.3.8 Power-Good Function

The TPS7A8300 has a power-good function that works by toggling the state of the PG output pin. When the output voltage falls below the PG threshold voltage ($V_{IT(PG)}$), the PG pin open-drain output engages (low impedance to GND). When the output voltage exceeds the $V_{IT(PG)}$ threshold by an amount greater than $V_{HYS(PG)}$, the PG pin becomes high-impedance. By connecting a pull-up resistor to an external supply, any downstream device can receive PG as a logic signal. Make sure that the external pull-up supply voltage results in a valid logic signal for the receiving device or devices. Use a pull-up resistor from 10 kΩ to 100 kΩ for best results.

When employing the feed-forward capacitor (C_{FF}), the turn-on time-constant for the LDO is increased and the power-good output time-constant stays the same, resulting in an invalid status of the LDO. To avoid this issue and receive a valid PG output, ensure that the time-constant of both the LDO and the power-good output match. For more details, see application report, *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator*, SBVA042.

7.3.9 Integrated Resistance Network (ANY-OUT)

An internal resistance network is provided allowing the TPS7A8300 output voltage to be programmed easily between 0.8 V to 3.95 V with a 50-mV step.

7.4 Device Functional Modes

7.4.1 Operation with 1.1 V > V_{IN} > 1.4 V

The TPS7A8300 requires a bias voltage on the BIAS pin ≥ 3.0 V if the high-current input supply voltage is between 1.1 to 1.4 V. The bias voltage pin consumes 2.3 mA, nominally.

7.4.2 Operation with 1.4 V ≥ V_{IN} > 6.5 V

If the input voltage is equal to, or exceeds 1.4 V, no bias voltage is necessary. The device is automatically selected to be powered from the IN pin in this condition and the BIAS pin can be left floating.

7.4.3 Disabled

If the voltage on the EN pin is less than 0.5 V, the device is disabled and the output is high impedance. The output impedance of the LDO is then set by the gain setting resistors if a path to GND is provided between OUT and GND. Raising EN above 1.1 V (maximum) initiates the startup sequence of the device. In this state, quiescent current does not exceed 2.5 µA.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7A8300 is a linear voltage regulator operating from 1.1 V to 6.5 V on the input and regulates voltages between 0.8 V to 5.0 V with a 1% accuracy and a 2-A maximum output current. Efficiency is defined by the ratio of output voltage to input voltage because the TPS7A8300 is a linear voltage regulator. To achieve high efficiency, the dropout voltage (V_{IN} – V_{OUT}) must be as small as possible, thus requiring a very low dropout LDO. Successfully implementing an LDO in an application depends on the application requirements. If the requirements are simply input voltage and output voltage, compliance specifications (such as internal power dissipation or stability) must be verified to ensure a solid design. If timing, startup, noise, PSRR, or any other transient specification is required, the design becomes more challenging. This section discusses the implementation and behavior of the TPS7A8300 LDO.

8.1.1 Start-Up

8.1.1.1 Enable (EN) and Undervoltage Lockout (UVLO)

The TPS7A8300 only turns on when both EN and UVLO are above the respective voltage thresholds. The UVLO circuit monitors input and bias voltage (V_{IN} and V_{BIAS}, respectively) to prevent device turn-on before V_{IN} and V_{BIAS} rise above the lockout voltage. The UVLO circuit also causes a shutdown when V_{IN} and V_{BIAS} fall below lockout. The EN signal allows independent logic-level turn-on and shutdown of the LDO. If the device turn-on is required to be controlled, the device must be enabled with or after V_{IN}. Connect EN to V_{IN} if turn-on control of the output voltage is not needed.

8.1.1.2 Noise-Reduction and Soft-Start Capacitor ($C_{NR/SS}$)

The TPS7A8300 features a programmable, monotonic, voltage-controlled soft-start that is set with an external capacitor ($C_{NR/SS}$).This soft-start eliminates power-up initialization problems when powering field-programmable gate arrays (FPGAs), digital signal processors (DSPs), or other processors. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transients to the input power bus.

To achieve a linear and monotonic start-up, the TPS7A8300 error amplifier tracks the voltage ramp of the external soft-start capacitor until the voltage exceeds the internal reference. The soft-start ramp time depends on the soft-start charging current ($I_{NR/SS}$), the soft-start capacitance ($C_{NR/SS}$), and the internal reference (V_{REF}). Soft-start ramp time can be calculated with Equation 6:

$$t_{SS} = (V_{REF} \times C_{NR/SS}) / I_{NR/SS} \tag{6}$$

Note that $I_{NR/SS}$ is provided in the *Electrical Characteristics* table and has a typical value of 6.2 µA.

For low-noise applications, the noise-reduction capacitor (connected to the NR/SS pin of the LDO) forms an RC filter for filtering out noise that is ordinarily amplified by the control loop and appears on the output voltage. For low-noise applications, a 10-nF to 1-µF $C_{NR/SS}$ is recommended.

Application Information (continued)

8.1.1.3 Soft-Start and Inrush Current

Soft-start refers to the ramp-up characteristic of the output voltage during LDO turn-on after EN and UVLO achieve threshold voltage. The noise-reduction capacitor serves a dual purpose of both governing output noise reduction and programming the soft-start ramp during turn-on.

Inrush current is defined as the current into the LDO at the IN pin during start-up. Inrush current then consists primarily of the sum of load and current used to charge the output capacitor. This current is difficult to measure because the input capacitor must be removed, which is not recommended. However, this soft-start current can be estimated by Equation 7:

$$I_{OUT(t)} = \left[\frac{C_{OUT} \times dV_{OUT}(t)}{dt} \right] + \left[\frac{V_{OUT}(t)}{R_{LOAD}} \right] \quad (7)$$

where:

- $V_{OUT}(t)$ is the instantaneous output voltage of the turn-on ramp,
- $dV_{OUT}(t)$ / dt is the slope of the V_{OUT} ramp, and
- R_{LOAD} is the resistive load impedance.

8.1.2 Capacitor Recommendation

The TPS7A8300 is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input, output, and noise-reduction pin (NR, pin 13). Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and COG-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged precisely because the capacitance varies so widely. In all cases, ceramic capacitance varies a great deal with operating voltage and temperature and the design engineer must be aware of these characteristics. As a rule of thumb, ceramic capacitors are recommended to be derated by 50%. To compensate for this derating, increase capacitor value by 100%. The input and output capacitors recommended herein account for a capacitance derating of 50%.

Attention must be given to the input capacitance to minimize transient input droop during load current steps. Input capacitances of 10 µF or greater provide the desired effect and do not affect stability. Note that simply using large ceramic input capacitances can also cause unwanted ringing at the output if the input capacitor (in combination with the wire-lead inductance) creates a high-Q peaking effect during transients. For example, a 5-nH lead inductance and a 10-µF input capacitor form an LC filter with a resonance frequency of 712 kHz that is near the edge of the open-loop bandwidth. Short, well-designed interconnect traces to the up-stream supply minimize this effect without adding damping. Damping of unwanted ringing can be accomplished by using a tantalum capacitor, with a few hundred milliohms of ESR, in parallel with the ceramic input capacitor.

8.1.2.1 Input and Output Capacitor Requirements (C_{IN} and C_{OUT})

The TPS7A8300 is designed and characterized for operation with ceramic capacitors of 22 µF or greater at the output and 10 µF at the input. Locate the input and output capacitors as near as practical to the respective input and output pins.

8.1.2.2 Feed-Forward Capacitor (C_{FF})

Although a feed-forward capacitor (C_{FF}), from the FB pin to the OUT pin is not required to achieve stability, a 10-nF, feed-forward capacitor optimizes the noise and PSRR performance. A higher capacitance C_{FF} can be used; however, the startup time is longer and the power-good signal may incorrectly indicate the output voltage has settled. For a detailed description, see application report *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator*, SBVA042.

8.1.3 AC Performance

The LDO ac performance is typically understood to include power-supply rejection ratio, load step transient response, and output noise. These metrics are primarily a function of open-loop gain and bandwidth, phase margin, and reference noise.

Application Information (continued)

8.1.3.1 Power-Supply Ripple Rejection (PSRR)

PSRR is a measure of how well the LDO control loop rejects ripple noise from the input source to make the dc output voltage as noise-free as possible across the frequency spectrum (usually 10 Hz to 10 MHz). Even though PSRR is therefore a loss in noise signal amplitude (the output ripple relative to the input ripple), the PSRR reciprocal is plotted in the Electrical Characteristics as a positive number in decibels (dB) for convenience. Equation 8 gives the PSRR calculation as a function of frequency where input noise voltage [$V_{S(IN)}(f)$] and output noise voltage [$V_{S(OUT)}(f)$] are understood to be purely ac signals.

$$\text{PSRR (dB)} = 20\ \text{Log}_{10}\left[\frac{V_{S(IN)}(f)}{V_{S(OUT)}(f)}\right] \tag{8}$$

Noise that couples from the input to the internal reference voltage for the control loop is also a primary contributor to reduced PSRR magnitude and bandwidth. This reference noise is greatly filtered by the noise-reduction capacitor at the NR pin of the LDO in combination with an internal filter resistor (R_{SS}) for improved PSRR.

The LDO is often employed not only as a dc-dc regulator, but also to provide exceptionally clean power-supply voltages that exhibit ultra-low noise and ripple to power-sensitive system components. This usage is especially true for the TPS7A8300.

8.1.3.2 Load-Step Transient Response

The load-step transient response is the output voltage response by the LDO to a step change in load current, whereby output voltage regulation is maintained. The worst-case response is characterized for a load step of 10 mA to 2 A (at 1 A per microsecond) and shows a classic critically-damped response of a very stable system. The voltage response shows a small dip in the output voltage when charge is initially depleted from the output capacitor and then the output recovers when the control loop adjusts itself. The depth of charge depletion immediately after the load step is directly proportional to the amount of output capacitance. However, to some extent, recovery speed is inversely proportional to that same output capacitance. In other words, larger output capacitances act to decrease any voltage dip or peak occurring during a load step but also decrease the control-loop bandwidth, thereby slowing response.

The worst-case off-loading step characterization occurs when the current step transitions from 2 A to 0 mA. Initially, the LDO loop cannot respond fast enough to prevent a small increase in output voltage charge on the output capacitor. The LDO cannot sink charge, therefore the control loop must turn off the main pass-FET to wait for the charge to deplete.

8.1.3.3 Noise

The TPS7A8300 is designed for system applications where minimizing noise on the power-supply rail is critical to system performance. This scenario is the case for phase-locked loop (PLL)-based clocking circuits where minimum phase noise is all important, or in test and measurement systems where even small power-supply noise fluctuations can distort instantaneous measurement accuracy.

LDO noise is defined as the internally-generated intrinsic noise created by the semiconductor circuits alone. This noise is the sum of various types of noise (such as shot noise associated with current-through-pin junctions, thermal noise caused by thermal agitation of charge carriers, flicker noise, or 1/f noise that is a property of resistors and dominates at lower frequencies as a function of 1/f, burst noise, and avalanche noise).

To calculate the LDO RMS output noise, a spectrum analyzer must first measure the spectral noise across the bandwidth of choice (typically 10 Hz to 100 kHz in units of $\mu V/\sqrt{Hz}$). RMS noise is then calculated as the integrated square root of the squared spectral noise over the band, then averaged by the bandwidth.

8.1.3.4 Behavior when Transitioning from Steady Dropout into Regulation

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, right after being in a normal regulation state, but *not* during startup), the pass-FET is driven as hard as possible when the control loop is out of balance. During the normal time required for the device to regain regulation, $V_{IN} \geq V_{OUT(NOM)} + V_{DO}$, V_{OUT} overshoots if the input voltage slew rate is 0.1 V/µs or faster.

Application Information (continued)

8.1.4 Power Dissipation (P_D)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. P_D can be calculated using Equation 9:

$$P_D = (V_{OUT} - V_{IN}) \times I_{OUT} \quad (9)$$

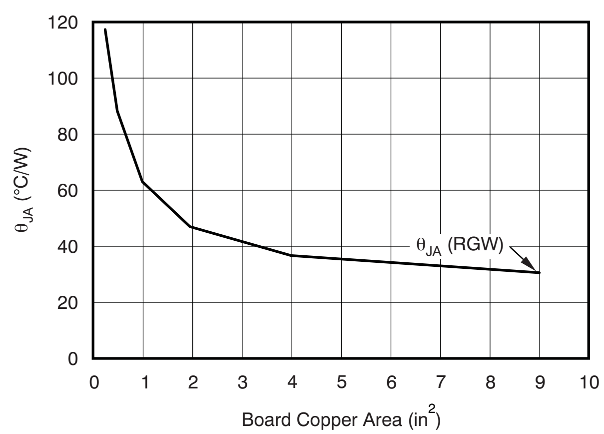
An important note is that power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input voltage necessary for output regulation to be obtained.

The primary heat conduction path for the VQFN (RGW and RGR) package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance (θ_{JA}) of the combined PCB and device package and the temperature of the ambient air (T_A), according to Equation 10.

$$T_J = T_A + (\theta_{JA} \times P_D) \quad (10)$$

Unfortunately, this thermal resistance (θ_{JA}) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The θ_{JA} recorded in the *Thermal Information* table is determined by the JEDEC standard, PCB, and copper-spreading area and is only used as a relative measure of package thermal performance. Note that for a well-designed thermal layout, θ_{JA} is actually the sum of the VQFN package junction-to-case (bottom) thermal resistance (θ_{JCbot}) plus the thermal resistance contribution by the PCB copper. When θ_{JCbot} is known, the amount of heat-sinking area required can be estimated for a given θ_{JA}, as shown in Figure 53. θ_{JCbot} can be found in the *Thermal Information* table.



NOTE: The θ_{JA} value at a board size of 9-in^2 (that is, 3-in × 3-in) is a JEDEC standard.

Figure 53. θ_{JA} versus Board Size

Application Information (continued)

8.1.5 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are given in the *Thermal Information* table and are used in accordance with Equation 11.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \times P_D$$
$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \times P_D$$

where:

- P_D is the power dissipated as explained in Equation 9,
- T_T is the temperature at the center-top of the device package, and
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge. (11)

8.2 Typical Application

This section discusses the implementation of the TPS7A8300 using the ANY-OUT configuration to regulate a 1.6-A load requiring good PSRR at high frequency with low-noise at 1.2 V using a 1.4-V input voltage. The schematic for this typical application circuit is provided in Figure 54.

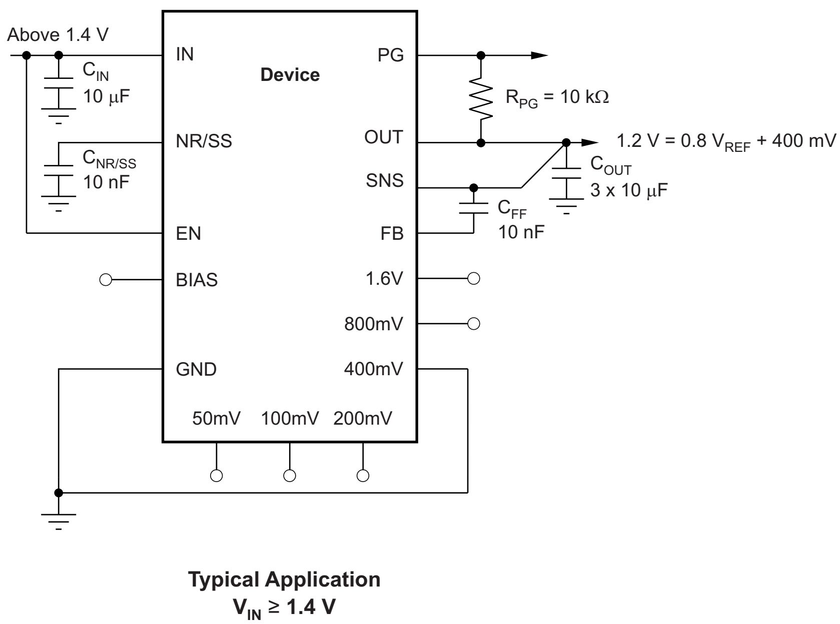


Figure 54. Typical Application

Typical Application (continued)

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 4 as the input parameters.

Table 4. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	1.4 V, ±3%, provided by the dc/dc converter switching at 1 MHz
Output voltage	1.2 V, ±1%
Output current	1.6 A (maximum), 10 mA (minimum)
RMS noise, 10 Hz to 100 kHz	< 20 µV_{RMS}
PSRR at 1 MHz	> 40 dB
Startup time	< 10 ms

8.2.2 Detailed Design Procedure

At 1.6 A, the dropout of the TPS7A8300 has 150 mV maximum dropout over temperature, thus a 200-mV headroom is sufficient for operation over both input and output voltage accuracy. The efficiency of the TPS7A8300 in this configuration is V_{OUT} / V_{IN} = 85.7%.

To achieve the smallest form factor, the 3.5-mm × 3.5-mm^2 RGR package is selected. The ANY-OUT internal resistor network is also used.

To achieve 1.2 V on the output, the 400mV pin is grounded. The voltage value of 400 mV is added to the 0.8-V internal reference voltage for $V_{OUT(NOM)}$ equal to 1.2 V; as described in Equation 12.

$$V_{OUT(NOM)} = V_{REF} + 0.4\ V = 0.8\ V + 0.4\ V = 1.2\ V \quad (12)$$

Input and output capacitors are selected in accordance with the *Capacitor Recommendation* section. Ceramic capacitances of 10 µF for the input and three 10-µF capacitors for the output are selected.

To satisfy the required startup time and still maintain low noise performance, a 10-nF $C_{NR/SS}$ is selected. This value is calculated with Equation 13.

$$t_{SS} = (V_{NR/SS} \times C_{NR/SS}) / I_{NR/SS} \quad (13)$$

With an efficiency of 85.7% and a 1.6-A maximum load, the internal power dissipation is 320 mW, which corresponds to a 11.3°C junction temperature rise for the RGR package. With an 85°C maximum ambient temperature, the junction temperature is at 96.3°C. To minimize noise, a feed-forward capacitance (C_{FF}) of 10 nF is selected.

8.2.3 Application Curves

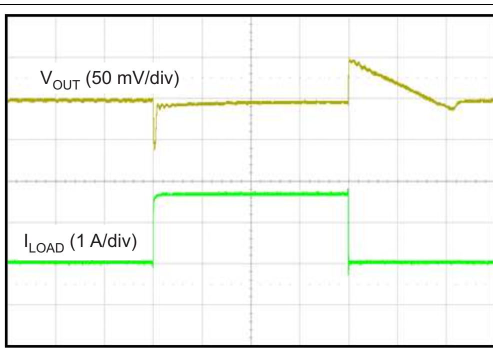


Figure 55. Output Load Transient Response

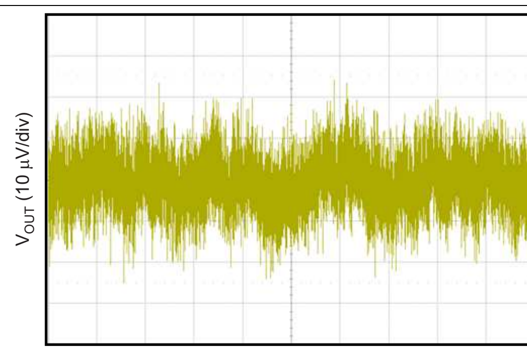


Figure 56. 10-Hz to 100-kHz Output Noise Voltage, 1.6-A Load Current

8.3 Do's and Don'ts

Do place at least one 22-µF ceramic capacitor as close as possible to the OUT terminal of the regulator.

Do not place the output capacitor more than 10 mm away from the regulator.

Do connect a 10-µF low equivalent series resistance (ESR) capacitor across the IN pin and GND input of the regulator.

Do not exceed the absolute maximum ratings.

Do not float the Enable pin.

9 Power-Supply Recommendations

The TPS7A8300 is designed to operate from an input voltage supply range between 1.1 V and 6.5 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability.

A ground reference plane is also recommended and is either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the PowerPAD™. In most applications, this ground plane is necessary to meet thermal requirements.

10.2 Layout Example

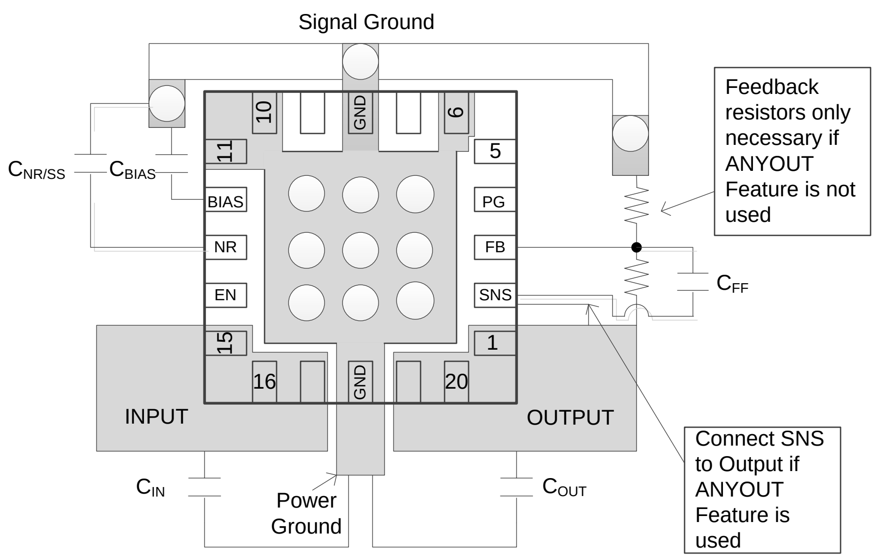


Figure 57. Example Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS7A8300. The summary information for this fixture is shown in Table 5.

Table 5. Design Kits and Evaluation Modules

NAME	LITERATURE NUMBER
TPS7A8300EVM-209 Evaluation Module	SLVU919
TPS7A8300EVM-579 Evaluation Module	SBVU021

The EVM can be requested at the Texas Instruments web site through the TPS7A8300 product folder.

11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS7A8300 is available through the TPS7A8300 product folder under simulation models.

11.1.2 Device Nomenclature

Table 6. Ordering Information(1)

PRODUCT	DESCRIPTION
TPS7A8300**YYYZ**	**YYY** is the package designator. **Z** is the package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- TPS7A8300EVM-209 Evaluation Module, SLVU919
- TPS7A8300EVM-579 Evaluation Module, SBVU021
- *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator*, SBVA042

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

ANY-OUT, DSP, PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A8300RGRR	ACTIVE	VQFN	RGR	20	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PA9Q	Samples
TPS7A8300RGRT	ACTIVE	VQFN	RGR	20	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PA9Q	Samples
TPS7A8300RGWR	ACTIVE	VQFN	RGW	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PZGM	Samples
TPS7A8300RGWT	ACTIVE	VQFN	RGW	20	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PZGM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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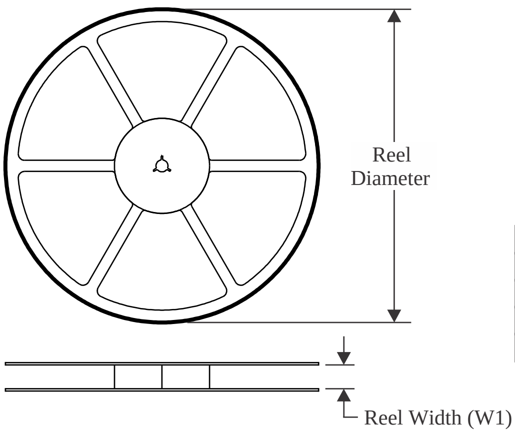
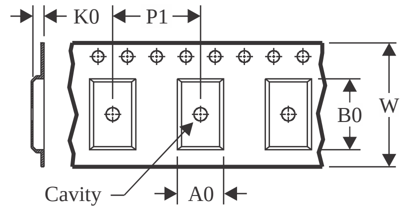
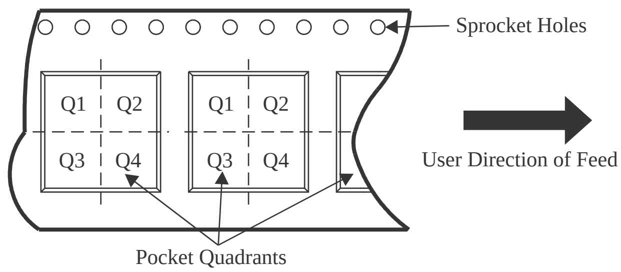
TAPE AND REEL INFORMATION





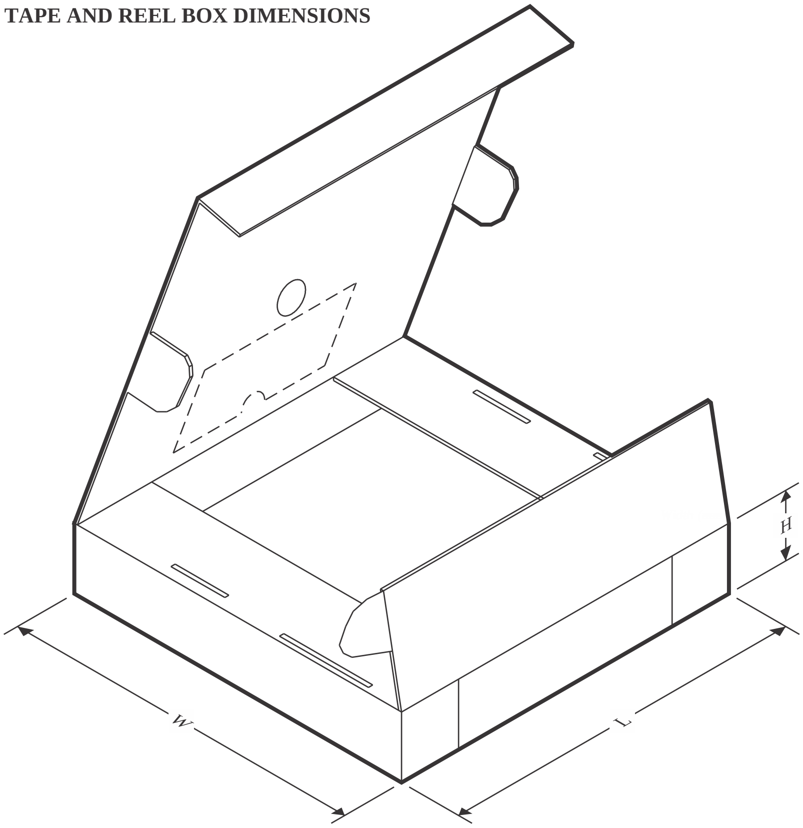
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A8300RGRR	VQFN	RGR	20	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2
TPS7A8300RGRR	VQFN	RGR	20	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2
TPS7A8300RGRT	VQFN	RGR	20	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2
TPS7A8300RGRT	VQFN	RGR	20	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2
TPS7A8300RGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS7A8300RGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS7A8300RGWT	VQFN	RGW	20	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

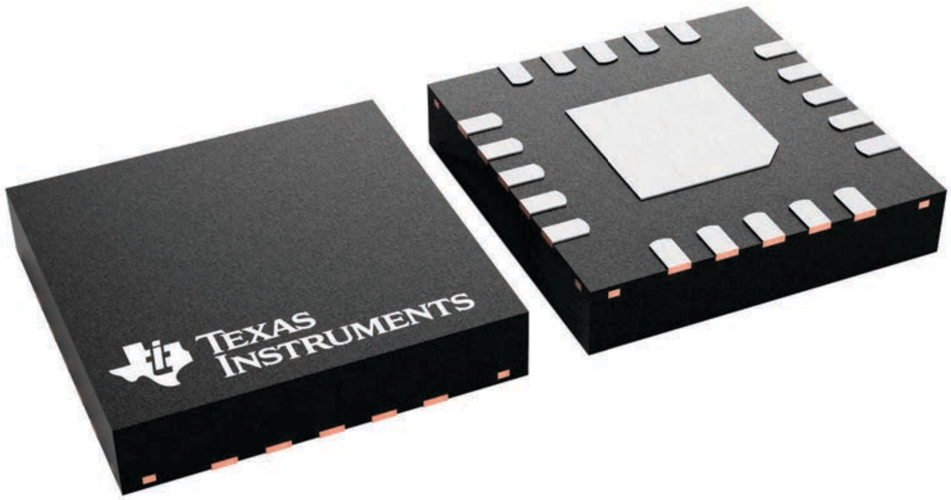
TAPE AND REEL BOX DIMENSIONS

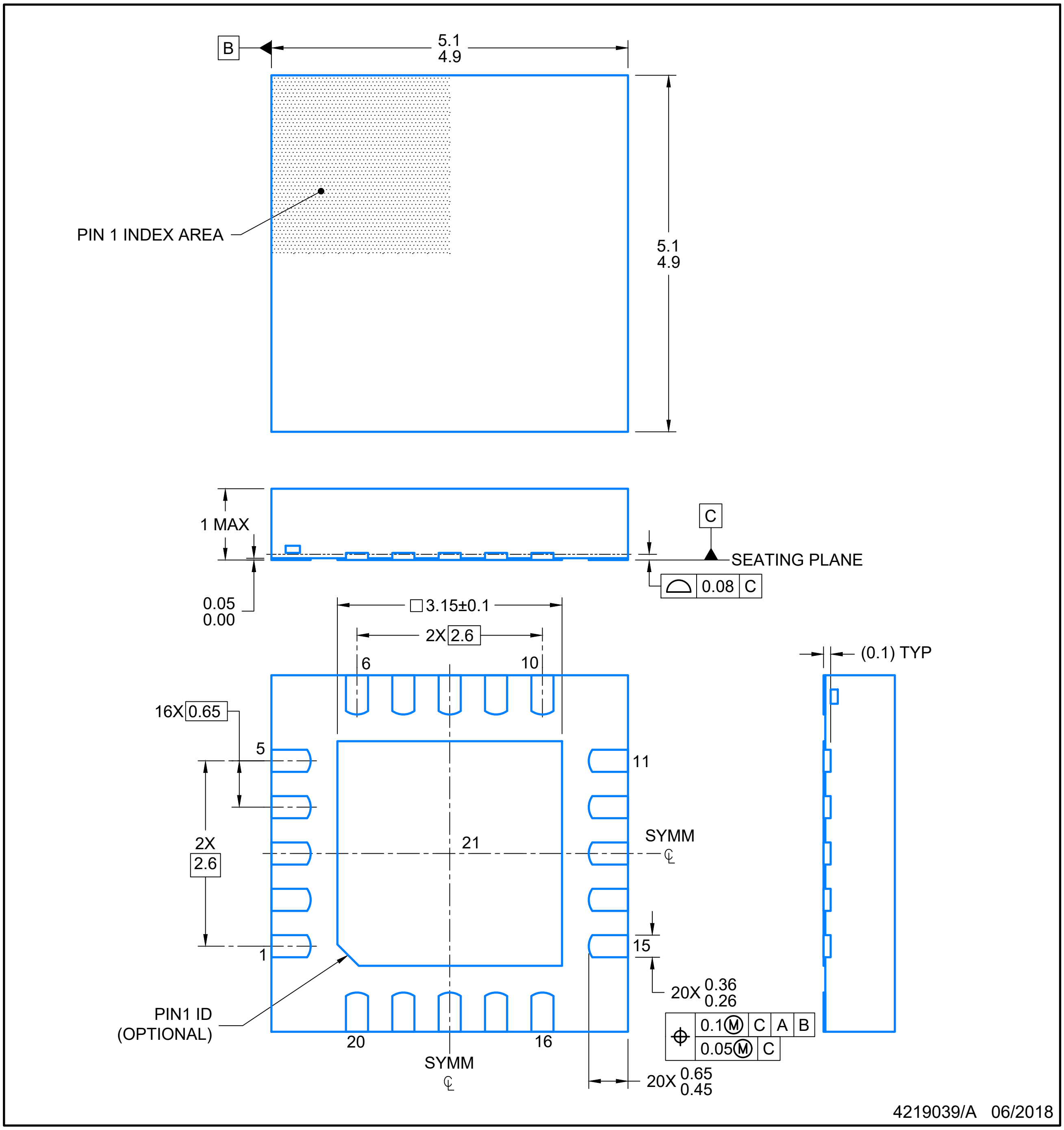


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A8300RGRR	VQFN	RGR	20	3000	367.0	367.0	35.0
TPS7A8300RGRR	VQFN	RGR	20	3000	335.0	335.0	25.0
TPS7A8300RGRT	VQFN	RGR	20	250	182.0	182.0	20.0
TPS7A8300RGRT	VQFN	RGR	20	250	210.0	185.0	35.0
TPS7A8300RGWR	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS7A8300RGWR	VQFN	RGW	20	3000	346.0	346.0	33.0
TPS7A8300RGWT	VQFN	RGW	20	250	210.0	185.0	35.0

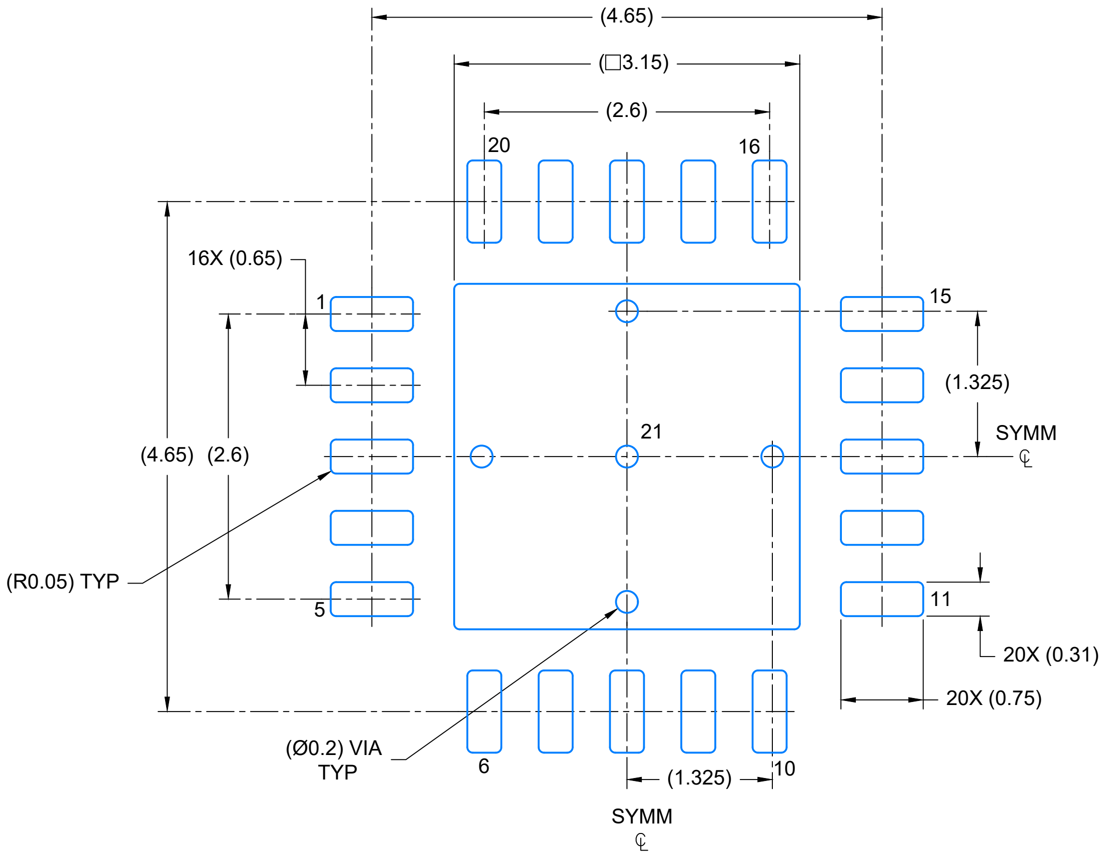
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



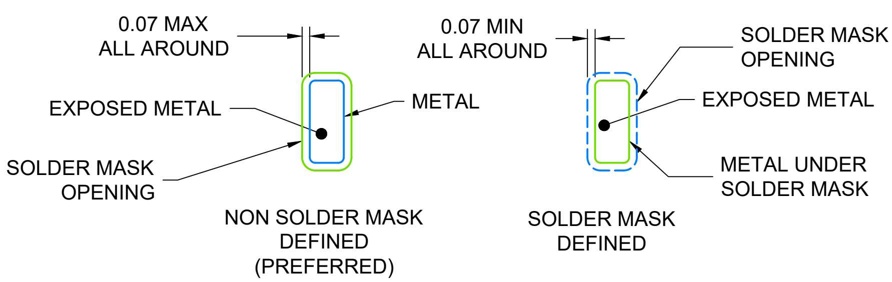


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 15X

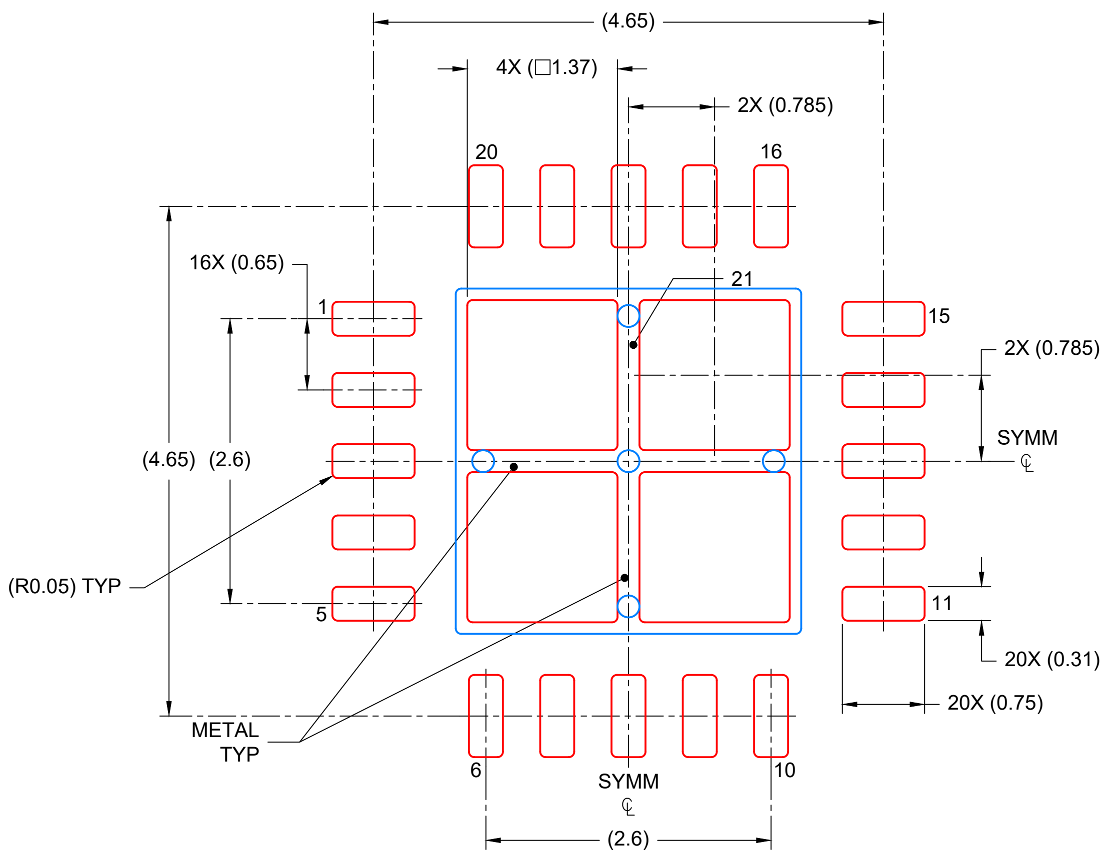


SOLDER MASK DETAILS

4219039/A 06/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED COVERAGE BY AREA
SCALE: 15X

4219039/A 06/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

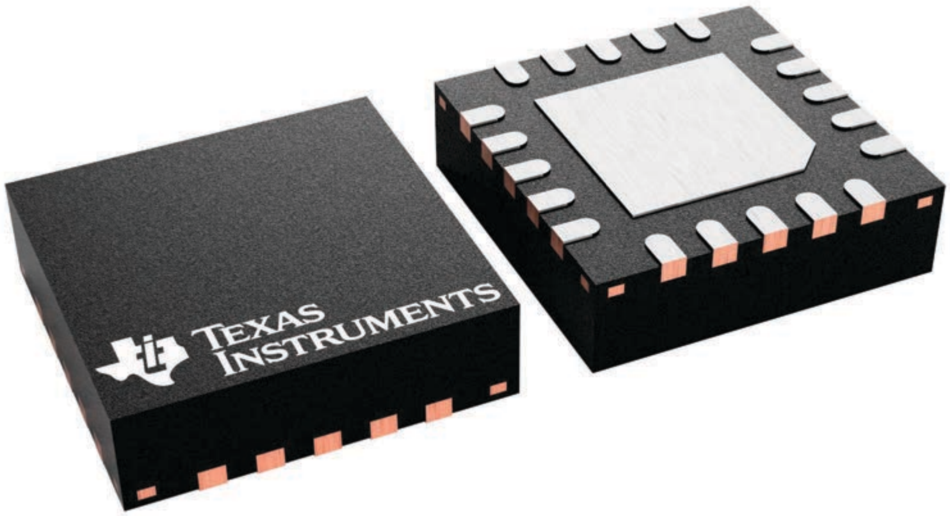
RGR 20

VQFN - 1 mm max height

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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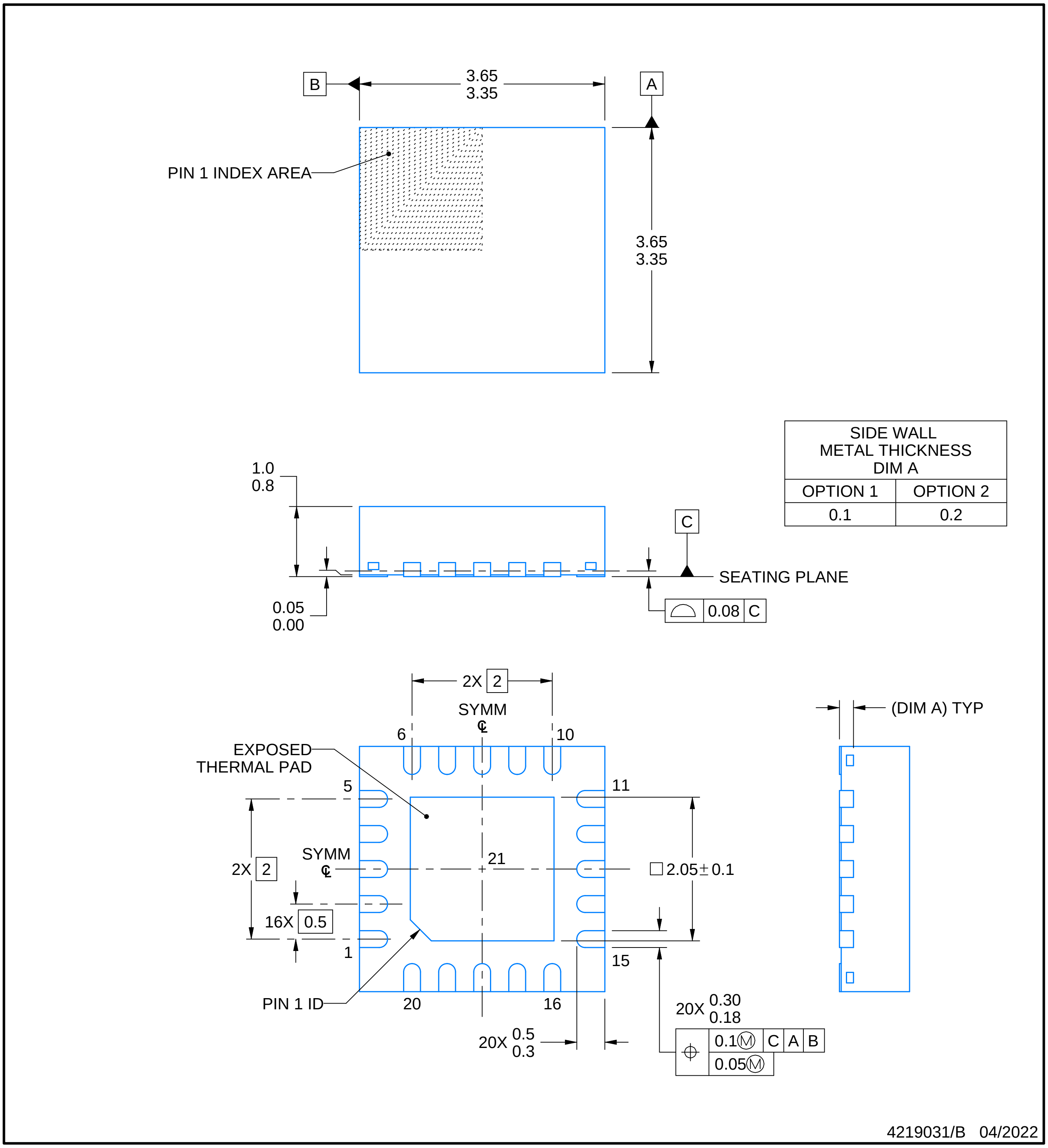
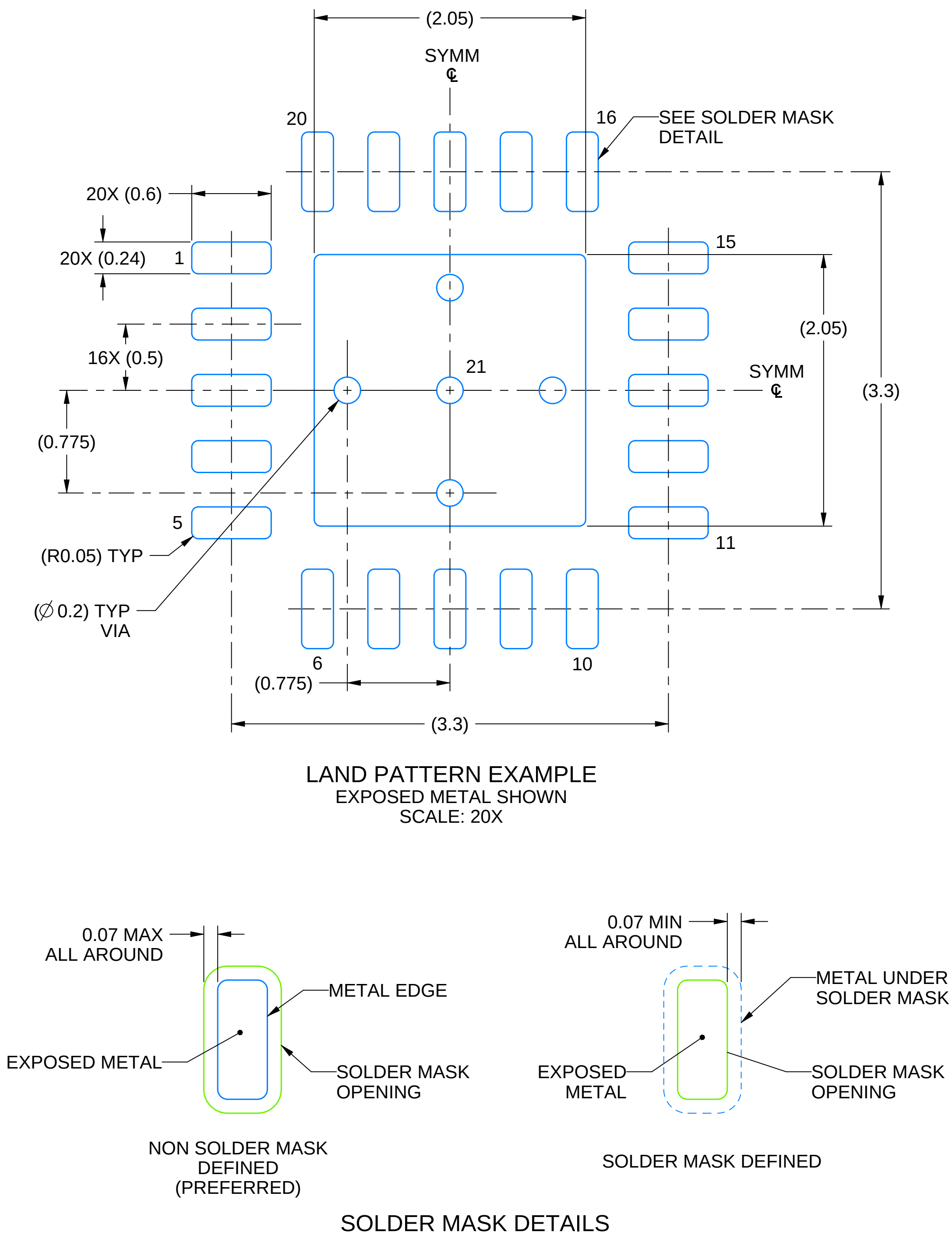


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
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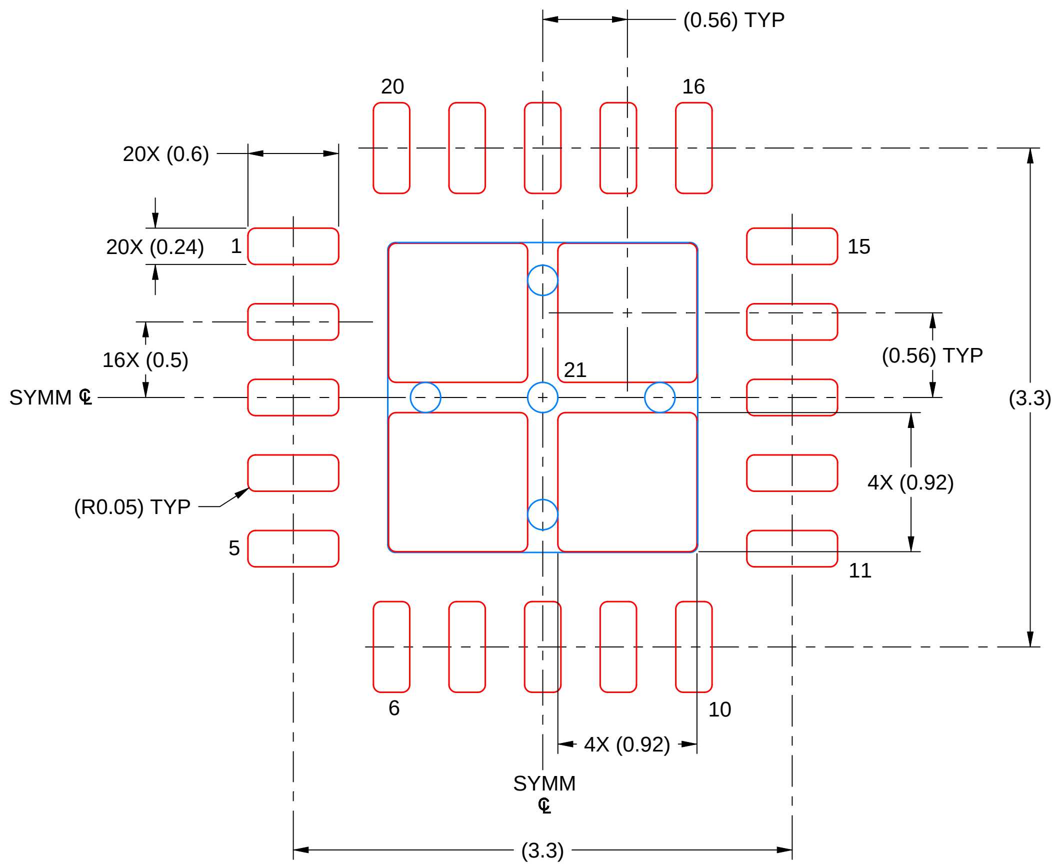

SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 21
81% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219031/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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