MS7024

TV Encoder

DATA SHEET

General Description

The MS7024 is a TV encoder device targeting handheld, portable video applications such as digital still cameras and similar portable embedded systems. The device is able to encode the video signals and generate synchronization signals for NTSC and PAL standards. Supporting NTSC-M, NTSC-J, NTSC-433, PAL-B/D/G/H/I, PAL-M, PAL-N and PAL-60 formats for TV output. The device can via 24/16/8bit digital input selector that supports different input data formats, including RGB and YUV.

Features

Input Formatter

- Supports 24-bit/16-bit/8-bit digital input
- Supports various RGB and YCrCb input data formats
- Supports for input resolutions of 720×480 and 720×576 in interlace or progressive mode
- Supports ITU-R BT.601/656 standard input
- Brightness, contrast and saturation adjustable
- Fully programmed through a serial ports

Output Formatter

- High quality 10-bit tirple-DAC
- Supports analog AV and S-Video output
- Supports formats NTSC-M, NTSC-J, NTSC-433, PAL-B/D/G/H/I, PAL-M, PAL-N and PAL-60
- Supports hot plug detection

2-wire I2C Slave Interface

Package

- TQFP-48 plastic(7mm×7mm)
- PB-free and RoHS compliant

Applications

- Video Converter/ Set-Top-Box
- Car Infotainment Device
- Portable/ Desktop Visualizer
- Video Matrix

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Function Block Diagram

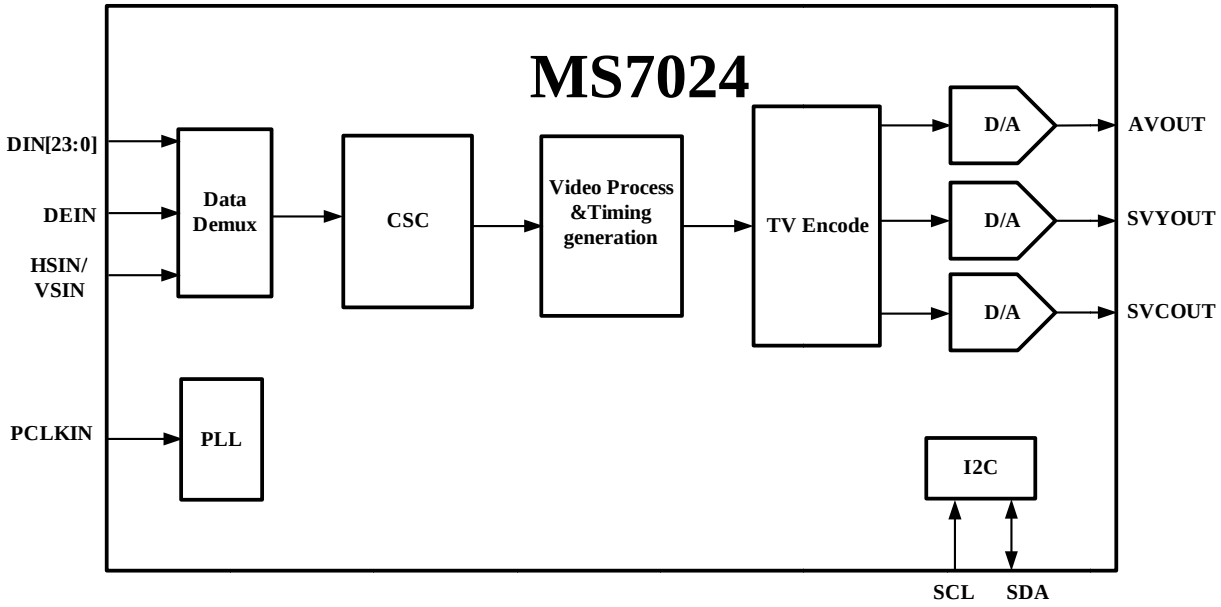


Figure 1. MS7024 Function Block

Function Description

Operation Modes

MS7024 can take non-interlaced data from the graphics controller and encode it to analog NTSC and PAL waveforms. It can also take interlaced data from sources and perform SDTV encoding.

Table 1. Operation Modes

Input Scan Type	Input Resolution	Input Data Format	Output Scan Type	Output Format	Operating Mode
Non-Interlaced	480P	RGB/ YCbCr	Interlaced	CVBS/ S-Video	SDTV encoder(NTSC/PAL) with non-interlaced input
Non-Interlaced	576P	RGB/ YCbCr	Interlaced	CVBS/ S-Video	SDTV encoder(NTSC/PAL) with non-interlaced input
Interlaced	480I	RGB/ YCbCr	Interlaced	CVBS/ S-Video	SDTV encoder(NTSC/PAL) with interlaced input
Interlaced	576I	RGB/ YCbCr	Interlaced	CVBS/ S-Video	SDTV encoder(NTSC/PAL) with interlaced input

Input Interface

The device accepts different data formats including RGB and YCrCb via 24 bit/16 bit/ 8bit multiplexed digital inputs. Most existing industrial embedded controllers are supported.

Input Clock Requirement

For different video input formats, the required clock is different. MS7024 supports three kinds of clocks (13.5Mhz/27Mhz/54Mhz). Input clock frequency variation should be within ± 0.01%.

Table 2. Clock For Different Video Formats

Resolution	Bit	CCIR	Clock(MHz)
480I	24	NA	13.5
480P	24	NA	27
576I	24	NA	13.5
576P	24	NA	27
480I	16	601	13.5
480P	16	601	27
576I	16	601	13.5
576P	16	601	27
480I	16	656	13.5
480P	16	656	27
576I	16	656	13.5

Resolution	Bit	CCIR	Clock(MHz)
576P	16	656	27
480I	8	601	27
480P	8	601	54
576I	8	601	27
576P	8	601	54
480I	8	656	27
480P	8	656	54
576I	8	656	27
576P	8	656	54

Sync Swap

MS7024 support sync swap for DEIN/HSIN/VSIN.

Table 3. Sync Swap

0x50[2:0]	000	001	010	011	100	101
Display enable	DEIN	DEIN	HSIN	HSIN	VSIN	VSIN
Vertical sync	VSIN	HSIN	VSIN	DEIN	HSIN	DEIN
Horizontal sync	HSIN	VSIN	DEIN	VSIN	DEIN	HSIN

Data Swap

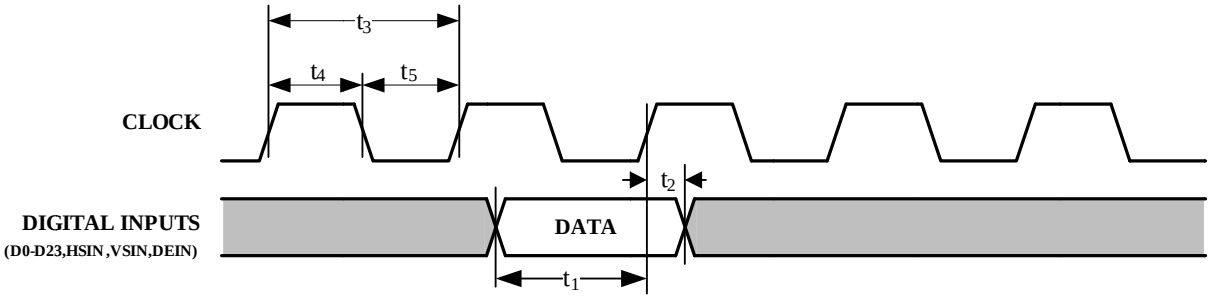
MS7024 support data swap and byte select function.

Table 4. Data Swap

Control	Input Format		0x50[6:4]					
			101	100	011	010	001	000
0x50[7] = 0	24bit RGB	R	D[15:8]	D[23:16]	D[15:8]	D[7:0]	D[7:0]	D[23:16]
		G	D[7:0]	D[7:0]	D[23:16]	D[23:16]	D[15:8]	D[15:8]
		B	D[23:16]	D[15:8]	D[7:0]	D[15:8]	D[23:16]	D[7:0]
	24bit YCbCr	Y	D[7:0]	D[7:0]	D[23:16]	D[23:16]	D[15:8]	D[15:8]
		Cb	D[23:16]	D[15:8]	D[7:0]	D[15:8]	D[23:16]	D[7:0]
		Cr	D[15:8]	D[23:16]	D[15:8]	D[7:0]	D[7:0]	D[23:16]
	16bit YCbCr	Y	D[7:0]	D[23:16]	D[15:8]	D[23:16]	D[7:0]	D[15:8]
		CbCr	D[23:16]	D[7:0]	D[23:16]	D[15:8]	D[15:8]	D[7:0]
	8bit YCbCr	YCbCr	D[7:0]	D[7:0]	D[7:0]	D[7:0]	D[15:8]	D[23:16]
0x50[7] = 1	24bit RGB	R	D[8:15]	D[16:23]	D[8:15]	D[0:7]	D[0:7]	D[16:23]
		G	D[0:7]	D[0:7]	D[16:23]	D[16:23]	D[8:15]	D[8:15]
		B	D[16:23]	D[8:15]	D[0:7]	D[8:15]	D[16:23]	D[0:7]
	24bit YCbCr	Y	D[0:7]	D[0:7]	D[16:23]	D[16:23]	D[8:15]	D[8:15]
		Cb	D[16:23]	D[8:15]	D[0:7]	D[8:15]	D[16:23]	D[0:7]

Control	Input Format		0x50[6:4]					
			101	100	011	010	001	000
		Cr	D[8:15]	D[16:23]	D[8:15]	D[0:7]	D[0:7]	D[16:23]
	16bit YCbCr	Y	D[0:7]	D[16:23]	D[8:15]	D[16:23]	D[0:7]	D[8:15]
		CbCr	D[16:23]	D[0:7]	D[16:23]	D[8:15]	D[8:15]	D[0:7]
	8bit YCbCr	YCbCr	D[0:7]	D[0:7]	D[0:7]	D[0:7]	D[8:15]	D[16:23]

Clock and Data Timing



Parameter	MIN	TYP	MAX	Unit	Condition
CLOCK CONTROL					
f_{CLK}			13.5	MHz	13.5 MHz Grade
f_{CLK}			27	MHz	27 MHz Grade
f_{CLK}			54	MHz	54 MHz Grade
Data and Control Setup, t_1	0.2			ns	
Data and Control Hold, t_2	1.5			ns	
Clock Pulse width High, t_4	9.25			ns	f_{CLK_MAX} = 54 MHz
Clock Pulse width Low t_5	9.25			ns	f_{CLK_MAX} = 54 MHz
Clock Pulse width High t_4	18.5			ns	f_{CLK_MAX} = 27 MHz
Clock Pulse width Low t_5	18.5			ns	f_{CLK_MAX} = 27 MHz
Clock Pulse width High t_4	37			ns	f_{CLK_MAX} = 13.5 MHz
Clock Pulse width Low t_5	37			ns	f_{CLK_MAX} = 13.5 MHz

Figure 2. Timing Diagram

MS7024 provide clock invert function, as follows:

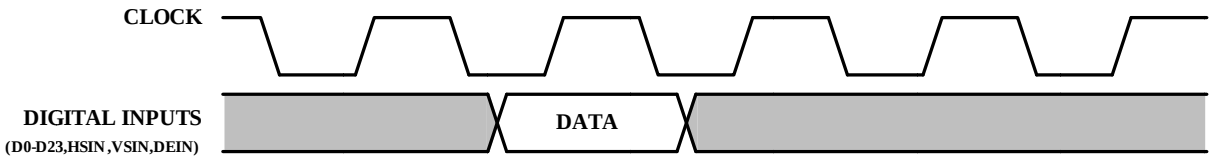


Figure 3. Clock Inverse Function

TV Output

TV Output Format

The MS7024 support the following output formats:

Table 5.Support TV Output Format

No.	Standards	Field Rate(Hz)	Total	Scan Type
1	NTSC-M	60/1.001	858x525	Interlaced
2	NTSC-J	60/1.001	858x525	Interlaced
3	NTSC-443	60/1.001	858x525	Interlaced
4	PAL-B/D/G/H/I	50	864x625	Interlaced
5	PAL-M	50	864x625	Interlaced
6	PAL-N	50	864x625	Interlaced
7	PAL-N	50	864x625	Interlaced
8	PAL-60	60/1.001	858x525	Interlaced

Video DAC Output

MS7024 provides three DACs for multiple outputs, as follows:

Table 6. Video Output

PIN / STDV	AVOUT	SVYOUT	SVCOUT
Single CVBS	CVBS		
		CVBS	
			CVBS
Dual CVBS	CVBS	CVBS	
	CVBS		CVBS
		CVBS	CVBS
Triple CVBS	CVBS	CVBS	CVBS
CVBS+S-Video	CVBS	S-Video-Y	S-Video-C
	CVBS	S-Video-C	S-Video-Y
	S-Video-Y	CVBS	S-Video-C
	S-Video-C	CVBS	S-Video-Y
	S-Video-Y	S-Video-C	CVBS
	S-Video-C	S-Video-Y	CVBS
S-Video	S-Video-Y	S-Video-C	
	S-Video-Y		S-Video-C
	S-Video-C	S-Video-Y	
		S-Video-Y	S-Video-C
	S-Video-C		S-Video-Y
		S-Video-C	S-Video-Y

PIN Map

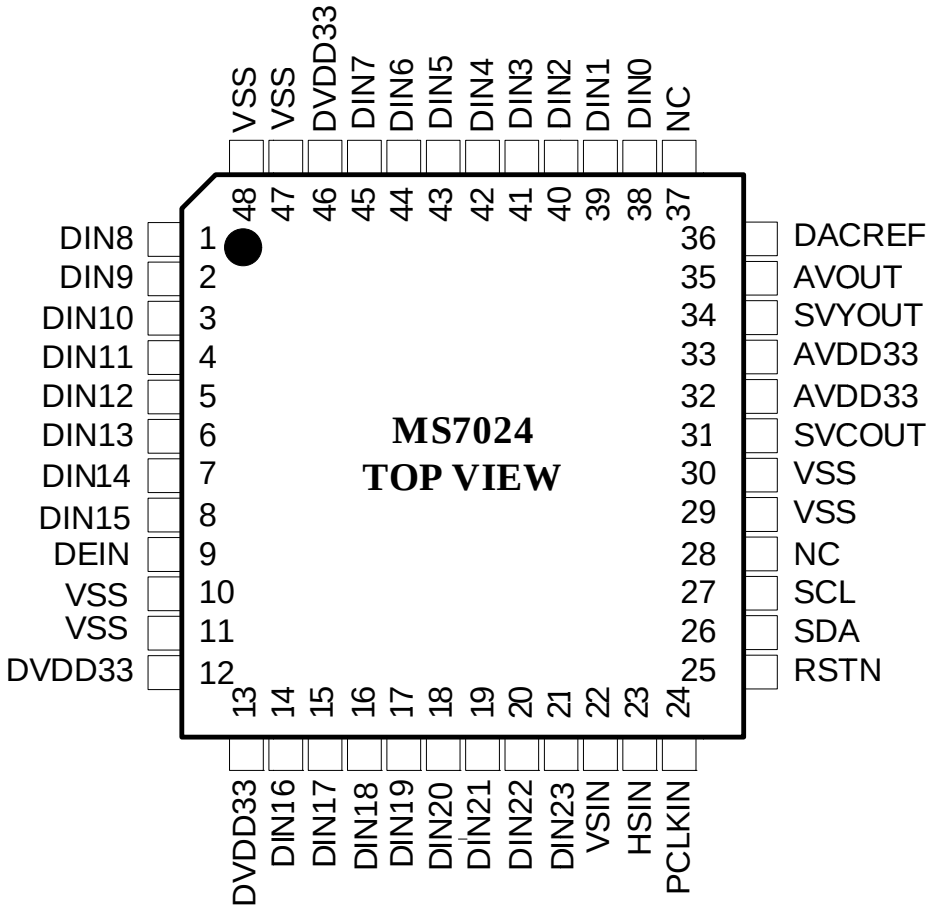


Figure 4. MS7024 Package Top View

PIN Description

Table 7. PIN Description

Pin Name	Pin #	Type	Description
System			
RSTN	25	DI	External reset in, active low
SCL	27	DI	Serial bus clock
SDA	26	DIO	Serial bus data
Digital Video Interface			
HSIN	23	DI	Horizontal sync input
VSIN	22	DI	Vertical sync input
PCLKIN	24	DI	Video pixel clock input
DEIN	9	DI	Video display enable input
DIN[0:7]	38-45	DI	Digital video input Byte0
DIN[8:18]	1-8	DI	Digital video input Byte1
DIN[16:23]	14-21	DI	Digital video input Byte2
Analog Video Output			
DACREF	36	AI	Full-scale adjust reference resistor
AVOUT	35	AO	Analog component CVBS output
SVCOUT	31	AO	Analog component S-Video C output
SVYOUT	34	AO	Analog component S-Video Y output
Power and Ground			
DVDD33	12,13,46	P	Digital Power 3.3V
AVDD33	32,33	P	Analog Power 3.3V
VSS	10,11,29,30, 47,48	G	Ground

Table 8. Abbreviation Of Pin Description

Abbreviation	Description
AI	Analog Input
AO	Analog Output
DI	Digital Input
DIO	Digital Bi-direction
P	Power
G	Ground
NC	No Connect

Electrical Characteristics

Absolute Maximum Ratings

Table 9. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Ambient Operating Temperature	TA	0 to 70	℃
Storage Temperature	Tsto	-40 to 150	℃
ESD Ratings	Vsed		
Human Body Model		2000	V
Machine Model		200	V

Note1：Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and does not imply functional operation of the device. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

ESD CAUTION: Electrostatic charges accumulate on the human body and test equipment and can discharge without detection. Although this product features has dedicated ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

DC Characteristics

Table 10. DC Characteristics

Parameter	Symbol	MIN	TYP	MAX	Unit
Analog 3.3V Power	AVDD33	2.97	3.3	3.63	V
Digital IO Power	DVDD33	2.97	3.3	3.63	V
Analog 3.3V Current (Note 2)	I_{AVDD33}		35		mA
Digital IO Power Current	I_{DVDD33}		25		mA

Note 2：The AVDD33 supply current is 18mA for one DAC single 75Ohm termination. The current will be 35mA for one DAC double 75Ohm termination(37.5Ohm). For two DACs, the current will be doubled according to different terminations.

Video DAC Characteristics

Table 11. Video DAC Characteristics

Analog Output	MIN	TYP	MAX	UNIT
Full-scale Output Current AV/S-Video		34		mA
Video Level Error		10		%
Voltage Reference				
Reference Voltage Output		1.22		V
Static Performance				
DAC Resolution		10		Bit

Analog Output	MIN	TYP	MAX	UNIT
DNL (Differential Non-Linearity)		+/-0.5		LSB
INL (Integral Non-Linearity)		+/-0.7		LSB
Dynamic Performance				
Power Supply				
Supply Voltage	2.97	3.3	3.63	V

Package Outline

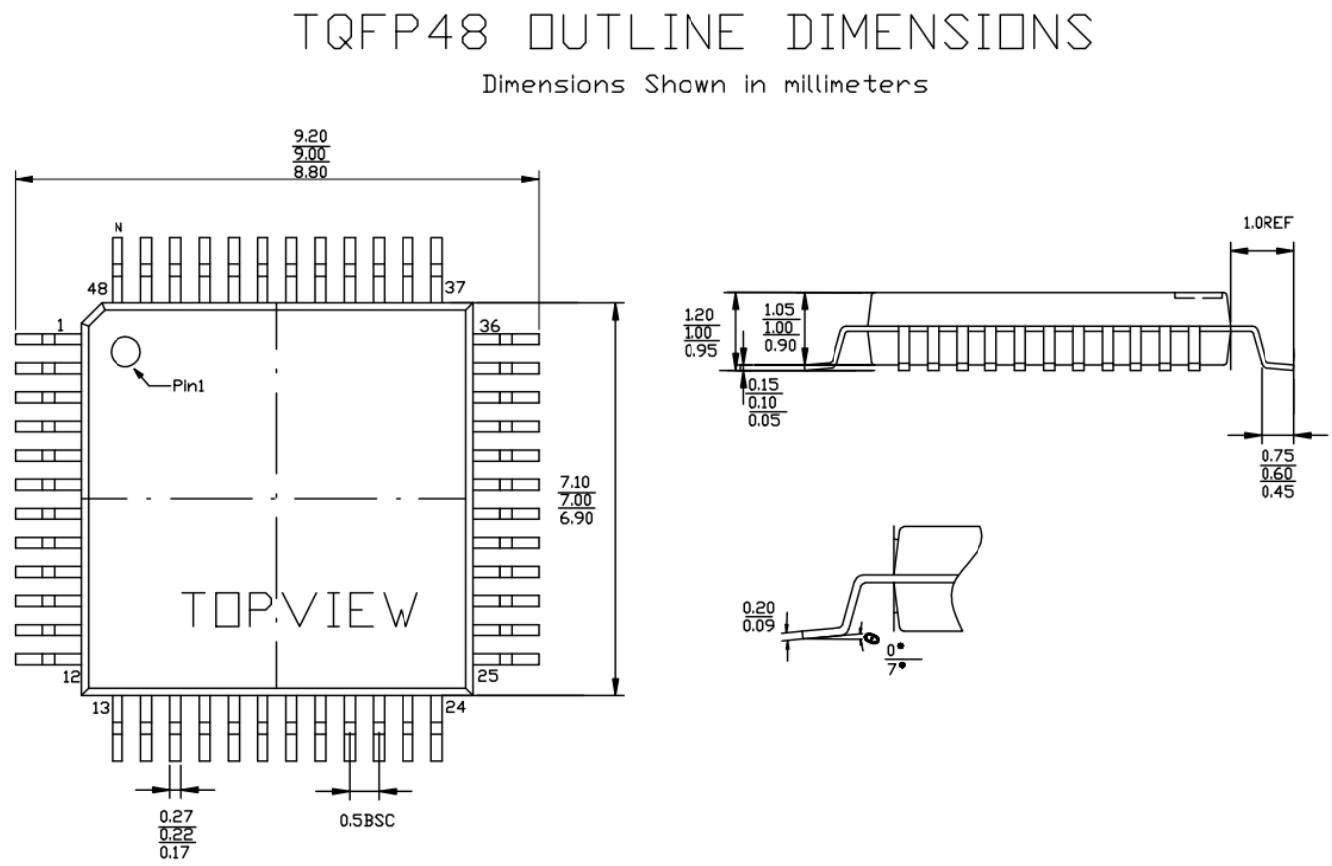


Figure 5. TQFP48 Package Diagram

Top Mark

Figure 6. MS7024 Top Mark Diagram

Revision History

Date	Version	Author	Comments
2015-9-2	V1.0	Tina Wang	Initial Version
2016-4-8	V1.1	Feng Gu	Add Absolute Maximum Ratings