Features

- Input Voltage Range: 2.2 V to 6.5 V
- Output Voltage Options:
  - Fixed Output Voltage: 0.8 V to 5 V
  - Adjustable Output Voltage: 0.8 V to 5.2 V
- 3% Accuracy over Line Regulation, Load Regulation, and Operating Temperature Range
- 1 A Maximum Output Current
- Low Dropout Voltage: 500 mV Maximum at 1 A
- High PSRR:
  - 65 dB at 1 kHz
  - 50 dB at 100 kHz
- 24 μV_{RMS} Output Voltage Noise (100 Hz to 100kHz)
- Excellent Transient Response
- Stable with a 10 μF or Larger Ceramic Output Capacitor
- Thermal Shutdown and Over-Current Protection
- Operating Junction Temperature: –40°C to +125°C
- Package: 3×3 DFN-8

Applications

- Wireless Communication: CPU, ASIC, FPGA, CPLD, DSP
- High-Performance Analog: ADC, DAC, LVDS, VCO
- Noise-Sensitive Imaging: CMOS Sensors, Video ASICs

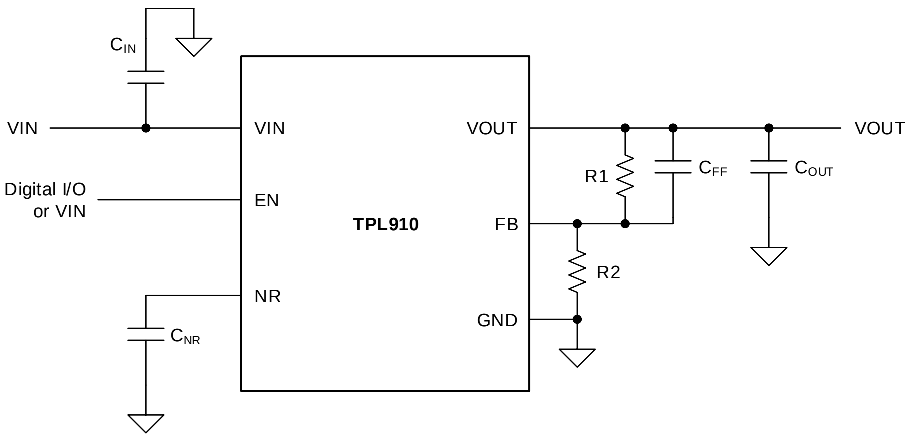
Description

The TPL910 series products are 1-A high-current, 24-μV_{RMS} low-noise, high-PSRR, high-accuracy linear regulators with only 500-mV maximum ultra-low dropout voltage at 1-A load current. The TPL910 series products support both fixed output voltage ranges from 0.8 V to 5 V and adjustable output voltage ranges from 0.8 V to 5.2 V with external resistor divider.

Ultra-low noise, high PSRR, and high output current capability makes the TPL910 series products ideal power supply for noise-sensitive applications, such as high-speed communication facilities, test and measurement devices, or high-definition imaging equipment. Accurate output voltage tolerance, output remote sensing, excellent transient response, and adjustable soft-start control ensures the TPL910 series products optimal power supply for the large-scale processors or digital loads, such as ASIC, FPGA, CPLD and DSP.

The TPL910 series products provide 3×3 DFN-8 package with guaranteed operating junction temperature range (T_J) from –40°C to +125°C.

Typical Application Schematic



Product Family Table

Part Number	Output Voltage	Orderable Number	Package	Transport Media, Quantity	MSL	Marking information
TPL910	Adjustable (0.8 V ~ 5.2 V)	TPL910ADJ-DF6R	3×3 DFN-8	4,000	MSL3	L910A

Table of Contents

Revision History

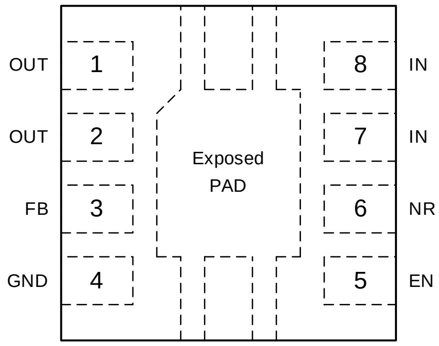
Date	Revision	Notes
2019/04/30	Rev.Pre	Preliminary Version
2020/05/08	Rev.A.0	Initial Release
2021/06/07	Rev.A.1	1. Update the top view figure of DFN-8 Package in Page 5 2. Add Tape and Reel Information in Page 16 3. Change Package Outline Dimensions, 3×3 DFN-8, in Page 17

Pin Configuration and Functions

TPL910 Series

DFN-8 Package

Top View



Pin Functions

NAME	PIN NUMBER	TYPE	DESCRIPTION
EN	5	I	Regulator enable pin. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to IN directly.
FB	3	I	Output voltage feedback pin. Connect to an external resistor divider to adjust the output voltage. A 10-nF feed-forward capacitor from FB to OUT (as close as possible to FB pin) is recommended to maximize regulator ac performance.
GND	4	–	Ground reference pin. Connect GND pin to PCB ground plane directly.
IN	7, 8	I	Input voltage pin. A 10-µF or larger ceramic capacitor from IN to ground (as close as possible to IN pin) is required to reduce the jitter from previous-stage power supply.
NR	6	I	Noise-reduction and soft-start pin. A 10-nF or larger capacitor from NR/SS to GND (as close as possible to NR/SS pin) is recommended to maximize ac performance.
OUT	1, 2	O	Regulated output voltage pin. A 10-µF or larger ceramic capacitor from OUT to ground (as close as possible to OUT pin) is required to ensure regulator stability.

(1) Exposed PAD must be connected to a large-area ground plane to maximum the thermal performance.

Specifications

Absolute Maximum Ratings

		MIN	MAX	UNIT
IN, EN		–0.3	7	V
OUT		–0.3	V_{IN} + 0.3	V
FB, NR		–0.3	3.6	V
T_J	Junction Temperature Range	–40	150	°C
T_{STG}	Storage Temperature Range	–65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond the Absolute Maximum Ratings may permanently damage the device.

(2) All voltage values are with respect to GND.

ESD Ratings

		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	±4000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	±1500	V

Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
IN	Input voltage	2.2		6.5	V
EN	Enable voltage	0		6.5	V
OUT	Output voltage	0.8		5.2	V
OUT	Output current	0		1	A
C_{IN}	Input capacitor	10			μF
C_{OUT}	Output capacitor	10			μF
C_{FF}	Feed-forward capacitor		10		nF
C_{NR}	NR capacitor		10		nF
P_D	Power dissipation		1000		mW
T_J	Junction Temperature Range	–40		125	°C

Thermal Information

PACKAGE	θ_{JA}	$\theta_{JC,bottom}$	UNIT
3×3 DFN-8	69.3	8.16	°C/W

Electrical Characteristics

T_J = –40°C to +125°C (typical value at T_J = +25°C), V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.2 V, whichever is greater; V_{EN} = 2.2 V, I_{OUT} = 1 mA, C_{IN} = 10 μF, C_{OUT} = 47 μF, C_{NR} = 10 nF, C_{FF} = open, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Input Voltage and Current						
V_{IN}	Input supply voltage range (1)		2.2		6.5	V
UVLO	Input supply UVLO	VIN rising, R_L = 1 kΩ		1.3	2.1	V
	Hysteresis			200		mV
I_{GND}	GND pin current	V_{IN} = 6.5 V, I_{OUT} = 1 mA		15	30	mA
		V_{IN} = 6.5 V, I_{OUT} = 1 A		15	30	mA
I_{SD}	Shutdown current	V_{IN} = 6.5 V, V_{EN} = Low		10	25	μA
Device Enable						
$V_{IH(EN)}$	EN pin high-level input voltage	Device enable	1.2		6.5	V
$V_{IL(EN)}$	EN pin low-level input voltage	Device disable	0		0.4	V
I_{EN}	EN pin current	V_{IN} = 6.5 V, V_{EN} = 0 V to 6.5 V		0.1	1	μA
Regulated Output Voltage and Current						
V_{FB}	Feedback voltage		0.79	0.8	0.81	V
I_{FB}	FB pin leakage current	V_{IN} = 6.5 V, stress V_{FB} = 0.8V		0.1	1	μA
V_{NR}	NR/SS pin voltage			0.8		V
I_{NR}	NR/SS pin charging current	V_{IN} = 6.5 V, V_{NR} = GND		7.2	9	μA
V_{OUT}	Output accuracy (2)	V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.5 V to 6 V, V_{OUT} = 0.8 V to 5.2 V, I_{OUT} = 100 mA to 500 mA	–2%		2%	
		V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.2 V to 6.5 V, V_{OUT} = 0.8 V to 5.2 V, I_{OUT} = 100 mA to 1 A	–3%		3%	
ΔV_{OUT}	Line regulation	V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.2 V to 6.5 V, I_{OUT} = 100 mA		0.03		mV/V
	Load regulation	I_{OUT} = 100 mA to 1 A		0.07		mV/A
V_{DO}	Dropout voltage (1)	V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.2 V to 6.5 V, I_{OUT} = 500 mA, V_{FB} = GND or V_{SNS} = GND			250	mV
		V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.2 V to 6.5 V, I_{OUT} = 750 mA, V_{FB} = GND or V_{SNS} = GND			350	mV
		V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.2 V to 6.5 V, I_{OUT} = 1 A, V_{FB} = GND or V_{SNS} = GND			500	mV
I_{LIM}	Output current limit	V_{OUT} forced at 0.9 × $V_{OUT(NOM)}$, V_{IN} ≥ 3.3 V	1.1.	1.4		A
t_{STR}	Start-up time	$V_{OUT(NOM)}$ = 3.3 V, V_{OUT} = 0% to 90% $V_{OUT(NOM)}$, R_L = 3.3 kΩ, C_{OUT} = 10 μF, C_{NR} = 100 nF		13		ms

(1) Minimum V_{IN} = $V_{OUT(NOM)}$ + V_{DO} or 2.2 V, whichever is greater.

(2) Resistor tolerance is not included. Output accuracy is not tested at this condition: V_{OUT} = 0.8 V, 4.5V ≤ V_{IN} ≤ 6.5 V, and 750 mA ≤ I_{OUT} ≤ 1 A, because the power dissipation is out of package limitation.

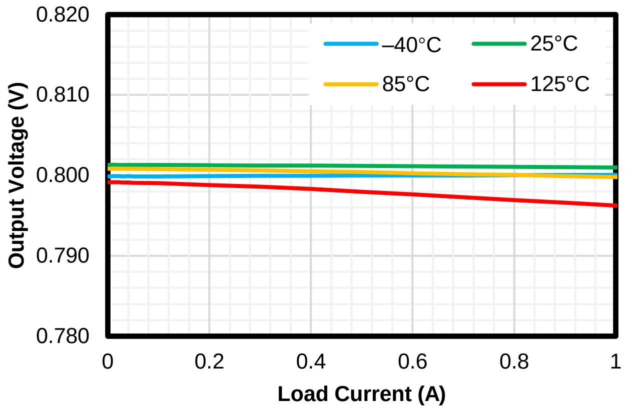
Electrical Characteristics (continued)

T_J = –40°C to +125°C (typical value at T_J = +25°C), V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.2 V, whichever is greater; V_{EN} = 2.2 V, I_{OUT} = 1 mA, C_{IN} = 10 µF, C_{OUT} = 47 µF, C_{NR} = 10 nF, C_{FF} = open, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
PSRR and Noise							
PSRR	Power supply ripple rejection	V_{IN} = 5.5 V, V_{OUT} = 5.2 V, I_{OUT} = 1 A	f = 1 kHz		65		dB
			f = 100 kHz		50		dB
			f = 1 MHz		30		dB
V_N	Output noise voltage	BW = 100 Hz to 100 kHz, V_{IN} = 5.5 V, V_{OUT} = 5.2 V, I_{OUT} = 1 A, C_{NR} = 100 nF, C_{FF} = 10 nF			24		μV_{RMS}
Temperature Range							
T_{SD}	Thermal shutdown threshold	Temperature increasing			160		°C
	Hysteresis				20		°C
T_J	Operating junction temperature			–40		125	°C

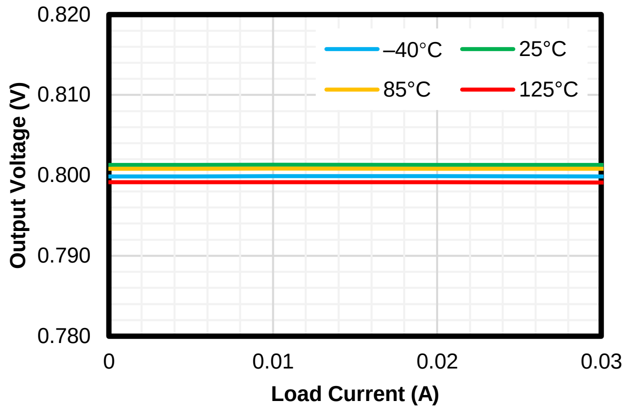
Typical Performance Characteristics

V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.2 V, whichever is greater; V_{EN} = 2.2 V, C_{IN} = 10 µF, C_{OUT} = 47 µF, C_{NR} = 10 nF, C_{FF} = open, unless otherwise noted.



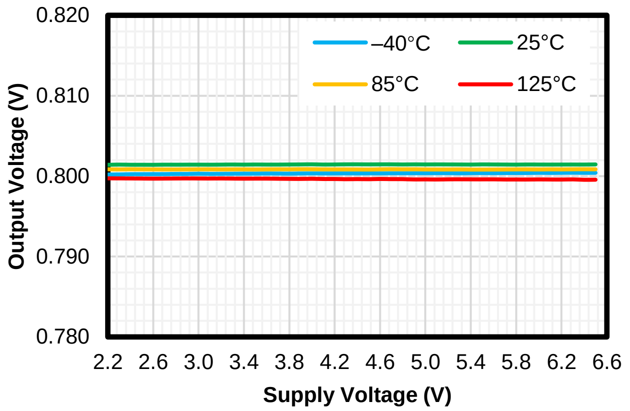
V_{OUT} = 0.8 V

Figure 1 Load Regulation



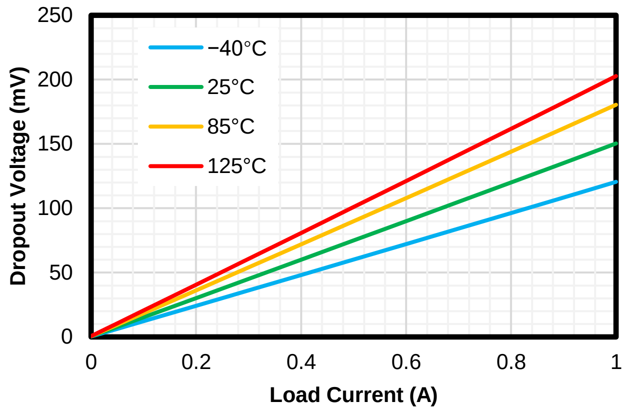
V_{OUT} = 0.8 V

Figure 2 Load Regulation at Light Load



V_{OUT} = 0.8 V, I_{OUT} = 5 mA

Figure 3 Line Regulation



V_{OUT} = 1.5 V

Figure 4 Dropout Voltage vs. Load Current

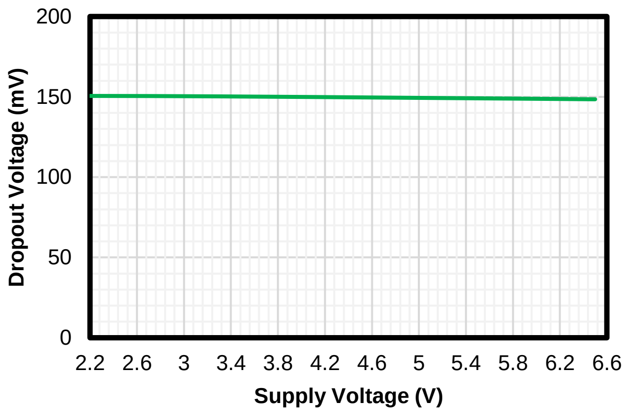


Figure 5 Dropout Voltage vs. Supply Voltage

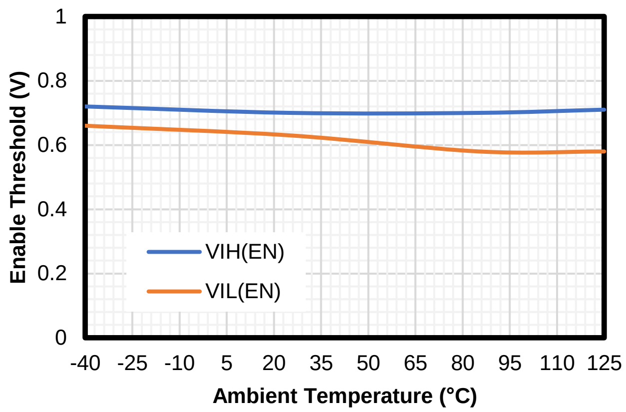


Figure 6 Enable Threshold vs. Temperature

Typical Performance Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.2 V, whichever is greater; V_{EN} = 2.2 V, C_{IN} = 10 µF, C_{OUT} = 47 µF, C_{NR} = 10 nF, C_{FF} = open, unless otherwise noted.

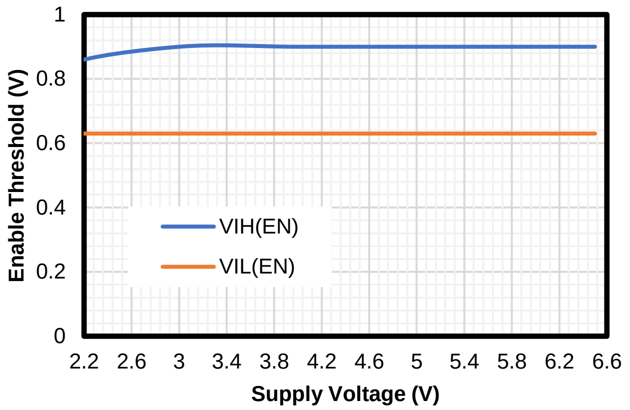
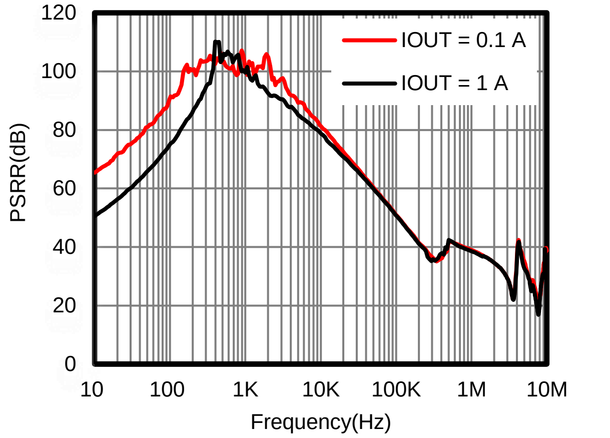
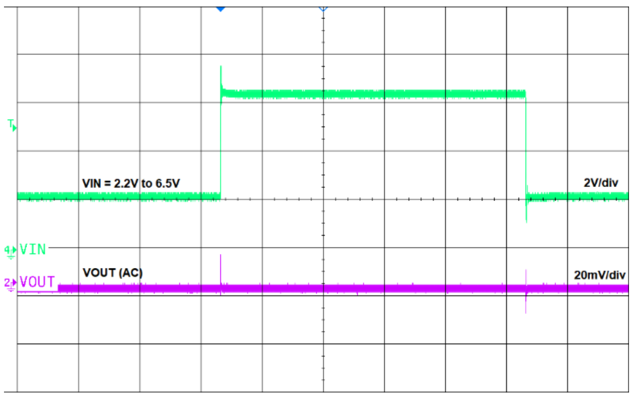


Figure 7 Enable Threshold vs. Supply Voltage



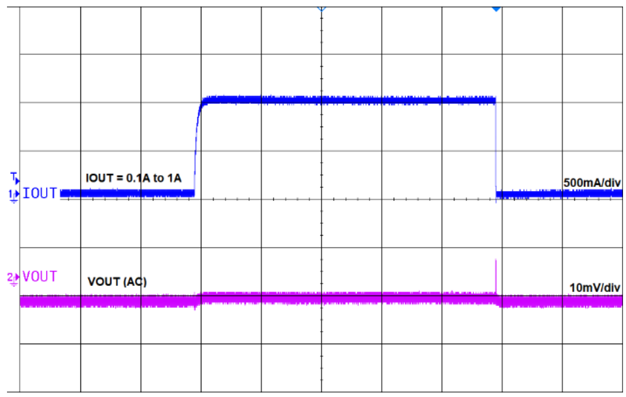
V_{IN} = 5.5 V, V_{OUT} = 5.2 V, C_{OUT} = 47µF // 10µF // 10µF, $C_{NR/SS}$ =100nF, C_{FF} = open

Figure 8 PSRR



V_{IN} = 2.2V to 6.5V, V_{OUT} = 0.8V

Figure 9 Line Transient



I_{OUT} = 0.1A to 1A, V_{OUT} = 0.8V

Figure 10 Load Transient

Detailed Description

Overview

The TPL910 series products are 1-A high-current, 24-μV_{RMS} low-noise, high-PSRR, high-accuracy linear regulators with only 500-mV maximum ultra-low dropout voltage at 1-A load current. The TPL910 series products support both fixed output voltage ranges from 0.8 V to 5 V and adjustable output voltage ranges from 0.8 V to 5.2 V with external resistor divider.

Ultra-low noise, high PSRR, and high output current capability makes the TPL910 series products ideal power supply for noise-sensitive applications, such as high-speed communication facilities, test and measurement devices, or high-definition imaging equipment. Accurate output voltage tolerance, output remote sensing, excellent transient response, and adjustable soft-start control ensures the TPL910 series products optimal power supply for the large-scale processors or digital loads, such as ASIC, FPGA, CPLD and DSP.

Functional Block Diagram

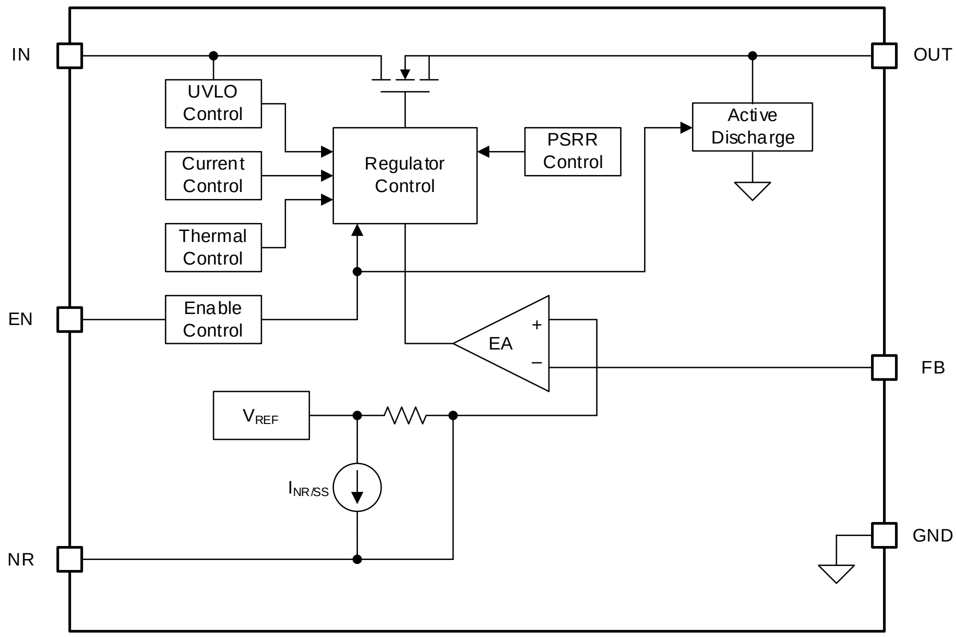


Figure 11 Functional Block Diagram

Feature Description

Enable (EN)

The TPL910 series provide a device enable pin (EN) to enable or disable the device. Connect this pin to the GPIO of an external digital logic control circuit to control the device. When the V_{EN} voltage falls below $V_{IL(EN)}$, the LDO device turns off, and when the V_{EN} ramps above $V_{IH(EN)}$, the LDO device turns on.

Under-Voltage Lockout (IN and UVLO)

The TPL910 series use an under-voltage lockout circuit to keep the output shut off until the internal circuitry operates properly.

Voltage Regulation (OUT and FB)

The TPL910 series provide adjustable output voltage option. Using external resistors divider, the output voltage of TPL910 series is determined by the value of the resistor R1 and R2 in Figure 12. Use Equation 1 to calculate the output voltage.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

Where the feedback voltage V_{FB} is 0.8 V.

Table 1 provides a list of recommended resistor combinations to achieve the common output voltage values.

Table 1 External Resistor Combinations

Target Output Voltage (V)	External Resistors Divider		Calculated Output Voltage (V)
	R1 (kΩ)	R2 (kΩ)	
0.80	0	Open	0.800
0.81	2	160	0.810
0.82	4.02	160	0.820
0.83	6.04	160	0.830
0.84	8.06	160	0.840
0.85	10	160	0.850
0.86	12	160	0.860
0.87	12.4	143	0.869
0.88	12.4	124	0.880
0.89	12	107	0.890
0.90	12.4	100	0.899
0.95	12.4	66.5	0.949
1.00	12.4	49.9	0.999
1.10	12.4	33.2	1.099
1.20	12.4	24.9	1.198
1.50	12.4	14.3	1.494
1.80	12.4	10	1.792
1.90	12.1	8.87	1.891
2.50	12.4	5.9	2.481
2.85	12.1	4.75	2.838
3.00	12.1	4.42	2.990
3.30	11.8	3.74	3.324
3.60	12.1	3.48	3.582
4.50	11.8	2.55	4.502
5.00	12.4	2.37	4.986

Output Active Discharge

The TPL910 series integrate an output discharge path from OUT to GND. When the device is disabled, either EN or VIN is lower than turn-on threshold, the output will actively discharge the output voltage through an internal resistor of several hundred ohms.

Do not rely on this active discharge circuit for discharging large output capacitors when the input voltage falls below the output voltage. Reverse current flow through internal power MOSFET can permanently damage the device, and external current protection is essential at this condition.

Over-Current Protection

The TPL910 series integrate an internal current limit that helps to protect the device during fault conditions. When the output is pulled down below the target output voltage, over-current protection starts to work and limit the output current to a typical value of 1.4 A. Under the over-current conditions, the internal junction temperature ramps up quickly. When the junction temperature is high enough, it will cause the over temperature protection.

Over-Temperature Protection

The recommended operating junction temperature range is –40°C to 125°C. When the junction temperature is between 125°C and the thermal shutdown (TSD) threshold, the regulator can still work well, but will reduce the device lifetime for long-term using.

The over-temperature protection works when the junction temperature exceeds the thermal shutdown (TSD) threshold, which turns off the regulator immediately. Until when the device cools down and the junction temperature falls below the thermal shutdown threshold minus thermal shutdown hysteresis, the regulator turns on again.

Application and Implementation

NOTE

Information in the following applications sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPL910 series products are 1-A high-current, 24-μV_{RMS} low-noise, high-PSRR, high-accuracy linear regulators with only 500-mV maximum ultra-low dropout voltage. The following application schematic shows a typical usage of the TPL910 series.

Typical Application

Adjustable Output Operation

Figure 12 shows the typical application schematic of the TPL910 series.

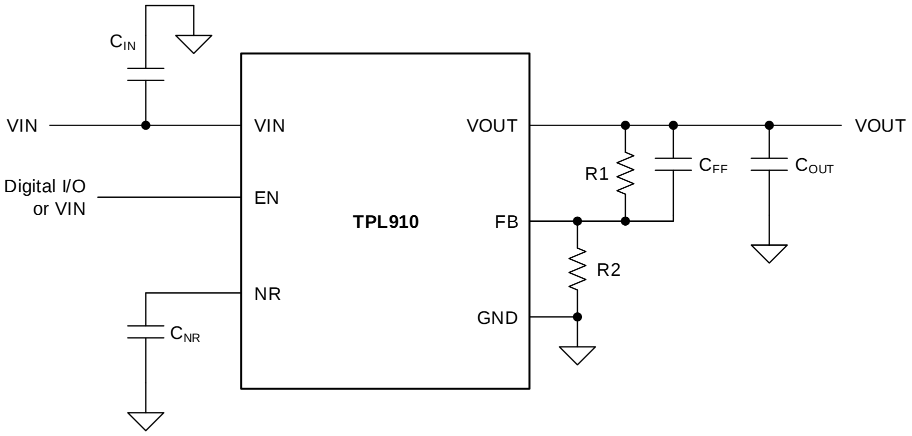


Figure 12 Adjustable Output Operation

Input Capacitor and Output Capacitor

The TPL910 series is designed to be stable with low equivalent series resistance (ESR) ceramic capacitors at the input, output, and noise-reduction pin (NR/SS). It is recommended to use ceramic capacitors with X7R-, X5R-, and COG-rated dielectric materials to get good capacitive stability across temperature.

3PEAK recommends adding a 10 μF or greater capacitor with a 0.1 μF bypass capacitor in parallel at IN pin to keep the input voltage stable. The voltage rating of the capacitors must be greater than the maximum input voltage.

To ensure loop stability, the TPL910 series requires an output capacitor with a minimum effective capacitance value of 3.3 μF. 3PEAK recommends selecting a X7R-type 10-μF ceramic capacitor with low ESR over temperature.

Both input capacitors and output capacitors must be placed as close to the device pins as possible.

Power Dissipation

During normal operation, LDO junction temperature should not exceed 125°C. Using below equations to calculate the power dissipation and estimate the junction temperature.

The power dissipation can be calculated using Equation 2.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (2)$$

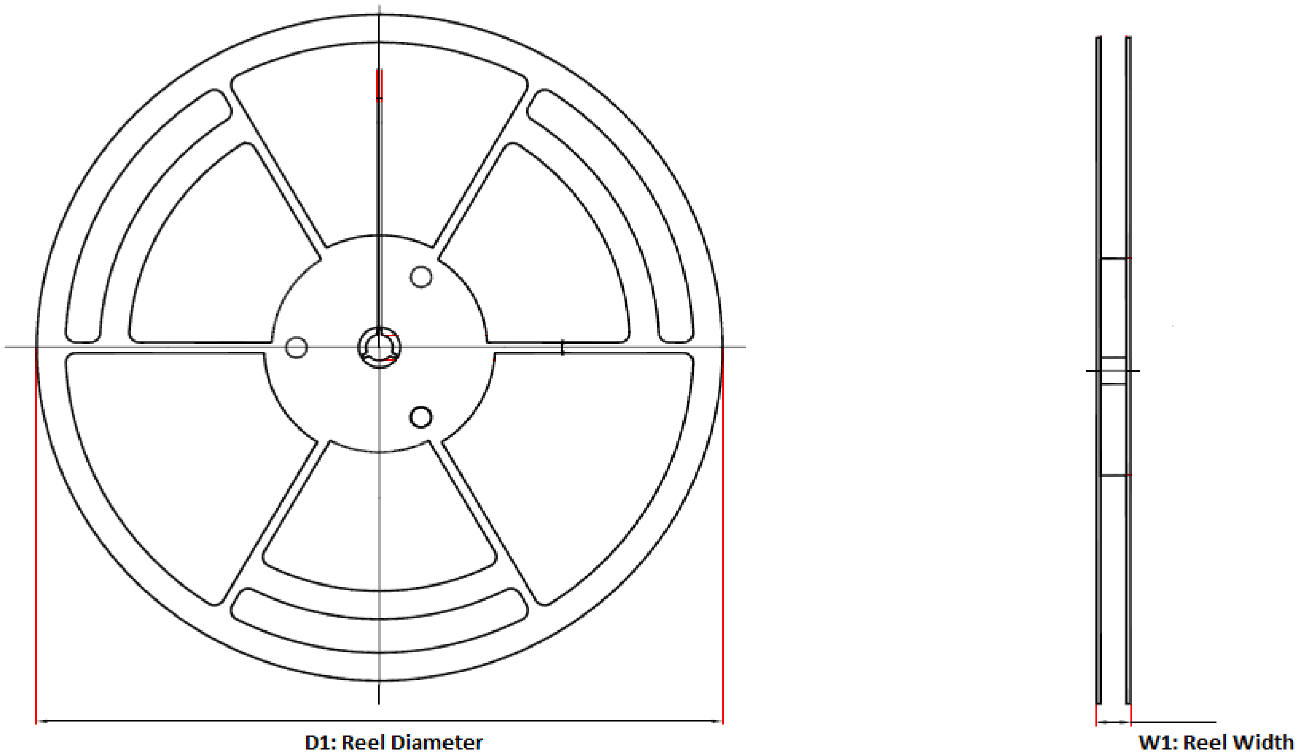
The junction temperature can be estimated using Equation 3. θ_{JA} is the junction-to-ambient thermal resistance.

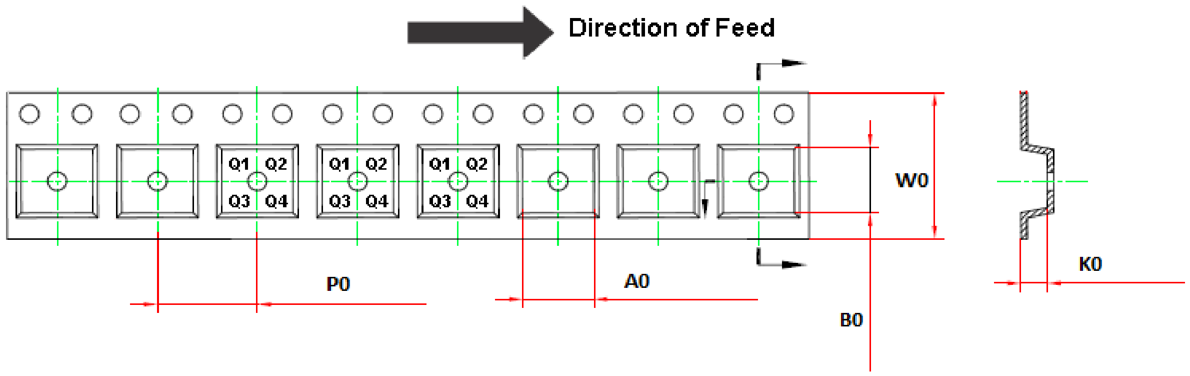
$$T_J = T_A + P_D \times \theta_{JA} \quad (3)$$

Layout Requirements

- Both input capacitors and output capacitors must be placed as close to the device pins as possible, and vias between capacitors and device power pins must be avoid.
- It is recommended to bypass the input pin to ground with a 0.1 μF bypass capacitor. The loop area formed by the bypass capacitor connection, IN pin and the GND pin of the system must be as small as possible.
- It is recommended to use wide trace lengths or thick copper weight to minimize I×R drop and heat dissipation.

Tape and Reel Information

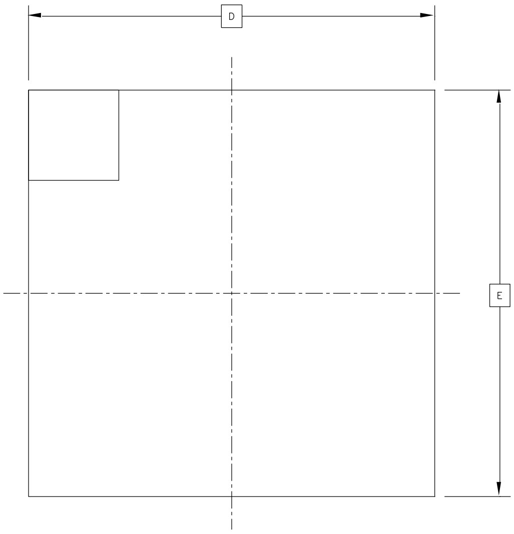




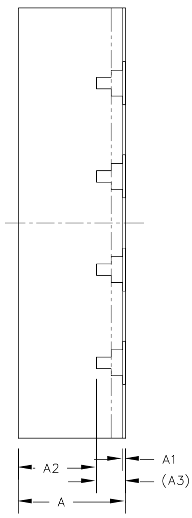
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPL910ADJ-DF6R	3×3 DFN-8	330.0	17.6	3.4	3.4	1.1	8.0	12.0	Q2

Package Outline Dimensions

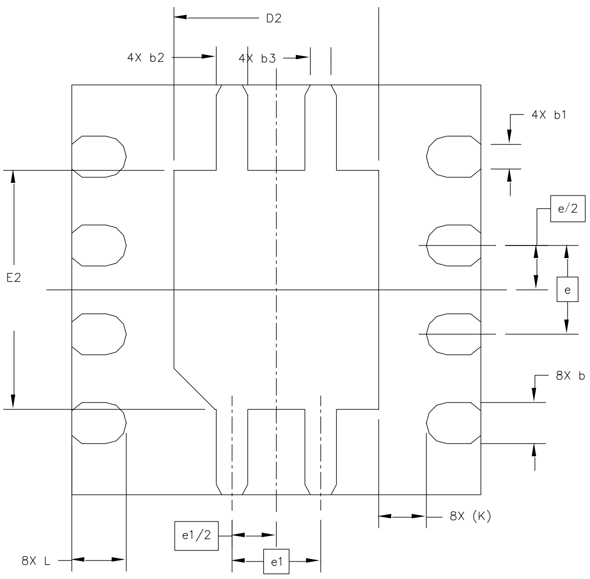
3×3 DFN-8



Top View



Side View



Bottom View

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.25	0.3	0.35
		b1		0.18 REF	
		b2	0.18	0.23	0.28
		b3		0.15 REF	
BODY SIZE	X	D		3 BSC	
	Y	E		3 BSC	
LEAD PITCH		e		0.65 BSC	
		e1		0.65 BSC	
EP SIZE	X	D2	1.4	1.5	1.6
	Y	E2	1.65	1.75	1.85
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.35 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
LEAD OFFSET		bbb		0.1	
		ddd		0.05	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.05	
EXPOSED PAD OFFSET		fff		0.1	

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