Quad Output PolyPhase Step-Down DC/DC Voltage Mode Controller with Digital Power System Management

FEATURES

- **PMBus/I²C Compliant Serial Interface**
  - **Monitor Voltage, Current, Temperature and Faults**
  - **Program Voltage, Soft-Start/Stop, Sequencing, Margining, AVP and UV/OV/OC Limits**
- **3V ≤ VINSNS ≤ 38V, 0.1V (Limited by DrMOS t_{ON_MIN}) ≤ V_{OUT} ≤ 5.25V**
- **±0.5% Output Voltage Error**
- **Programmable PWM Frequency or External Clock Synchronization from 250kHz to 2.5MHz**
- **Accurate PolyPhase® Current Sharing**
- **Internal EEPROM with Fault Logging and ECC**
- IC Supply Range: 3V to 13.2V
- Resistor or Inductor DCR Current Sensing
- Power Good Output Voltage Monitor
- Supports Start-Up Into a Prebiased Load
- Optional Resistor Programming for Key Parameters
- 99-Lead BGA Package (9mm × 7.5mm)

APPLICATIONS

- High Current Distributed Power Systems
- Servers, Network and Storage Equipment
- Intelligent Energy Efficient Power Regulation

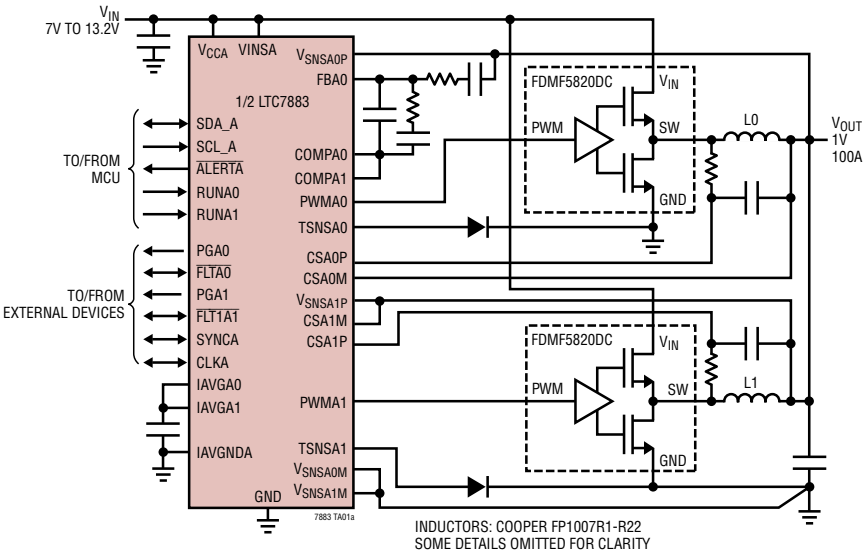
DESCRIPTION

The LTC®7883 is a quad, PolyPhase DC/DC synchronous step-down switching regulator controller with PMBus compliant serial interface. It uses a constant frequency, leading-edge modulation, voltage mode architecture for excellent transient response and output regulation. Each PWM channel can produce output voltages from 0.1V to 5.25V using a wide range of 3.3V compatible power stages, including power blocks, DrMOS or discrete FET drivers. LTC7883 devices can operate in parallel, supporting ideal phasor positioning for PolyPhase rails up to 8 phases.

System configuration and monitoring is supported by the LTpowerPlay® software tool. The LTC7883 serial interfaces can read back input voltage, output voltage and current, temperature and fault status. Most operating parameters can be set via the digital interfaces or stored in internal EEPROM for use at power-up. Switching frequency and phase, output voltage and device address can also be set using external configuration resistors.

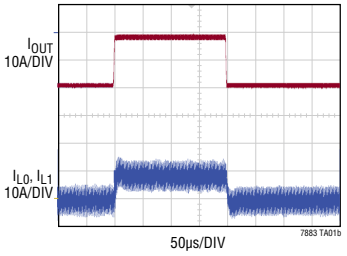
Note: ADI does not recommend using the following PWM frequencies in new designs: 600kHz, 750kHz, 900kHz, and 1MHz.

TYPICAL APPLICATION



INDUCTORS: COOPER FP1007R1-R22
SOME DETAILS OMITTED FOR CLARITY

Load Step Transient Current Sharing (Using FDMF5820DC DrMOS)



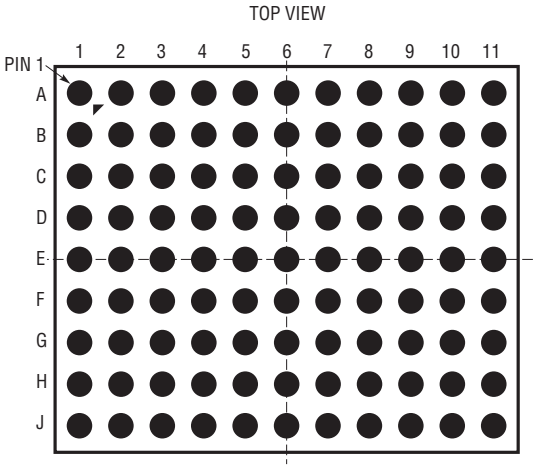
ABSOLUTE MAXIMUM RATINGS

(Note 1)

$V_{CC[A/B]}$ Supply ..... –0.3V to 15V
VINS[A/B] ..... –0.3V to 40V
$V_{SNS[A/B][1:0]M}$ ..... –0.3V to 1V
$V_{SNS[A/B][1:0]P}$, CS[A/B][1:0]P/M ..... –0.3V to 6V
FB[A/B][1:0], COMP[A/B][1:0],
TSNS[A/B][1:0], IAVGND[A/B],
IAVG[A/B][1:0] ..... –0.3V to 3.6V
SYNC[A/B], $\overline{FLT}$[A/B][1:0], WP[A/B],
PG[A/B][1:0], SHCLK[A/B] ..... –0.3V to 3.6V
SCL[A/B], SDA[A/B], RUN[A/B][1:0],
$\overline{ALERT}$[A/B] ..... –0.3V to 5.5V
ASEL0[A/B], ASEL1[A/B],
VO[A/B][1:0]CFG, FCFG[A/B],
PCFG[A/B] ..... –0.3V to 2.75V
PWM[A/B][1:0], $V_{DD25[A/B]}$ ..... (Note 13)
$V_{DD33[A/B]}$ ..... (Note 14)
Operating Junction Temperature
(Notes 2, 3) ..... –40°C to 125°C*
Storage Temperature Range ..... –65°C to 150°C*
Absolute Maximum Junction Temperature ..... 125°C

*See Derating EEPROM Retention at Temperature in the Applications Information section for junction temperatures in excess of 125°C.

PIN CONFIGURATION



BGA PACKAGE
99-LEAD (9mm × 7.5mm × 1.29mm)
T_{JMAX} = 125°C, θ_{JA} = 32°C/W,
θ_{JCtop} = 17°C/W, $\theta_{JCbottom}$ = 12.1°C/W, θ_{JB} = 14.5°C/W,
WEIGHT = **TBD**g,
θ VALUES DETERMINED PER JEDEC 51-9, 51-12

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	OPERATING JUNCTION TEMPERATURE RANGE
		DEVICE	FINISH CODE			
LTC7883AY#PBF	SAC305 (RoHS)	LTC7883Y	e1	BGA	3	–40°C to 125°C

- Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
- Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_J = 25°C (Note 2). Specifications apply to both units with V_{CC} = 5V, V_{SNSP} = 1.8V, V_{SNSM} = IAVGND = GND = 0V, f_{SYNC} = 500kHz (externally driven) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IC Supply							
V_{CC}	V_{CC} Voltage Range	V_{DD33} = Internal LDO		4.5		13.8	V
V_{DD33_EXT}	V_{DD33} Voltage Range	V_{CC} = V_{DD33} (Note 6)	●	3		3.6	V
V_{UVLO}	Undervoltage Lockout Threshold	V_{DD33} Rising Hysteresis	●		 42	3	V mV
I_Q	IC Operating Current	per Unit			32		mA
t_{INIT}	Controller Initialization Time	Delay from RESTORE_USER_ALL, MFR_RESET or V_{DD33} > V_{UVLO} Until TON_DELAY Can Begin			35		ms
V_{DD33} Linear Regulators							
V_{DD33}	V_{DD33} Regulator Output Voltage	V_{CC} ≥ 4.5V		3.2	3.3	3.4	V
I_{DD33}	V_{DD33} Current Limit	V_{DD33} = 2.8V V_{DD33} = 0V			85 40		mA mA
V_{DD25} Linear Regulators							
V_{DD25}	V_{DD25} Regulator Output Voltage			2.25	2.5	2.75	V
I_{DD25}	V_{DD25} Current Limit				95		mA
PWM Control Loops							
VINS	V_{IN} Sense Voltage Range			3		38	V
R_{VINS}	VINS Input Resistance				278		kΩ
V_{OUT_R0}	Range 0 Maximum V_{OUT} Range 0 Set Point Error (Note 7) Range 0 Set Point Resolution	0.6V ≤ V_{OUT} ≤ 5V	 ● 	 –0.5 	5.25 1.375	 0.5 	V % mV
V_{OUT_R1}	Range 1 Maximum V_{OUT} Range 1 Set Point Error (Note 7) Range 1 Set Point Resolution	0.6V ≤ V_{OUT} ≤ 2.5V	 ●	 –0.5 	2.65 0.6875	 0.5 	V % mV
I_{VSNS}	V_{SNS} Input Current	V_{SNSP} = 5.5V V_{SNSM} = 0V			235 –335		µA µA
$V_{LINEREG}$	V_{CC} Line Regulation, No Output Servo	4.5V ≤ V_{CC} ≤ 13.2V (See Test Circuit)		–0.02		0.02	%/V
AVP	AVP ΔV_{OUT}	AVP = 10%, VOUT_COMMAND = 1.8V, CS Differential Step 3mV to 12mV with IOUT_OC_WARN_LIMIT = 15mV		–118	–108	–96	mV
$A_{V(OL)}$	Error Amplifier Open-Loop Voltage Gain				87		dB
SR	Error Amplifier Slew Rate				9.5		V/µs
f_{0dB}	Error Amplifier Bandwidth	(Note 12)			30		MHz
I_{COMP}	Error Amplifier Output Current	Sourcing Sinking			–2.6 34		mA mA
R_{VSFB}	Resistance Between V_{SNSP} and FB	Range 0 Range 1	● ●	52 37	67 49	83 61	kΩ kΩ
V_{ISENSE}	CS Differential Input Range				±70		mV
I_{ISENSE}	CSP/M Input Current	0V ≤ V_{PIN} ≤ 5.5V		–1	±0.1	1	µA
I_{AVG_VOS}	IAVG Current Sense Offset	Referred to CS Inputs		 –600	±175 	 650	µV µV
V_{SIOS}	Slave Current Sharing Offset	Referred to CS Inputs		 –800	±300 	 700	µV µV
f_{SYNC}	SYNC Frequency Error	250kHz ≤ f_{SYNC} ≤ 1.25MHz	●	–10		10	%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at TJ = 25°C (Note 2). Specifications apply to both units with V_{CC} = 5V, V_{SNSP} = 1.8V, V_{SNSM} = IAVGND = GND = 0V, f_{SYNC} = 500kHz (externally driven) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Supervisor							
V_{ON_TOL}	Input ON/OFF Threshold Error	15V ≤ V_{IN_ON} ≤ 35V	●	–2		2	%
N_{VON}	Input ON/OFF Threshold Resolution				143		mV
Output Voltage Supervisors							
V_{UVOV_R0}	Range 0 Maximum Threshold Range 0 Error Range 0 Threshold Resolution Range 0 Threshold Hysteresis	2V ≤ V_{OUT} ≤ 5V (Falling for UV and Rising for OV)	 ● 	 –1 	5.5 11 50	 1 	V % mV mV
V_{UVOV_R1}	Range 1 Maximum Threshold Range 1 Error Range 1 Threshold Resolution Range 1 Threshold Hysteresis	1V ≤ V_{OUT} ≤ 2.5V (Falling for UV and Rising for OV)	 ● 	 –1 	2.75 5.5 25	 1 	V % mV mV
Output Current Supervisors							
V_{ILIM_TOL}	Output Current Limit Tolerance CSP – CSM	15mV < CSP – CSM ≤ 30mV 30mV < CSP – CSM ≤ 50mV 50mV < CSP – CSM ≤ 70mV	● ● ●	–1.7 –2.5 –5.2		1.7 2.5 5.2	mV mV mV
N_{ILIM}	CSP – CSM Threshold Resolution	1LSB			0.4		mV
ADC Readback Telemetry (Note 8)							
N_{VIN}	VINS Readback Resolution	(Note 9)			10		Bits
V_{IN_TUE}	VINS Total Unadjusted Readback Error	4.5V ≤ VINS ≤ 38V	 ●			0.5 2	% %
N_{DC}	PWM Duty Cycle Resolution	(Note 9)			10		Bits
DC_{TUE}	PWM Duty Cycle Total Unadjusted Readback Error	PWM Duty Cycle = 12.5%		–2		2	%
N_{VOUT}	V_{OUT} Readback Resolution				244		µV
V_{OUT_TUE}	V_{OUT} Total Unadjusted Readback Error	0.6V ≤ V_{OUT} ≤ 5.5V, Constant Load	 ●	 –0.5	±0.2	 0.5	% %
N_{ISENSE}	I_{OUT} Readback Resolution LSB Step Size (at $I_{SENSE}^{\pm}$)	(Note 9) 0mV ≤ |CSP – CSM| < 16mV 16mV ≤ |CSP – CSM| < 32mV 32mV ≤ |CSP – CSM| < 63.9mV 63.9mV ≤ |CSP – CSM| ≤ 70mV			10 15.625 31.25 62.5 125		Bits µV µV µV µV
I_{SENSE_TUE}	I_{OUT} Total Unadjusted Readback Error	|CSP – CSM| ≥ 6mV, 0V ≤ V_{OUT} ≤ 5.5V	●		±1		%
I_{SENSE_OS}	I_{OUT} Zero-Code Offset Voltage				±32		µV
N_{TEMP}	Temperature Resolution				0.25		°C
T_{EXT_TUE}	External Temperature Total Unadjusted Readback Error	TSNS ≤ 1.85V (Note 10) MFR_PWM_MODE_LTC3882-1[6] = 0 MFR_PWM_MODE_LTC3882-1[6] = 1	 ● ●	 –3 –7		 3 7	 °C °C
T_{INT_TUE}	Internal Temperature Total Unadjusted Readback Error	Internal Diode (Note 10)			±1		°C
$t_{CONVERT}$	Update Rate	(Note 11)			90		ms
Internal EEPROM (Notes 4, 6)							
Endurance	Number of Write Operations	0°C ≤ T_J ≤ 85°C During All Write Operations		10,000			Cycles
Retention	Stored Data Retention	T_J ≤ 125°C		10			Years
Mass Write Time	STORE_USER_ALL Execution Duration	0°C ≤ T_J ≤ 85°C During All Write Operations			0.2	2	s

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at TJ = 25°C (Note 2). Specifications apply to both units with V_{CC} = 5V, V_{SNSP} = 1.8V, V_{SNSM} = IAVGND = 0V, f_{SYNC} = 500kHz (externally driven) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Inputs (SCL, SDA, RUN, $\overline{FLT}$, SYNC, SHCLK, WP)							
V_{IH}	Input High Voltage	SCL, SDA, RUN, $\overline{FLT}$ SYNC, SHCLK, WP	● ●	1.35 1.8			V V
V_{IL}	Input Low Voltage	SCL, SDA, RUN, $\overline{FLT}$ SYNC, SHCLK, WP	● ●			0.8 0.6	V V
V_{HYST}	Input Hysteresis	SCL, SDA			80		mV
I_{LKG}	Input Pull-Up Current	WP = 0V			10		µA
C_{IN}	Input Capacitance	SCL, SDA, RUN, $\overline{FLT}$, SYNC, SHCLK (Note 12)				10	pF
t_{FILT}	Input Digital Filter Delay	$\overline{FLT}$ RUN			3 10		µs µs
Digital Outputs (SCL, SDA, RUN, $\overline{FLT}$, SYNC, SHCLK, $\overline{ALERT}$, PWM, PG)							
V_{OL}	Output Low Voltage	I_{SINK} = 3mA; SCL, SDA, RUN, $\overline{FLT}$, SYNC, SHCLK, $\overline{ALERT}$ I_{SINK} = 2mA; PWM, PG	● ●		0.2	0.4 0.3	V V
V_{OH}	PWM Output High Voltage	I_{SOURCE} = 2mA	●	2.7			V
I_{LKG}	Output Leakage Current	0V ≤ PWM, PG ≤ V_{DD33} 0V ≤ $\overline{FLT}$, SYNC, SHCLK ≤ 3.6V 0V ≤ RUN ≤ 5.5V 0V ≤ SCL, SDA, $\overline{ALERT}$ ≤ 5.5V	 ●	 –1 –5 –5		 1 5 5	µA µA µA
t_{RO}	PWM Output Rise Time	C_{LOAD} = 30pF, 10% to 90%			5		ns
t_{FO}	PWM Output Fall Time	C_{LOAD} = 30pF, 90% to 10%			4		ns
Serial Bus Timing							
f_{SMB}	Serial Bus Operating Frequency		●	10		400	kHz
t_{BUF}	Bus Free Time Between Stop and Start		●	1.3			µs
$t_{HD,STA}$	Hold Time After (Repeated) Start Condition. After This Period, the First Clock Is Generated		●	0.6			µs
$t_{SU,STA}$	Repeated Start Condition Setup Time		●	0.6			µs
$t_{SU,STO}$	Stop Condition Setup Time		●	0.6			µs
$t_{HD,DAT}$	Data Hold Time: Receiving Data Transmitting Data		 ● ●	 0 0.3		 0.9	 ns µs
$t_{SU,DAT}$	Input Data Setup Time		●	100			ns
$t_{TIMEOUT}$	Clock Low Timeout		●	25		35	ms
t_{LOW}	Serial Clock Low Period		●	1.3		10000	µs
t_{HIGH}	Serial Clock High Period		●	0.6			µs

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC7883 is specified over the –40°C to 125°C operating junction temperature range. High Junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Note 4: EEPROM endurance, retention and mass write times are guaranteed by design, characterization and correlation with statistical process controls. Minimum retention applies only for devices cycled less than the minimum endurance specification. EEPROM read commands (e.g. RESTORE_USER_ALL) are valid over the entire specified operating junction temperature range.

Note 5: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified.

Note 6: Minimum EEPROM endurance, retention and mass write time specifications apply when writing data with $3.15V \le V_{DD33} \le 3.45V$. EEPROM read commands are valid over the entire specified V_{DD33} operating range.

Note 7: Specified V_{OUT} error with AVP = 0% requires servo mode to be set with MFR_PWM_MODE_LTC3882-1 command bit 6. Performance is guaranteed by testing the LTC7883 in a feedback loop that servos V_{OUT} to a specified value.

Note 8: ADC tested with PWMs disabled. Comparable capability demonstrated by in-circuit evaluations. Total Unadjusted Error includes all gain and linearity errors, as well as offsets.

Note 9: Internal 32-bit calculations using 16-bit ADC results are limited to 10-bit resolution by PMBus Linear 11-bit data format.

Note 10: Limits guaranteed by TSNS voltage and current measurements during test, including ADC readback.

Note 11: Data conversion is done in round robin fashion. All inputs signals are continuously scanned in sequence resulting in a typical conversion latency of 90ms.

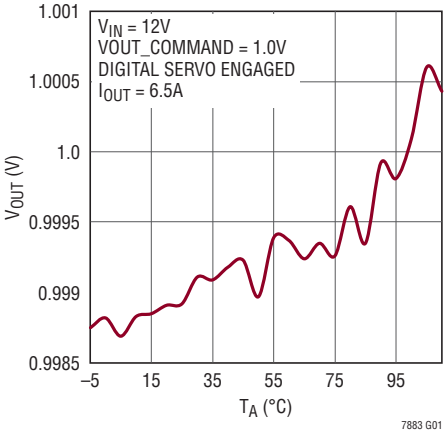
Note 12: Guaranteed by design.

Note 13: Do not apply a voltage or current source directly to these pins. They should only be connected to passive RC loads, otherwise permanent damage may occur.

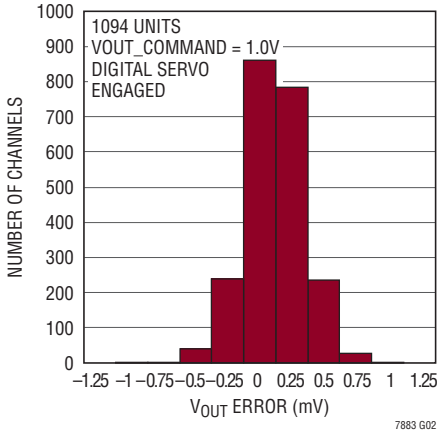
Note 14: Do not apply a voltage source to this pin unless shorted to V_{CC}. See Electrical Characteristics for applicable limits beyond which permanent damage may occur.

TYPICAL PERFORMANCE CHARACTERISTICS

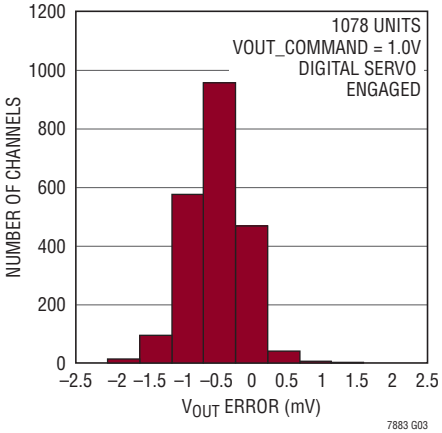
LTC7883 1.0V Regulated Output vs Temperature



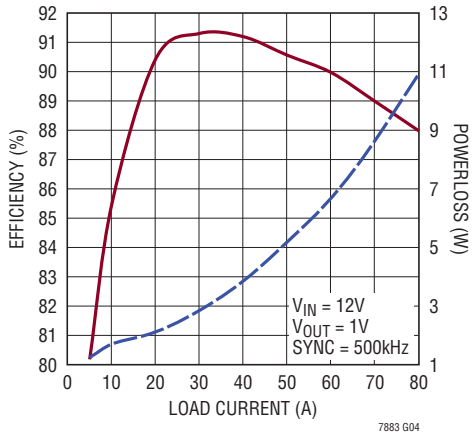
Typical LTC7883 Output Voltage Distribution at 0°C



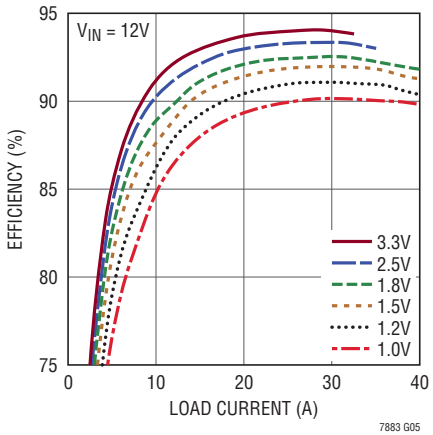
Typical LTC78883 Output Voltage Distribution at 105°C



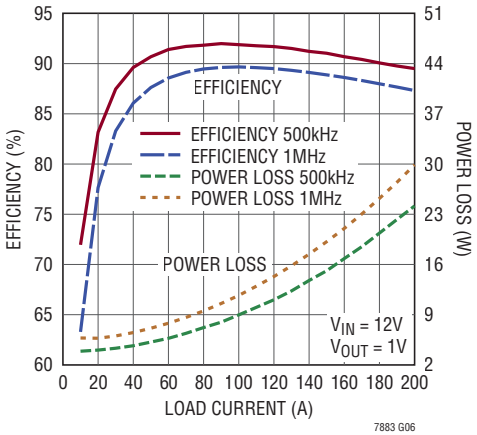
Efficiency and Loss vs Load (2-Phase Using FDMF5820DC DrMOS)



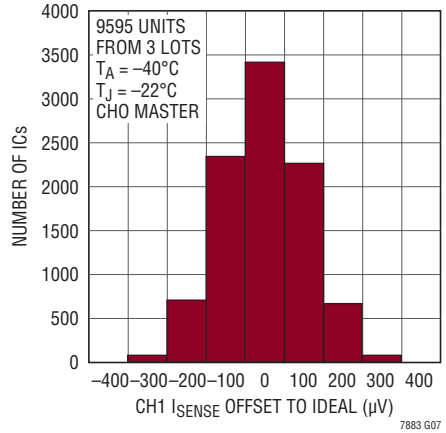
Efficiency vs Load Current (1-Phase Using D12S1R880A Power Block)



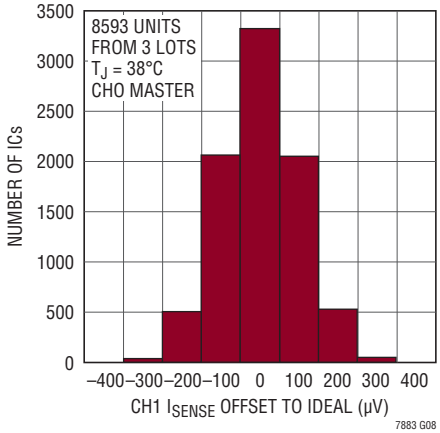
Efficiency and Loss vs Load (4-Phase Using LTC7051)



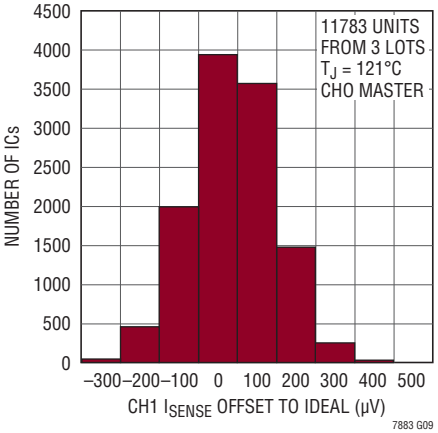
Typical Distribution of Slave I_{OUT} Offset (Not Including DCR Mismatch)



Typical Distribution of Slave I_{OUT} Offset (Not Including DCR Mismatch)

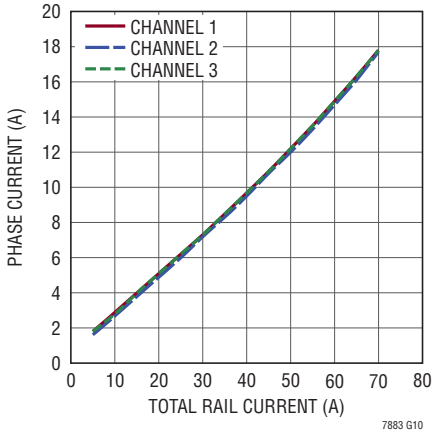


Typical Distribution of Slave I_{OUT} Offset (Not Including DCR Mismatch)

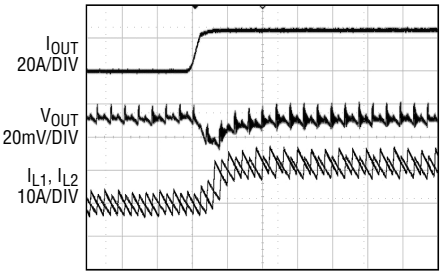


TYPICAL PERFORMANCE CHARACTERISTICS

3-Phase DC Output Current Sharing (Using D12S1R845A Power Block

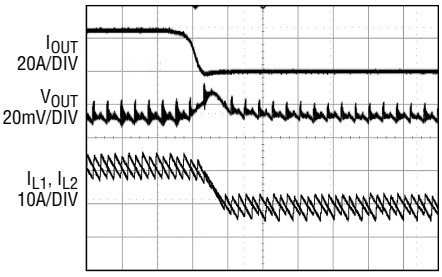


Load Step Transient Current Sharing (Using FDMF6707B DrMOS)



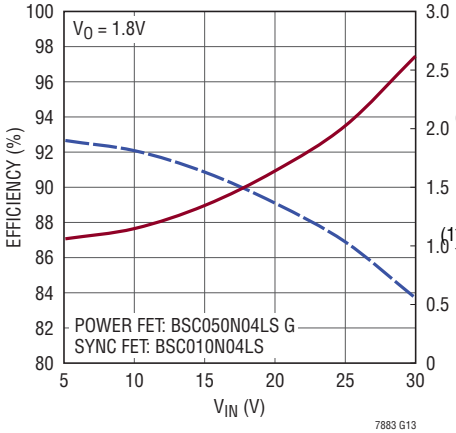
V_{OUT} = 1V
V_{IN} = 12V
SYNC = 500kHz
L = 320nH

Load Dump Transient Current Sharing (Using FDMF6707B DrMOS)

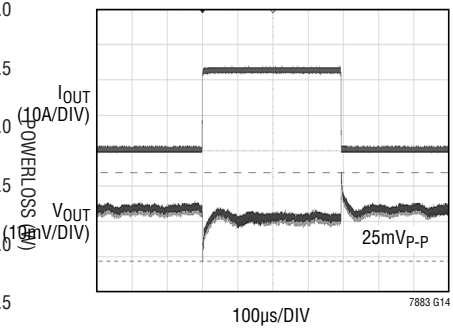


V_{OUT} = 1V
V_{IN} = 12V
SYNC = 500kHz
L = 320nH

Efficiency and Power Loss vs Input Voltage (1-Phase Using LTC4449)

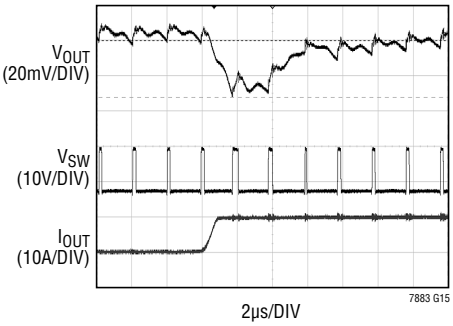


3-Phase Transient Response (Using D12S1R860A Power Block)



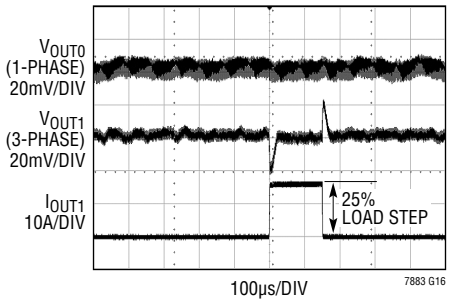
V_{OUT} = 0.9V/90A
V_{IN} = 12V
SYNC = 500kHz
L = 210nH

1-Phase Single Cycle Response (Using D12S1R860A Power Block with C_{OUT} = 6 × 100µF X5R 1210)

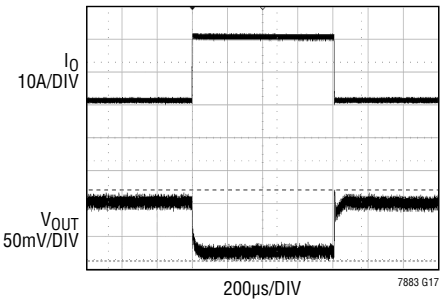


V_{OUT} = 1V/25A
V_{IN} = 12V
SYNC = 1MHz
L = 210nH

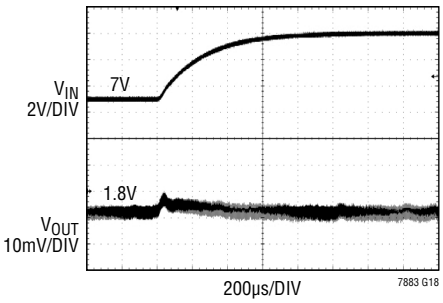
3+1 Channel Crosstalk (Using D12S1R845A Power Blocks)



Load Step Transient Response Using AVP

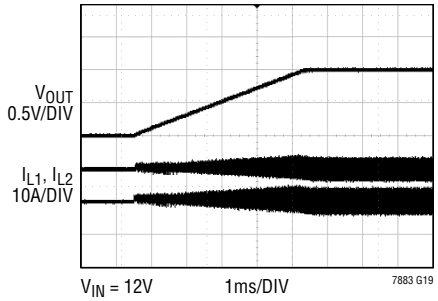


Line Step Transient Response (1-Phase Using LTC4449)

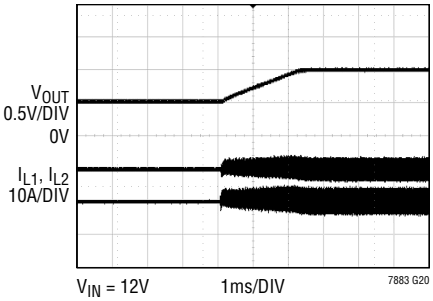


TYPICAL PERFORMANCE CHARACTERISTICS

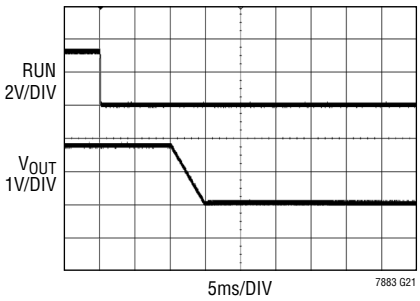
Soft-Start Ramp



Start-Up Into a Prebiased Load

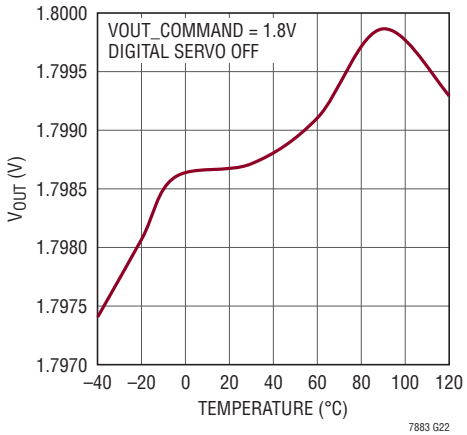


Soft-Off Ramp

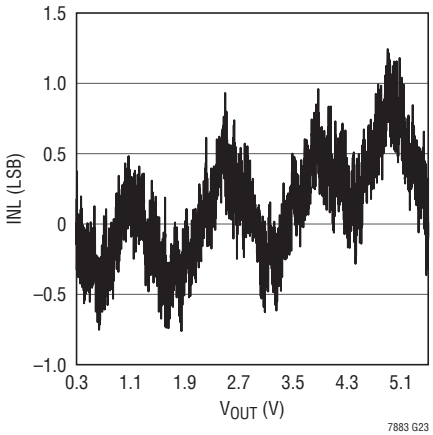


TOFF_DELAY = 10ms
TOFF_FALL = 5ms

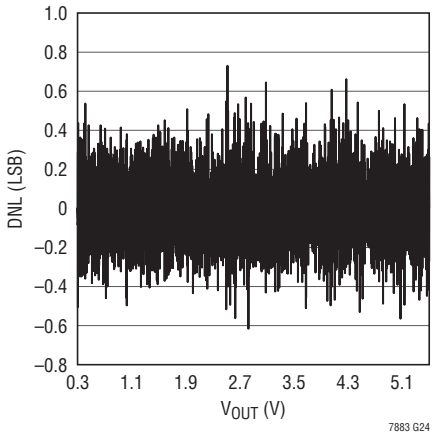
Regulated Output vs Temperature



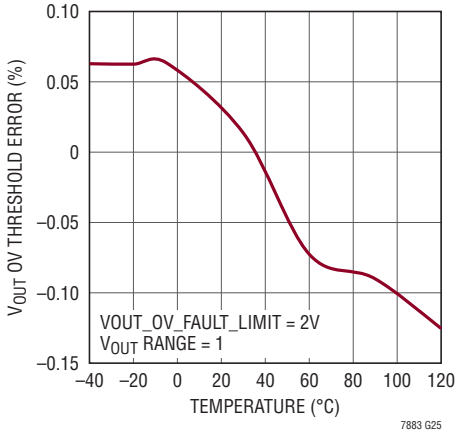
VOUT_COMMAND INL



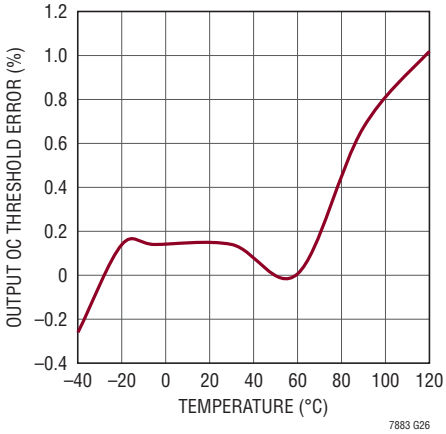
VOUT_COMMAND DNL



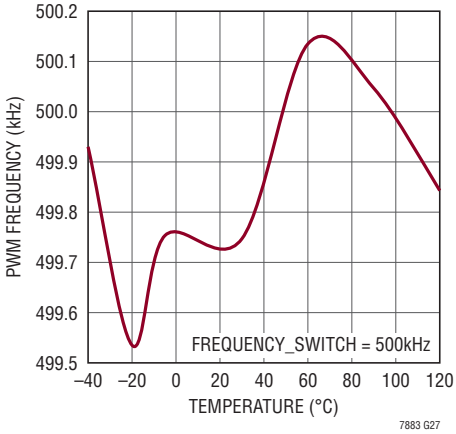
Output Overvoltage Threshold Error vs Temperature



Output Overcurrent Threshold Error vs Temperature

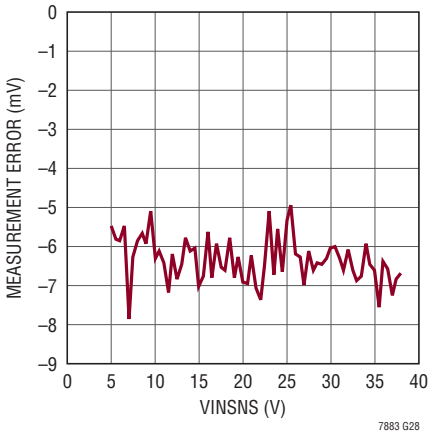


PWM Frequency vs Temperature

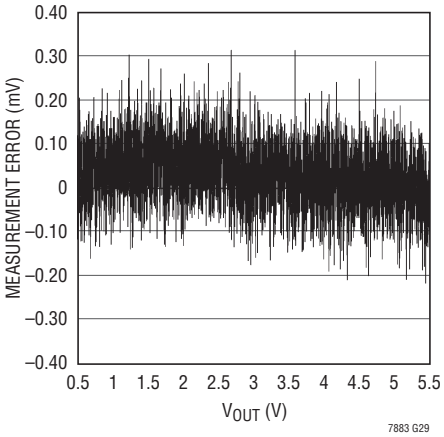


TYPICAL PERFORMANCE CHARACTERISTICS

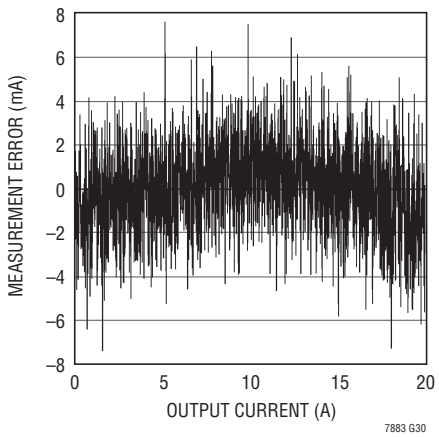
VINS ADC TUE



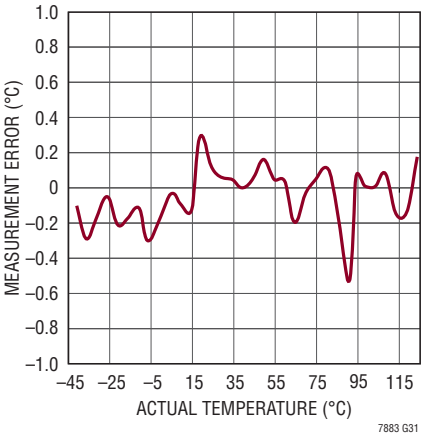
V_{OUT} ADC TUE



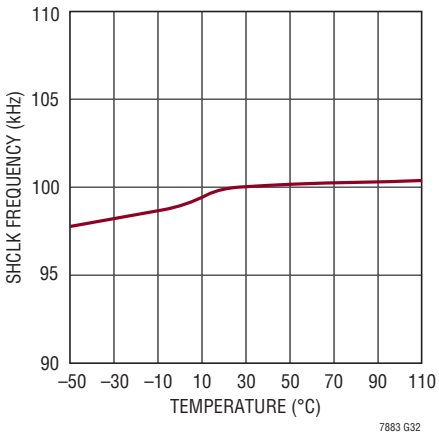
I_{OUT} ADC TUE



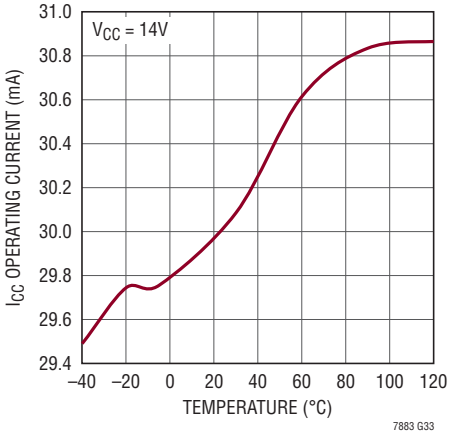
Temperature ADC TUE



SHCLK Frequency vs Temperature



IC Operating Current vs Temperature



LTC7883 PIN (BALL) ASSIGNMENTS

BALL	PIN NAME	
	UNIT A	UNIT B
A1	V_{SNSA1P}	
A2	V_{SNSA1M}	
A3	V_{SNSA0M}	
A4	V_{SNSA0P}	
A5	$\overline{ALERTA}$	
A6	V_{CCA}	
A7		$\overline{ALERTB}$
A8		V_{SNSB1P}
A9		V_{SNSB1M}
A10		V_{SNSB0M}
A11		V_{SNSB0P}
B1	ASELA1	
B2	ASELA0	
B3		ASELB1
B4		ASELB0
B5	GND	GND
B6		V_{CCB}
B7	GND	GND
B8	RUNA0	
B9	RUNA1	
B10		RUNB0
B11		RUNB1
C1	SDA_A	
C2		SDA_B
C3	GND	GND
C4	PCFGA	
C5	FCFGA	
C6	GND	GND
C7		PCFGB
C8		VOB1CFG
C9	GND	GND
C10	SCL_A	
C11		SCL_B
D1	$\overline{FLTA1}$	
D2	$\overline{FLTA0}$	
D3		$\overline{FLTB1}$
D4		$\overline{FLTB0}$
D5	VOA0CFG	
D6	GND	GND
D7		FCFGB
D8		VOB0CFG
D9	GND	GND
D10	SYNCA	
D11		SYNCB
E1	IAVGNDA	
E2	V_{DD25A}	
E3	VOA1CFG	
E4	GND	GND
E5	GND	GND
E6	GND	GND
E7	GND	GND

BALL	PIN NAME	
	UNIT A	UNIT B
E6	GND	GND
E7	GND	GND
E8	GND	GND
E9	GND	GND
E10		V_{DD25B}
E11		IAVGNDB
F1	COMPA1	
F2	FBA1	
F3	V_{DD33A}	
F4	SHCLKA	
F5		SHCLKB
F6	GND	GND
F7	WPA	
F8		WPB
F9		V_{DD33B}
F10		FBB0
F11		COMPB0
G1	COMPA0	
G2	FBA0	
G3	PGA0	
G4	PGA1	
G5	GND	GND
G6	GND	GND
G7		PGB0
G8		PGB1
G9		FBB1
G10		COMPB1
G11		COMPB1
H1	CSA1M	
H2	IAVGA0	
H3	IAVGA1	
H4	TSNSA1	
H5	TSNSA0	
H6	VINSA	
H7		IAVGB0
H8		IAVGB1
H9		TSNSB1
H10		TSNSB0
H11		PWMB0
J1	CSA1P	
J2	PWMA1	
J3	CSA0M	
J4	CSA0P	
J5	PWMA0	
J6		VINSB
J7		CSB1M
J8		CSB1P
J9		PWMB1
J10		CSB0M
J11		CSB0P

PIN FUNCTIONS

COMP[A/B][1:0]: Error Amplifier Outputs. PWM duty cycle increases with this control voltage. These are true low impedance outputs and cannot be directly connected together when active. For PolyPhase operation, wiring FB to V_{DD33} will three-state the error amplifier output of that channel, making it a slave. PolyPhase control is then implemented in part by connecting all slave COMP pins together to one master error amplifier output.

TSNS[A/B][1:0]: External Temperature Sense Inputs. The LTC7883 supports two methods of calculation of external temperature based on forward-biased P/N junctions between these pins and GND.

VINS[A/B]: V_{IN} Supply Sense. Connect to the V_{IN} power supply to provide line feedforward compensation. A change in V_{IN} immediately modulates the input to the PWM comparator and inversely changes the pulse width to provide excellent transient line regulation and fixed modulator voltage gain. An external lowpass filter can be added to this pin to prevent noisy signals from affecting the loop gain.

IAVGND[A/B]: IAVG Ground Reference. The same IAVGND should be shared between all channels of a PolyPhase rail and connected to system ground at a single point. IAVGND may be wired directly to GND on units that do not share phases with other units.

PG[A/B][1:0]: Power Good Indicator Open-Drain Outputs. These outputs are driven low through a 30µs filter when the respective channel output is below its programmed UV fault limit or above its programmed OV fault limit. If used, a pull-up resistor is required in the application. Operating voltage range is GND to V_{DD33}.

PWM[A/B][1:0]: PWM Three-State Control Outputs. These pins provide single-wire PWM switching control for each channel to an external gate driver, DrMOS or power block. Operating voltage range is GND to V_{DD33}.

SYNC[A/B]: External Clock Synchronization Input and Open-Drain Output. If desired, an external clock can be applied to this pin to synchronize the internal PWM channels. If an LTC7883 unit is configured as a clock master, this pin will also pull to ground at the selected PWM switching frequency with a 125ns pulse width. A pull-up resistor to 3.3V is required in the application if SYNC is driven by any LTC7883. Minimize the capacitance on this line to ensure its time constant is fast enough for the application.

SCL[A/B]: Serial Bus Clock Input. A pull-up resistor to 3.3V is required in the application.

SDA[A/B]: Serial Bus Data Input and Output. A pull-up resistor to 3.3V is required in the application.

$\overline{\text{ALERT}}$[A/B]: Open-Drain Status Output. This pin may be connected to the system $\overline{\text{SMBALERT}}$ wire-AND interrupt signal and should be left open if not used. If used, a pull-up resistor is required in the application. Operating voltage range is GND to V_{DD33}.

$\overline{\text{FLT}}$[A/B][1:0]: Programmable Digital Inputs and Open-Drain Outputs for Fault Sharing. Used for channel-to-channel fault communication and propagation. These pins should be left open if not used. If used, a pull-up resistor to 3.3V is required in the application.

RUN[A/B][1:0]: Run Control Inputs and Open-Drain Outputs. A voltage above 2V is required on these pins to enable the respective PWM channel. The LTC7883 will drive these pins low under certain reset/restart conditions regardless of any PMBus command settings. A pull-up resistor to 3.3V is required in the application.

ASELA[1:0]: Unit A Serial Bus Address Select Pins. Connect optional 1% resistor dividers between V_{DD25A} and GND to these pins to select the serial bus interface address.

ASELB[1:0]: Unit B Serial Bus Address Select Pins. Connect optional 1% resistor dividers between V_{DD25B} and GND to these pins to select the serial bus interface address.

VO[A/B][1:0]CFG: Output Voltage Configuration Pins. Connect optional 1% resistor dividers between V_{DD25} and GND to these pins to select the output voltage for each channel.

FCFG[A/B]: Frequency Configuration Pins. Connect an optional 1% resistor divider between V_{DD25} and GND to these pins to configure PWM switching frequency.

PIN FUNCTIONS

PCFG[A/B]: Phase Configuration Pins. Connect an optional 1% resistor divider between V_{DD25} and GND to these pins to configure the phase of each PWM channel relative to SYNC.

$V_{DD25[A/B]}$: Internal 2.5V Regulator Outputs. Bypass these pins to GND with a low ESR 1µF capacitor. Do not short these pins together or load them with external current beyond that required for local LTC7883 configuration.

WP[A/B]: Write Protect Inputs. If WP is above 2V, PMBus writes are restricted and any software WRITE_PROTECT settings for that unit are overridden. These pins have an internal 10µA pull-up to V_{DD33}.

SHCLK[A/B]: Share Clock Open-Drain Outputs (bussed). Share Clock, nominally 100kHz, is used to sequence multiple rails in a power system utilizing more than one ADI PSM controller. A pull-up resistor is required in the application. Minimize the capacitance on this line to ensure the time constant is fast enough for the application. Operating voltage range is GND to V_{DD33}.

$V_{DD33[A/B]}$: Internal 3.3V Regulator Outputs. Bypass these pins to GND with a low ESR 2.2µF capacitor. The LTC7883 may also be powered from an external 3.3V rail attached to these pins, if also shorted to $V_{CC[A/B]}$. Otherwise do not short these pins together or overload them with external system current. Local pull-up resistors for the LTC7883 itself may be powered from V_{DD33}.

$V_{CC[A/B]}$ (Pin 25): 3.3V Regulator Input(s). Bypass these pins, which may be shorted together, to GND with a capacitor (0.1µF to 1µF ceramic) in close proximity to the IC.

$V_{SNS[A/B][1:0]M}$: Negative Output Voltage Sense Inputs. These pins must still be properly connected on slave channels for accurate output current telemetry.

$V_{SNS[A/B][1:0]P}$: Positive Output Voltage Sense Inputs. These pins must still be properly connected on slave channels for accurate output current telemetry.

CS[A/B][1:0]M: Current Sense Amplifier Inputs. These (–) inputs to the amplifiers are normally connected to the low side of a DCR sensing network or output current sense resistor for each phase.

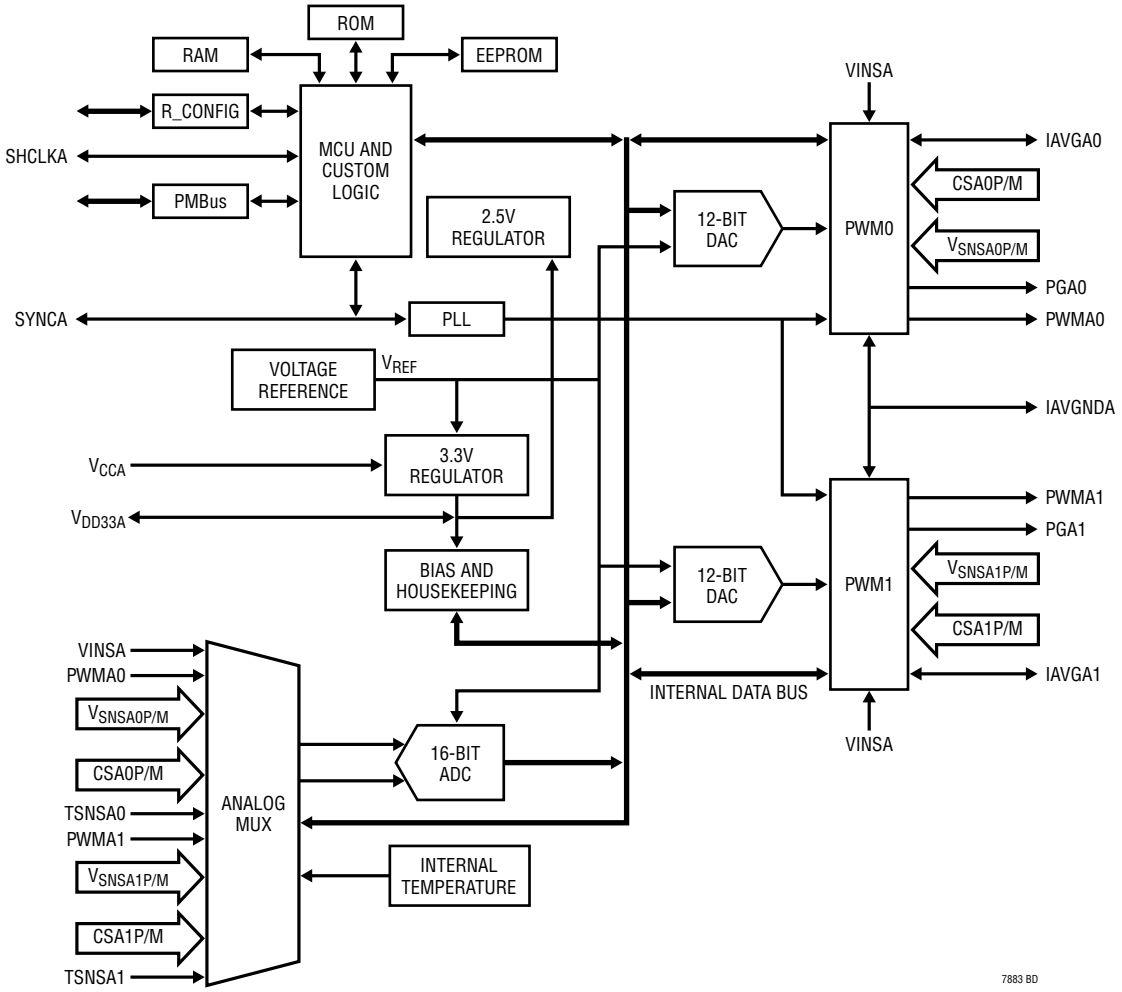
CS[A/B][1:0]P: Current Sense Amplifier Inputs. These (+) inputs are normally connected to the high side of an output current sense resistor or the R-C midpoint of a parallel DCR sense circuit for each phase.

IAVG[A/B][1:0]: Average Current Control Pins. A capacitor connected between these pins and IAVGND stores a voltage proportional to the average output current of the master channel. PolyPhase control is then implemented in part by connecting all slave IAVG pins together to the master IAVG output. This pin should be left open on channels that control single-phase outputs. Operating voltage range is GND to 2.1V.

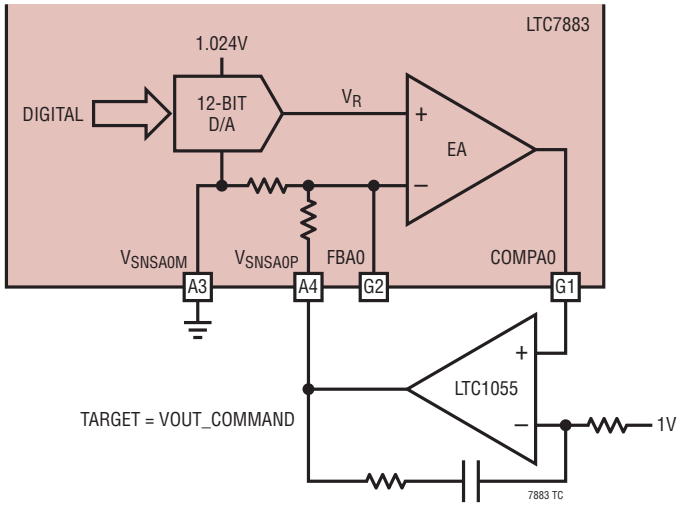
FB[A/B][1:0]: Error Amplifier Inverting Inputs. These pins provide an internally scaled version of the output voltage for use in loop compensation.

GND: Ground. *All GND balls must be soldered to a suitable PCB copper ground plane for proper electrical operation and to obtain the specified package thermal resistance.*

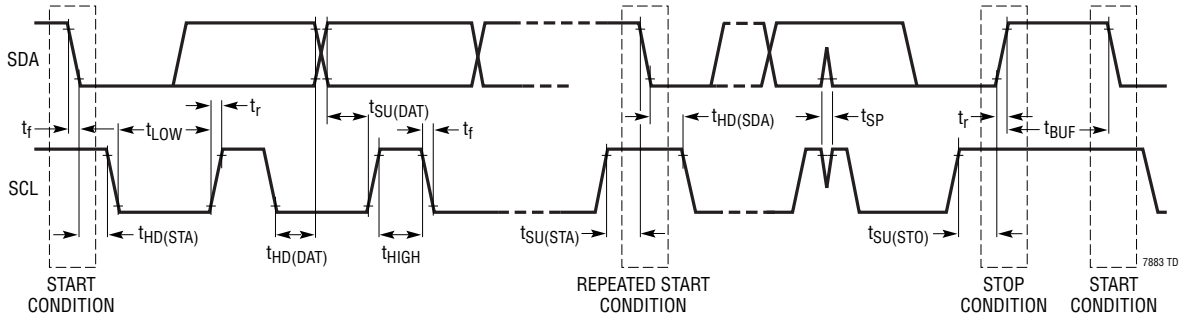
BLOCK DIAGRAM ("A" Side, 1 of 2 Units)



TEST CIRCUIT (Channel A0 Example)



TIMING DIAGRAM



OPERATION

Overview

The LTC7883 is a quad channel constant frequency analog voltage mode controller for DC/DC step-down applications. It features PMBus compliant digital interfaces for monitoring and control of important power system parameters. The IC operates from power supplies between 3V and 13.2V and is intended for conversion from V_{IN} between 3V and 38V to output voltages between 0.1V and 5.25V. It is designed to be used in a switching architecture with external FET drivers, including higher level integrations such as non-isolated power blocks.

Major features include:

- Digitally Programmable Output Voltage, Current Limit and Related Supervisors
- Digitally Programmable Input Voltage Supervisor
- Digitally Programmable Switching Frequency with PLL for Synchronous PolyPhase Operation Up to 8 Phases
- Digitally Programmable On and Off Delay Times
- Digitally Programmable Soft-Start/Stop
- Operating Condition Telemetry
- Fully Differential Load Sense
- Nonvolatile Configuration Memory with ECC Capable of Standalone Operation
- Optional External Resistor Configuration of Key Operating Parameters
- Optional Time-Base Interconnect for Synchronization Between Multiple Controllers
- Warning and Fault Status with Fault Event Data Logging
- PMBus Revision 1.2 Compliant Interface Up to 400kHz

Internal Structure

The LTC7883 comprises two dual-channel units, each equivalent to an LTC3882-2 with the added feature of a hardware PMBus write protect for each unit.

Refer to the LTC3882-1/LTC3882-2 data sheet for a detailed description of operation, PMBus command set, and applications information for each unit.

Refer to the LTC3888 data sheet for additional details on operation of the WP pins and their interaction with the PMBus WRITE_PROTECT command on each unit.

Unique Special ID

Each internal unit of the LTC7883 reports a unique MFR_SPECIAL_ID to differentiate it from an LTC3882-1/LTC3882-2. Table 1 lists MFR_SPECIAL_ID values for these products. X is adjustable by the manufacturer.

Table 1. MFR_SPECIAL_ID Values

DEVICE	MFR_SPECIAL_ID	MFR_MODEL
LTC3882-2	0x452X	LTC3882-2
LTC7883 Unit A	0x450X	LTC7883A
LTC7883 Unit B	0x451X	LTC7883B

OPERATION

Additional Identification Commands

The LTC7883 features a few new PMBus product identification commands as detailed in Table 2.

Switching Frequency and Phase

There is a high degree of flexibility for setting the PWM operating frequency of the LTC7883. The switching frequency of the PWM can be established with an internal oscillator or an external time base. The internal phase-locked loop (PLL) synchronizes PWM control to this timing reference with proper phase relation, whether the clock is provided internally or externally. The device can also be configured to provide the master clock to other ICs through PMBus command, EEPROM setting, or external configuration resistors as outlined in application Table 6. For PMBus or EEPROM configuration, an LTC7883 unit is designated as a clock master by clearing bit 4 of MFR_CONFIG_ALL_LTC3882-1. As clock master, an LTC7883 unit will drive its open-drain SYNC pin at the selected rate with a pulse width of 125ns. An external pull-up resistor between SYNC and V_{DD33} is required in this case. Only one unit connected to SYNC should be designated to drive the pin. If more than one LTC7883 unit sharing SYNC is programmed as clock master, just one of the units is automatically elected to provide the clock. The others disable their SYNC outputs and indicate this with bit 10 of MFR_PADS_LTC3882-1.

Unlike the LTC3882-1/LTC3883-2, which only allows a fixed set of predetermined frequencies, the LTC7883 FREQUENCY_SWITCH command supports a continuous range of values from 250kHz to 2.5MHz. The special case of 0x0000 for External SYNC Only is not permitted by the LTC7883. Sending this FREQUENCY_SWITCH command value will result in a CML fault for invalid data.

The LTC7883 will automatically accept an external SYNC input, disabling is own SYNC drive if necessary, as long as the external clock frequency is greater than 1/2 of the programmed internal oscillator. Whether configured to drive SYNC or not, an LTC7883 unit can continue PWM operation at the selected frequency (FREQUENCY_SWITCH) using its own internal oscillator if an expected external clock signal is not present.

The MFR_PWM_CONFIG_LTC3882-1 command can be used to configure the phase of each channel. Desired phase can also be set from EEPROM or external configuration resistors as outlined in Table 6. Phase designates the relationship between the falling edge of SYNC and the internal clock edge that resets the PWM latch. That reset turns off the top power switch, producing a PWM falling edge. Additional small propagation delays to the PWM control pins will apply.

Table 2. New Identification Commands

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	DEFAULT VALUE	
						UNIT A	UNIT B
ID_DEVICE_ID	0xAD	LTC7883 Model Number	R String	N	ASC	LTC7883A	LTC7883B
ID_DEVICE_REV	0xAE	LTC7883 Device Revision Code	R String	N	ASC	C0001	C0001

OPERATION

The phase relationships and frequency are independent of each other, providing numerous application options. Multiple LTC7883 units/ICs can be synchronized to realize a PolyPhase array. In this case the phases should be separated by 360/n degrees, where n is the number of phases driving the output voltage rail.

Serial Bus Addressing

The LTC7883 supports four types of serial bus addressing schemes to access the individual PWM channels separately or jointly.

- Global Bus Addressing
- Power Rail Addressing
- Individual Unit (Device) Addressing
- Page+ Channel Addressing

Each internal unit of the LTC7883 must be given a unique serial bus address for configuration and control. These units addresses can be derived from a combination of external configuration resistors attached to the ASEL pins and PMBus command values stored in on-board EEPROM. This method of using ASEL pins to specify some or all of each unit's physical address is necessary when using default factory EEPROM programing, where both units are assigned to 0x4F. Applying external resistor configuration for unit addresses is recommended, as it allows for easier device recovery under a wide range of programming errors. Refer to the values in Table 7 for full details on setting each unit address.

Advanced Power Stages

Some LTC7883 factory EEPROM defaults have been modified from LTC3882-1/LTC3882-2 values to better accommodate newer, advanced power stages that provide an output proportional to load current. Table 3 details these values. Refer to Figure 1 for an example of interfacing the LTC7883 to power stages or blocks of this type. If traditional DCR or discrete resistor sense of output current is used as shown on the front page, refer to factory EEPROM defaults given for Table 3 commands in the LTC3882-1/LTC3882-2 data sheet.

Table 3. Unique LTC7883 Default Factory EEPROM Values

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	DEFAULT VALUE
IOUT_CAL_GAIN	0x38	Ratio of I_{SENSE} ± Voltage to Sensed Current	R/W Word	Y	L11	mΩ	0.25mΩ 0xAA00
IOUT_OC_FAULT_LIMIT	0x46	Output Overcurrent Fault Limit	R/W Word	Y	L11	A	70.0A 0xEA30
IOUT_OC_WARN_LIMIT	0x4A	Output Overcurrent Warning Limit	R/W Word	Y	L11	A	50.0A 0xE320
MFR_IOUT_CAL_GAIN_TC	0xF6	Output Current Sense Element Temperature Coefficient	R/W Word	Y	CF	ppm/°C	0ppm/°C 0x0000

APPLICATIONS INFORMATION

Using FREQUENCY_SWITCH

Each unit in the LTC7883 that is a clock slave should have FREQUENCY_SWITCH programmed to the same value as its clock master, whether another LTC7883 or not. In the case where external synchronization will be used to control the shared SYNC line, each LTC7883 should be programmed with a value of FREQUENCY_SWITCH that is as close to the external clock frequency as possible.

Resistor Configuration Pins

Like the LTC3882-1/LTC3882-2, each LTC7883 unit is programmed to use external resistor configuration by factory default. This allows output voltage, PWM frequency and phasing, and the PMBus address to be set without programming the part through its serial interface or purchasing devices with custom EEPROM contents. The RCONFIG pins all require a resistor divider between V_{DD25} and GND. The RCONFIG pins are only interrogated at initial power-up and during a reset, so modifying their values on-the-fly is not recommended. RCONFIG pins on the same unit can share a single resistor divider if they require identical programming, but these dividers should not be shared across different LTC7883 units. Resistors with a tolerance of 1% or better must be used to assure proper operation. In Table 4 through Table 6, R_{TOP} is connected between V_{DD25} and the RCONFIG pin, while R_{BOT} is connected between the pin and GND. Noisy clock signals should not be routed near these pins.

RCONFIG address selection for each LTC7883 unit follows the values given in Table 7 of this data sheet. Refer to Application Note 152: Power System Management Addressing.

Output voltage can be set as shown in Table 4. For example, setting R_{TOP} to 16.2kΩ and R_{BOT} to 17.4kΩ is equivalent to programming a VOUT_COMMAND value of 1.8V. Refer to the Operation section of the LTC3882-1 data sheet for related parameters that are also automatically set as a percentage of the programmed V_{OUT} if resistor configuration pins are used to determined output voltage.

Operating PWM frequency can be set as shown in Table 5. Note that if SYNC pins are shared between LTC7883 units, all those units should be programmed to the same frequency, but only one SYNC output should be enabled. All other SYNC outputs should be disabled. Refer to the following PCFG discussion for additional details on controlling SYNC output enable with external programming resistors.

Table 4. VO*n*CFGA/B Resistor Programming

R_{TOP} (kΩ)	R_{BOT} (kΩ)	V_{OUT} (V)
0 or Open	Open	From EEPROM
10	23.2	5.0
10	15.8	3.3
16.2	20.5	2.5
16.2	17.4	1.8
20	17.8	1.5
20	15	1.35
20	12.7	1.25
20	11	1.2
24.9	11.3	1.15
24.9	9.09	1.1
24.9	7.32	1.0
24.9	5.76	0.9
24.9	4.32	0.75
30.1	3.57	0.65
30.1	1.96	0.6
Open	0	Output OFF* (V_{OUT} from EEPROM)

*OPERATION value and RUN*n* pin must both command the channel to start from this configuration.

Table 5. FCFGA/B Resistor Programming

R_{TOP} (kΩ)	R_{BOT} (kΩ)	SWITCHING FREQUENCY (kHz)
0 or Open	Open	From EEPROM
10	23.2	2500
10	15.8	2250
16.2	20.5	2000
16.2	17.4	1750
20	17.8	1500
20	15	1250
20	12.7	1000
20	11	900
24.9	11.3	750
24.9	9.09	600
24.9	7.32	500
24.9	5.76	450
24.9	4.32	400
30.1	3.57	350
30.1	1.96	300
Open	0	250

Note: ADI does not recommend using the following PWM frequencies in new designs: 600kHz, 750kHz, 900kHz, and 1MHz.

APPLICATIONS INFORMATION

Table 6 shows various PWM phase configurations that can be selected with external resistor programming. This RCONFIG pin, as with the LTC3882-1/LTC3882-2, can also be used to control SYNC output drive for each LTC7883 unit. However, there are more choices here, affording greater flexibility in PolyPhase configurations.

For example, to build a four-phase rail, one approach might be to select R_{TOP} of 24.9kΩ and R_{BOT} of 5.76kΩ for PHAS_CFG of Unit A (PCFGA). This programs the phase angles of PWMA0 to 0° and PWMA1 to 180°, relative to the falling edge of SYNC. Unit A is enabled to drive the shared SYNC clock line through the SYNCA pin (open-drain output).

For Unit B, R_{TOP} of 10kΩ and R_{BOT} of 15.8kΩ selects phase angles for PWMB0 of 90° and PWMB1 of 270°, configuring SYNCB as an input to accept the master clock from Unit A. The result, when wired as a 4-phase rail as described in PolyPhase Operation and Load Sharing under Applications Information in the LTC3882-1/LTC3882-2 data sheet, will be four non-overlapping phases operating in quadrature as desired. In this case, either Unit A or Unit B may be defined and wired as the voltage loop master, since this function is independent of clock mastering.

Only mix phase selections on PolyPhase rails that have the same maximum duty cycle specified in Table 6.

Table 6. CFGA/B Resistor Programming

R_{TOP} (kΩ)	R_{BOT} (kΩ)	θ_{SYNC} TO θ_0	θ_{SYNC} TO θ_1	MAXIMUM DUTY CYCLE	SYNC OUTPUT DISABLED
0 or Open	Open	From EEPROM	From EEPROM	See MFR_PWM_CONFIG	From EEPROM
10	23.2	135°	315°	87.5%	Yes
10	15.8	90°	270°		
16.2	20.5	45°	225°		
16.2	17.4	0°	180°		
20	17.8	120°	300°	83.3%	Yes
20	15	60°	240°		
20	12.7	0°	180°		
20	11	0°	120°		
24.9	11.3	135°	315°	87.5%	No
24.9	9.09	90°	270°		
24.9	7.32	45°	225°		
24.9	5.76	0°	180°		
24.9	4.32	120°	300°	83.3%	No
30.1	3.57	60°	240°		
30.1	1.96	0°	180°		
Open	0	0°	120°		

APPLICATIONS INFORMATION

Table 7. ASEL*n* Resistor Programming

R_{TOP} (kΩ)	R_{BOT} (kΩ)	ASEL1		ASEL0	
		LTC3882-1 DEVICE ADDRESS BITS[6:4]		LTC3882-1 DEVICE ADDRESS BITS[3:0]	
		BINARY	HEX	BINARY	HEX
0 or Open	Open	from EEPROM		from EEPROM	
10	23.2			1111	F
10	15.8			1110	E
16.2	20.5			1101	D
16.2	17.4			1100	C
20	17.8			1011	B
20	15			1010	A
20	12.7			1001	9
20	11			1000	8
24.9	11.3	111	7	0111	7
24.9	9.09	110	6	0110	6
24.9	7.32	101	5	0101	5
24.9	5.76	100	4	0100	4
24.9	4.32	011	3	0011	3
30.1	3.57	010	2	0010	2
30.1	1.96	001	1	0001	1
Open	0	000	0	0000	0

Design Example

As a design example, consider a 180W 4-phase application such as the one shown in Figure 1, where V_{IN} = 12V, V_{OUT} = 1.5V, and I_{OUT} = 120A. An auxiliary 7V source supplies the LTC7883 V_{CC} pins and the power stage FET gate drive voltage with a 2.2µF ceramic bypass, in addition to a smaller 0.1µF ceramic placed near the LTC7883 filtering HF components. Bypassing is also provided for each V_{DD33} (2.2µF) and V_{DD25} (1µF) LDO output. These LDO outputs should not be shared with each other or separate ICs that might have outputs of the same name, because they have independent, internal control loops.

The Delta D12S1R8140D power block is chosen for its high level of integration, power efficiency and direct interface to the LTC7883 using 3.3V three-state control. The use of a power block with the LTC7883 creates an efficient solution in terms of power, parts count and total solution volume. Placing the power stage directly beneath the LTC7883 on the other side of the PCB allows direct through-hole via connections to the power block for PWM controls, as well as output voltage and current sense. Table 8 shows the recommended channel mapping for the most efficient interconnect in this case. CCM operation, fast boost refresh, low V_{OUT} range and digital output voltage servo are selected by programming MFR_PWM_MODE_LTC3882-1 to 0xC0 on all channels.

Table 8. Suggested Power Block Channel Mapping

LTC7883 PWM	LTC7883 UNIT	PMBus PAGE (CH)	PB PWM
A0	A	0	2
A1		1	1
B0	B	0	4
B1		1	3

The regulated output is established by programming the VOUT_COMMAND stored in EEPROM for PWMA0 (the master channel) to 1.5V. The other PWMs are designated as slaves to PWMA0 by wiring their FB pins to V_{DD33} and shorting their COMP control pins to COMPA0 as shown.

The frequency and phase are also set by EEPROM values. Both units are programmed to operate at 500kHz (default FREQUENCY_SWITCH), with Unit A providing the clock master (see Figure 3, SYNCB output disabled by bit 4 of MFR_CONFIG_ALL_LTC3882-1 on Unit B). MFR_PWM_CONFIG_LTC3882-1 is programmed to 0x14 on Unit A to put PWMA0 phase at 0° and PWMA1 phase at 180°. This register is programmed to 0x16 on Unit B to put PWMB0 phase at 90° and PWMB1 phase at 270°, producing optimum 4-phase separation for minimum input and output ripple.

With these configurations, the inductors on the power block (160nH nominal) create an I_{OUT} ripple of $16.4A_{P-P}$. Each channel supplies 40ADC to the output at full load, resulting in a peak phase current of 48A. Setting IOUT_FAULT_LIMIT to 50A per phase adequately protects against the typical inductor saturation current of 55A.

APPLICATIONS INFORMATION

Two 100µF SUNCON capacitors and four 22µF ceramic capacitors are selected to provide acceptable input AC impedance against the designed converter ripple current. Ten 220µF ceramic capacitors are chosen for the output to maintain supply regulation during severe transient conditions and to minimize output voltage ripple.

The power block provides its own output current monitor signals for use by the LTC7883. The interface network, shown in detail for differential input CSA1, is also replicated for the other three channels. These remove high frequency noise from the power block outputs and scale those signals to be compatible with the LTC7883 inputs. A fixed common mode reference voltage is required for the power block –CS[4:1] outputs. A filtered resistor divider from V_{DD33} (10k/12.1k/4.3µF) fulfills this requirement, driving the negative side of the differential current sense (CSx) signals.

External temperature sense will employ an accurate ΔV_{BE} method. Q1 serves to sense the temperature of the PCB as close to the power block as physically possible, and the 10nF filter capacitor should be placed with the BJT. Unused TSNS inputs are loaded with 2.74k to produce a benign reading of about 25°C with factory EEPROM settings, if the direct V_{BE} interface mode is selected by MFR_PWM_MODE_LTC3888-1 on these channels.

Each internal LTC7883 unit must be configured for a unique address. Resistor configuration is used on the ASEL pins to program the three most significant PMBus address bits from EEPROM (MFR_ADDRESS, 0x4X). Then each unit is given its own unique lower address nibble, setting the two addresses to 0x4C (Unit A) and 0x4D (Unit B). Ensure the selected addresses do not collide with global addresses or any other specific devices in the system. Identical MFR_RAIL_ADDRESS should be set in EEPROM for all four channels to allow single-command control of common rail parameters such as IOUT_OC_FAULT_LIMIT. The LTC7883 units also respond to 7-bit global addresses 0x5A and 0x5B. MFR_ADDRESS and MFR_RAIL_ADDRESS should not be set to either of these values.

PMBus connections, as well as shared RUN control and fault propagation ($\overline{FLT}$) are provided. SYNC can be used to synchronize other PWMs to this rail if required. Recommended PMBus connections and shared PSM connections are shown in more detail in Figure 3.

Pull-ups are provided on all shared open-drain signals (Figure 1 and Figure 3). The values shown assume a maximum 100pF line load and PMBus rate of 100kHz. These pins should not be left floating. Termination to 3.3V ensures the absolute maximum ratings for the pins are not exceeded. All other operating parameters such as soft start/stop and desired faults responses are programmed via PMBus command values stored in internal LTC7883 EEPROM.

TYPICAL APPLICATIONS

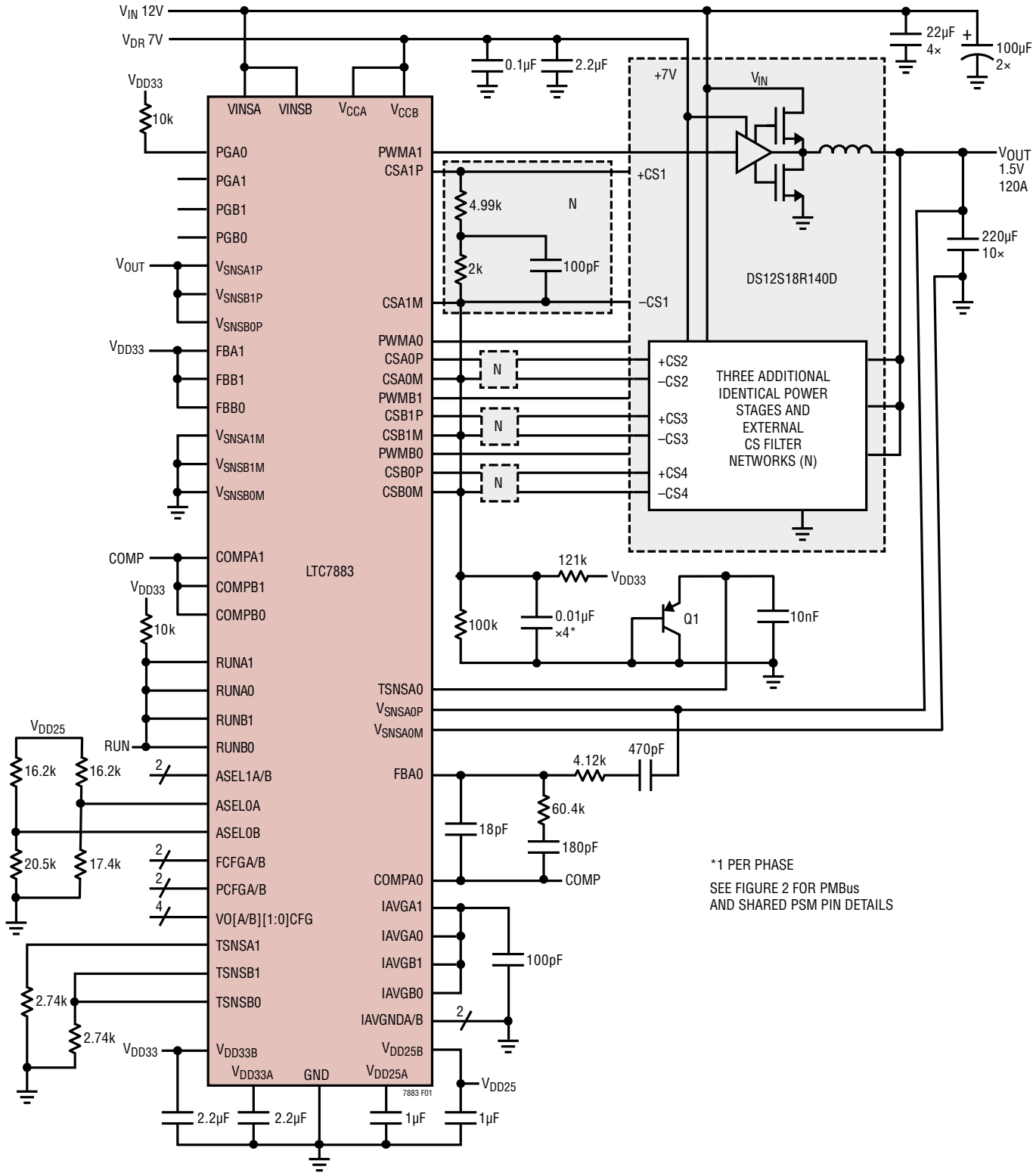


Figure 1. High Density 1.5V/120A 500kHz 4-Phase Converter Using Quad Power Block

TYPICAL APPLICATIONS

See Figure 2 for the LTC7883 controller plus the LTC7050/LTC7051 SilentMOS™ smart power stage. The LTC7050/LTC7051 have an on-chip diode that can be used by the LTC7883 to sense the temperature. Use the direct V_{BE} measurement option in MFR_PWM_MODE of the LTC7883. Consult the factory or review the LTC3882 DS for more information on this temperature sensing method.

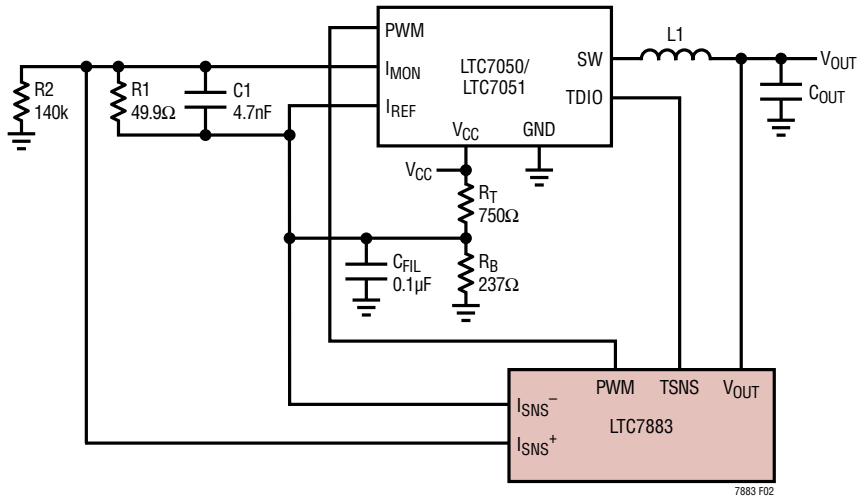
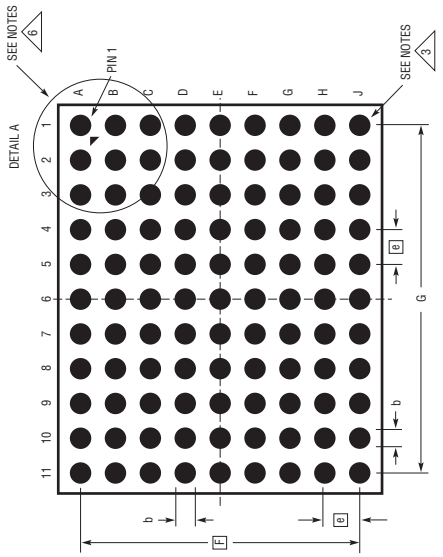


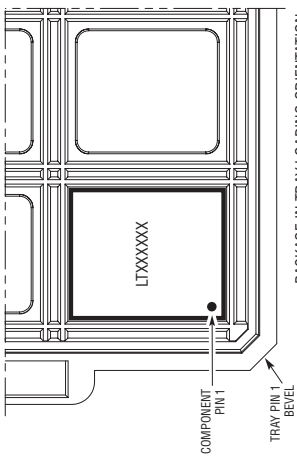
Figure 2. LTC7883 with LTC7050/LTC7051 SilentMOS Smart Power Stage

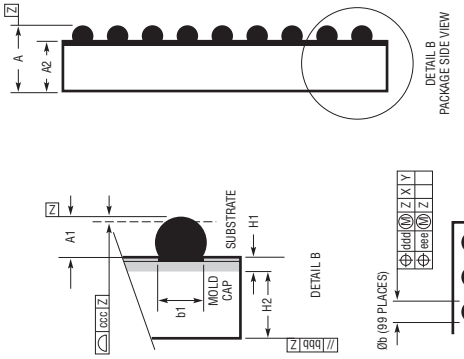
PACKAGE DESCRIPTION

BGA Package
99-Lead (9mm × 7.5mm × 1.52mm)
(Reference LTC DWG # 05-08-7029 Rev Ø)

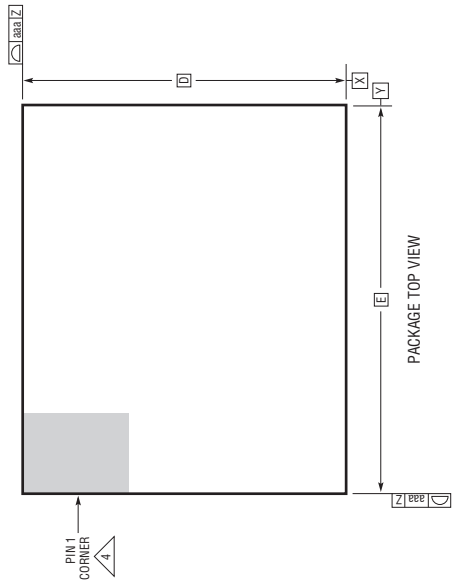


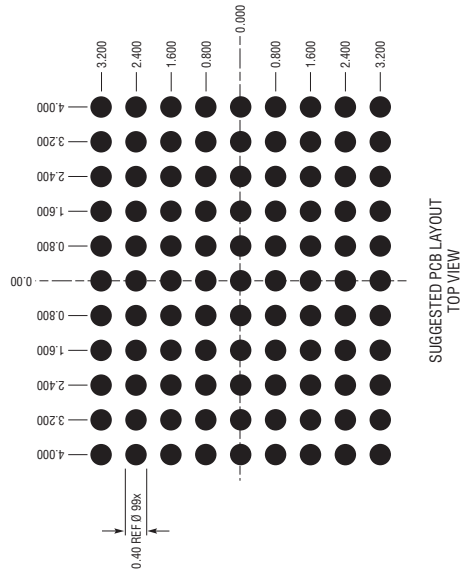
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS. DRAWING NOT TO SCALE
3. BALL DESIGNATION PER JEP95
4. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY





DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	1.32	1.52	1.72	
A1	0.30	0.40	0.50	BALL HT
A2	1.02	1.12	1.22	
b	0.45	0.50	0.55	BALL DIMENSION
b1	0.37	0.40	0.43	PAD DIMENSION
D		7.50		
E		9.00		
e		0.80		
F		6.40		
G		8.00		
H1		0.32 REF		SUBSTRATE THK
H2		0.80 REF		MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.15	
eee			0.08	
TOTAL NUMBER OF BALLS: 99				





REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
0	12/21	Initial release	—
A	07/25	Changes to Description	1
		Changes to Operation: Internal Structure, Unique Special ID	16
		Changes to Operation: Switching Frequency and Phase	17
		Changes to Operation: Advanced Power Stages	18
		Changes to Applications Information: Resistor Configurations Pins, added note to Table 5	19, 20

TYPICAL APPLICATION (Also See Figure 1)

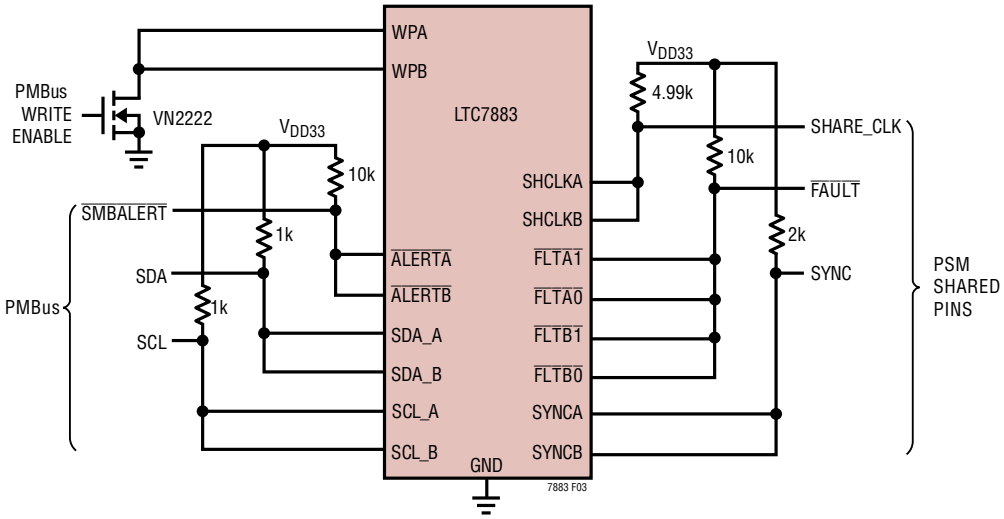


Figure 3. LTC7883 PMBus Interface and Configuration

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4700	Dual 50A or Single 100A Step-Down DC/DC µModule Regulator with Digital Power Management	V_{IN} Up to 16V; 0.5V ≤ V_{OUT} (±0.5%) ≤ 1.8V, ±3% I_{OUT} ADC Accuracy, Fault Logging, I^2C/PMBus Interface, 330-Lead BGA Package
LTC3882/ LTC3882-1	Dual Output Multiphase Step-Down DC/DC Voltage Mode Controller with Digital Power System Management	V_{IN} Up to 38V, 0.5V ≤ V_{OUT} (±0.5%) ≤ 5.25V, Fault Logging, I^2C/PMBus Interface, with EEPROM and 16-Bit ADC.
LTC3884/ LTC3884-1	Dual Output Multiphase Step-Down DC/DC Current Mode Controller with Sub-mΩ DCR Sensing and Digital Power Management	V_{IN} Up to 38V, 0.5V ≤ V_{OUT} (±0.5%) ≤ 5.5V, Fault Logging, I^2C/PMBus Interface, EEPROM, 16-Bit ADC, Input Current Sense, Programmable Analog Loop Compensation
LTC3886	60V Dual Output Multiphase Step-Down DC/DC Current Mode Controller with Digital Power System Management	V_{IN} Up to 60V, 0.5V ≤ V_{OUT} (±0.5%) ≤ 13.8V, Fault Logging, I^2C/PMBus Interface, EEPROM, 16-Bit ADC, Input Current Sense, Programmable Analog Loop Compensation
LTC3887/ LTC3887-1	Dual Output Multiphase Step-Down DC/DC Current Mode Controller with Digital Power System Management	V_{IN} Up to 24V, 0.5V ≤ V_{OUT} (±0.5%) ≤ 5.5V, Fault Logging, I^2C/PMBus Interface, EEPROM, 16-Bit ADC
LTC3889	60V Dual Output Multiphase Step-Down DC/DC Current Mode Controller with Digital Power System Management	V_{IN} Up to 60V, 1V ≤ V_{OUT} (±0.5%) ≤ 40V, Fault Logging, I^2C/PMBus Interface, EEPROM, 16-Bit ADC, Input Current Sense, Programmable Analog Loop Compensation
LTC7880	Dual Output Multiphase DC/DC Current Mode Boost Controller with Digital Power System Management	V_{IN} Up to 40V, V_{OUT} Up to 60V with ±0.5% Accuracy, Fault Logging, I^2C/PMBus Interface, EEPROM, 16-Bit ADC, Input Current Sense, Programmable Analog Loop Compensation
LTC2980	16-Channel PMBus Power System Manager Featuring Accurate Output Voltage Measurement and Trim	Fault Logging, I^2C/PMBus Interface, EEPROM, 16-Bit ADC Monitors 16 Output Voltages, 2 Input Voltages and Die Temperature
LTC2980-24	24-Channel PMBus Power System Manager Featuring Accurate Output Voltage Measurement and Trim	Fault Logging, I^2C/PMBus Interface, EEPROM, 16-Bit ADC Monitors 24 Output Voltages, 3 Input Voltages and Die Temperature
LTC7851/ LTC7851-1	Quad Output Multiphase Step-Down DC/DC Voltage Mode Controller with Soft-Start and Accurate Current Share	V_{IN} up to 27V, 0.6V ≤ V_{OUT} ≤ 5V, Operates up to 2.25MHz with Power FET Drivers, DrMOS Devices and Power Blocks
LTC3888/ LTC3888-1	Dual Loop, 8-Phase Step-Down DC/DC Controller with Digital Power System Management	V_{IN} Up to 26.5V; 0.1V ≤ V_{OUT} (±0.5%) ≤ 3.45V, Fault Logging, I^2C/PMBus Interface with NVM and 16-Bit ADC and Load Step Emulation