

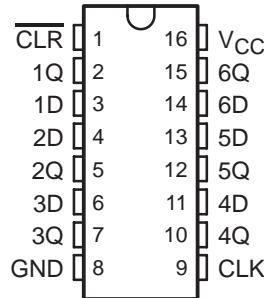
- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 8.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce)
<0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
>2.3 V at V_{CC} = 3.3 V, T_A = 25°C
- Support Mixed-Mode Voltage Operation on All Ports
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

description/ordering information

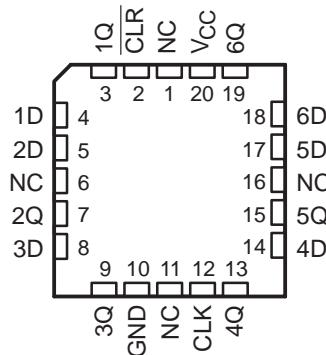
The 'LV174A devices are hex D-type flip-flops designed for 2-V to 5.5-V V_{CC} operation.

These devices are positive-edge-triggered flip-flops with a direct clear (CLR) input. Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of the clock pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

SN54LV174A . . . J OR W PACKAGE
SN74LV174A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV174A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE [†]	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SOIC – D	Tube of 40	SN74LV174AD
		Reel of 2500	SN74LV174ADR
	SOP – NS	Reel of 2000	SN74LV174ANSR
	SSOP – DB	Reel of 2000	SN74LV174ADBR
		Tube of 90	SN74LV174APW
		Reel of 2000	SN74LV174APWR
		Reel of 250	SN74LV174APWT
-55°C to 125°C	TVSOP – DGV	Reel of 2000	SN74LV174ADGVR
	CDIP – J	Tube of 25	SNJ54LV174AJ
	CFP – W	Tube of 150	SNJ54LV174AW
	LCCC – FK	Tube of 55	SNJ54LV174AFK
			SNJ54LV174AFK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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**TEXAS
INSTRUMENTS**

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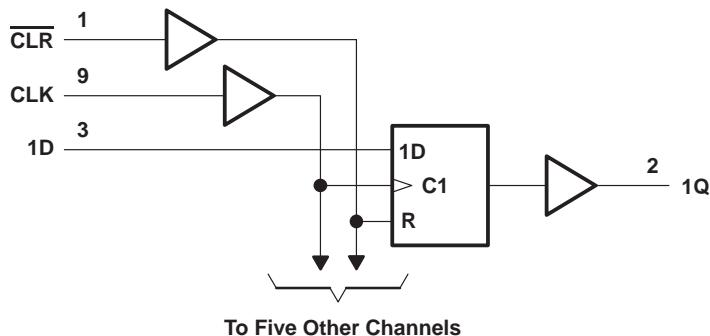
SN54LV174A, SN74LV174A HEX D-TYPE FLIP-FLOPS WITH CLEAR

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FUNCTION TABLE

INPUTS			OUTPUT
CLR	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q ₀

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-20 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	73°C/W
DB package	82°C/W
DGV package	120°C/W
NS package	64°C/W
PW package	108°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 5.5 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

		SN54LV174A		SN74LV174A		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	1.5	1.5	V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7	V _{CC} × 0.7	V _{CC} × 0.7	
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7	V _{CC} × 0.7	V _{CC} × 0.7	
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7	V _{CC} × 0.7	V _{CC} × 0.7	
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	0.5	0.5	V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3	V _{CC} × 0.3	V _{CC} × 0.3	
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3	V _{CC} × 0.3	V _{CC} × 0.3	
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3	V _{CC} × 0.3	V _{CC} × 0.3	
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	-50	-50	-50	μA
		V _{CC} = 2.3 V to 2.7 V	-2	-2	-2	mA
		V _{CC} = 3 V to 3.6 V	-6	-6	-6	
		V _{CC} = 4.5 V to 5.5 V	-12	-12	-12	
I _{OL}	Low-level output current	V _{CC} = 2 V	50	50	50	μA
		V _{CC} = 2.3 V to 2.7 V	2	2	2	mA
		V _{CC} = 3 V to 3.6 V	6	6	6	
		V _{CC} = 4.5 V to 5.5 V	12	12	12	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	200	200	200	ns/V
		V _{CC} = 3 V to 3.6 V	100	100	100	
		V _{CC} = 4.5 V to 5.5 V	20	20	20	
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV174A			SN74LV174A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} - 0.1			V _{CC} - 0.1			V
	I _{OH} = -2 mA	2.3 V	2			2			
	I _{OH} = -6 mA	3 V	2.48			2.48			
	I _{OH} = -12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V		0.1			0.1		V
	I _{OL} = 2 mA	2.3 V		0.4			0.4		
	I _{OL} = 6 mA	3 V		0.44			0.44		
	I _{OL} = 12 mA	4.5 V		0.55			0.55		
I _I	V _I = 5.5 V or GND	0 to 5.5 V		±1			±1		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V		20			20		μA
I _{off}	V _I or V _O = 0 to 5.5 V	0		5			5		μA
C _i	V _I = V _{CC} or GND	3.3 V		1.7			1.7		pF

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**SN54LV174A, SN74LV174A
HEX D-TYPE FLIP-FLOPS
WITH CLEAR**

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$			SN54LV174A		SN74LV174A		UNIT
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	CLR low	6		6.5		6.5		ns
		CLK high or low	7		7		7		
t_{SU}	Setup time before CLK^\uparrow	Data	8.5		9.5		9.5		ns
		CLR inactive	4		4		4		
t_H	Hold time, data after CLK^\uparrow		-0.5		0		0		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$			SN54LV174A		SN74LV174A		UNIT
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	CLR low	5		5		5		ns
		CLK high or low	5		5		5		
t_{SU}	Setup time before CLK^\uparrow	Data	5		6		6		ns
		CLR inactive	3		3		3		
t_H	Hold time, data after CLK^\uparrow		0		0		0		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$			SN54LV174A		SN74LV174A		UNIT
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	CLR low	5		5		5		ns
		CLK high or low	5		5		5		
t_{SU}	Setup time before CLK^\uparrow	Data	4.5		4.5		4.5		ns
		CLR inactive	2.5		2.5		2.5		
t_H	Hold time, data after CLK^\uparrow		0.5		0.5		0.5		ns

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV174A		SN74LV174A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			CL _L = 15 pF	55*	115*		50*		50		MHz
			CL _L = 50 pF	45	90		40		40		
t_{pd}	CLR	Q	CL _L = 15 pF		6.3*	17.3*	1*	19.5*	1	19.5	ns
					8.4*	17.1*	1*	19*	1	19	
t_{pd}	CLR	Q	CL _L = 50 pF		8.2	21.9	1	23.5	1	23.5	ns
					10.8	20.6	1	23	1	23	
$t_{sk(0)}$						2				2	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV174A		SN74LV174A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15 \text{ pF}$	95*	170*		80*		80		MHz
			$C_L = 50 \text{ pF}$	55	130		50		50		
t_{pd}	$\overline{\text{CLR}}$	Q	$C_L = 15 \text{ pF}$	4.5*	11.4*		1*	13.5*	1	13.5	ns
	CLK			5.8*	11*		1*	13*	1	13	
t_{pd}	$\overline{\text{CLR}}$	Q	$C_L = 50 \text{ pF}$	6	14.9		1	17	1	17	ns
	CLK			7.5	14.5		1	16.5	1	16.5	
$t_{\text{sk(o)}}$						1.5				1.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV174A		SN74LV174A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15 \text{ pF}$	130*	240*		110*		110		MHz
			$C_L = 50 \text{ pF}$	90	180		80		80		
t_{pd}	$\overline{\text{CLR}}$	Q	$C_L = 15 \text{ pF}$	3*	7.6*		1*	9*	1	9	ns
	CLK			4.1*	7.2*		1*	8.5*	1	8.5	
t_{pd}	$\overline{\text{CLR}}$	Q	$C_L = 50 \text{ pF}$	4.2	9.6		1	11	1	11	ns
	CLK			5.5	9.2		1	10.5	1	10.5	
$t_{\text{sk(o)}}$						1				1	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3 \text{ V}$, $C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER	SN74LV174A			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}		0.34	0.8	V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}		-0.3	-0.8	V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}		3.02		V
$V_{IH(D)}$ High-level dynamic input voltage		2.31		V
$V_{IL(D)}$ Low-level dynamic input voltage		0.99		V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance	$C_L = 50 \text{ pF}$, $f = 10 \text{ MHz}$	3.3 V	14	pF
		5 V	15.1	

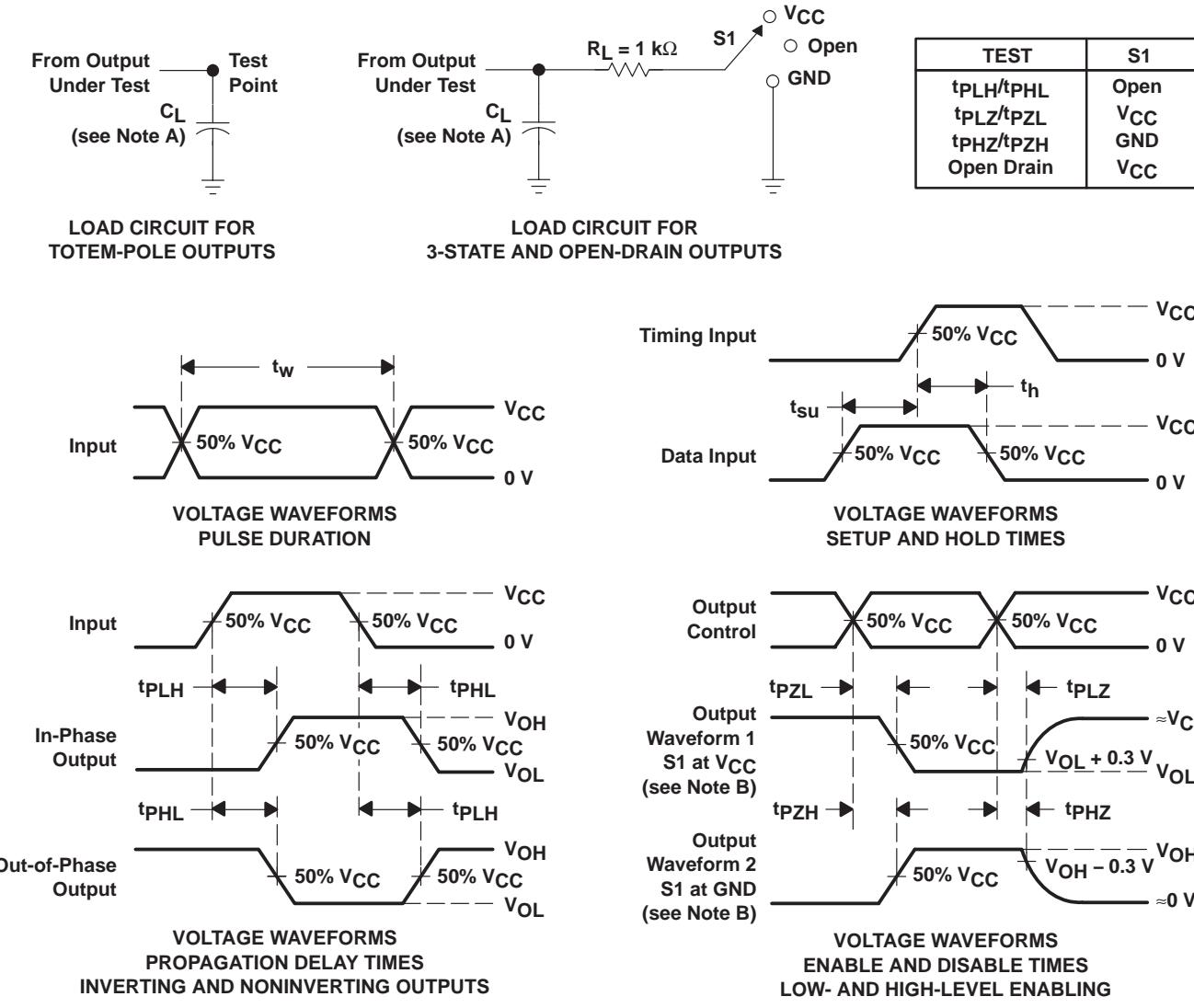
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SN54LV174A, SN74LV174A HEX D-TYPE FLIP-FLOPS WITH CLEAR

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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O = 50 \Omega$, $t_f \leq 3$ ns, $t_f \leq 3$ ns.
 D. The outputs are measured one at a time, with one input transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PHL} and t_{PLH} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV174AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV174A	Samples
SN74LV174ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV174A	Samples
SN74LV174ADGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV174A	Samples
SN74LV174ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV174A	Samples
SN74LV174ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV174A	Samples
SN74LV174ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV174A	Samples
SN74LV174ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV174A	Samples
SN74LV174APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV174A	Samples
SN74LV174APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV174A	Samples
SN74LV174APWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV174A	Samples
SN74LV174APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV174A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

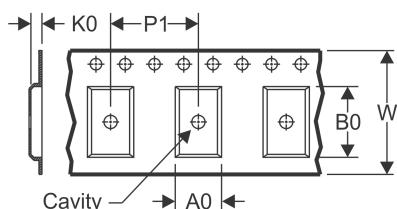
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

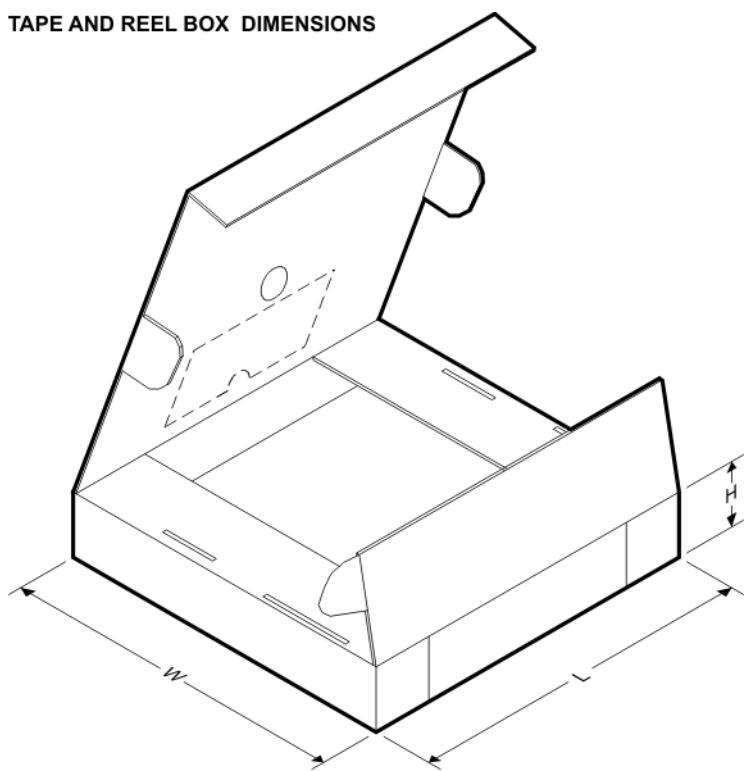
TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV174ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV174ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV174ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV174APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

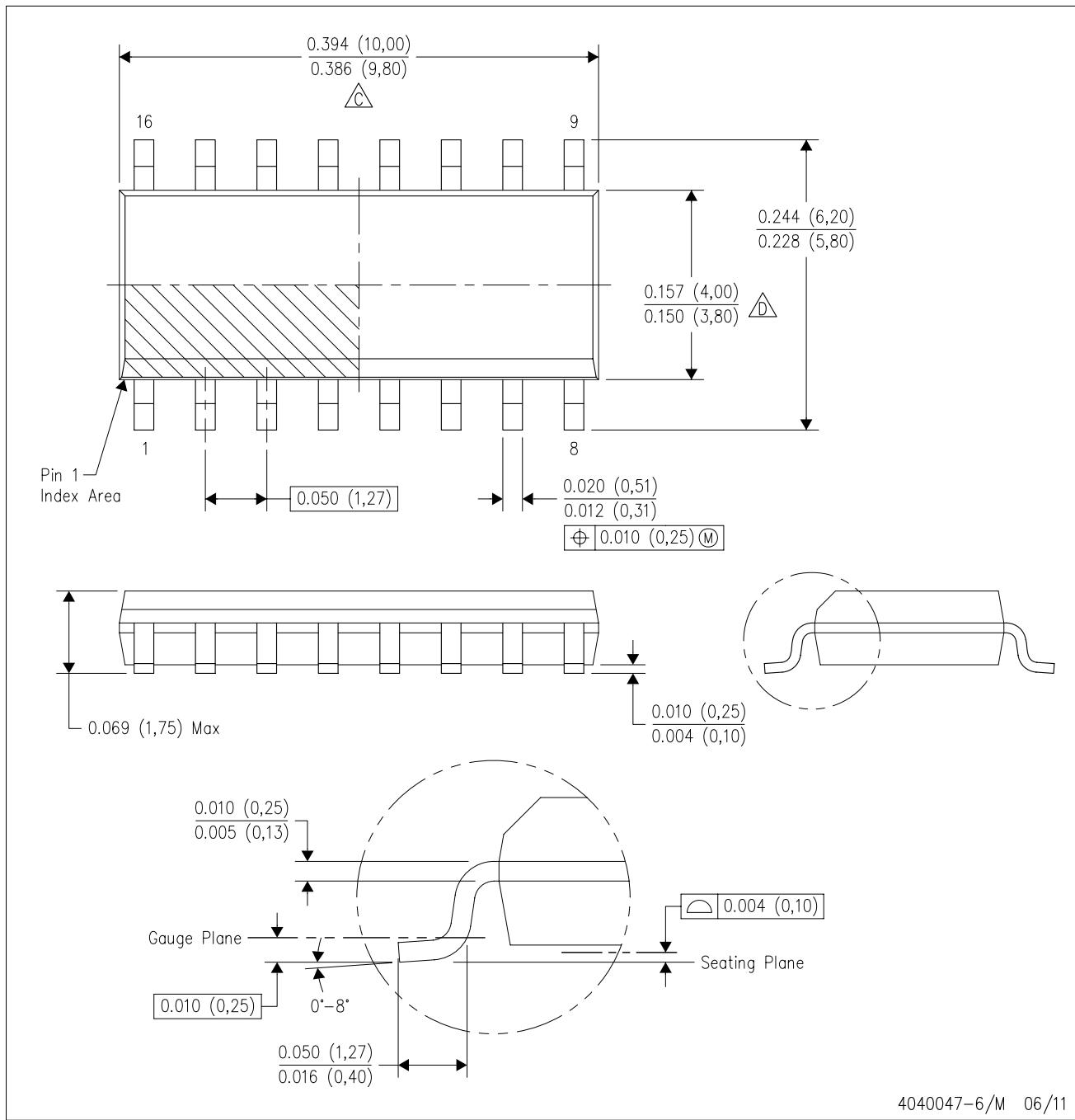
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV174ADGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
SN74LV174ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LV174ANSR	SO	NS	16	2000	367.0	367.0	38.0
SN74LV174APWR	TSSOP	PW	16	2000	367.0	367.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

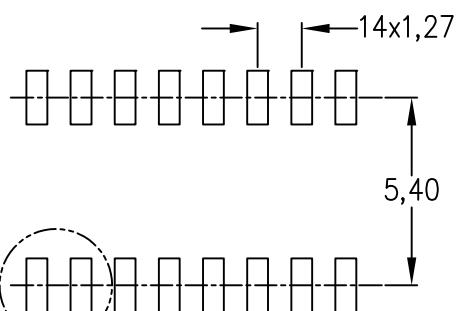
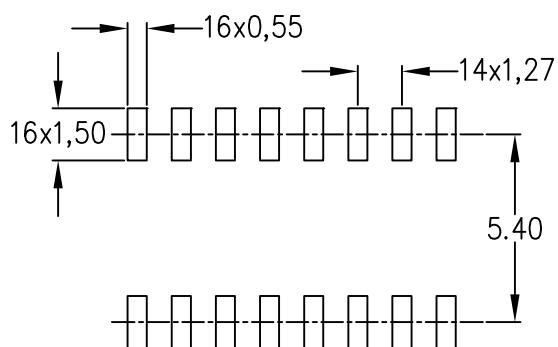
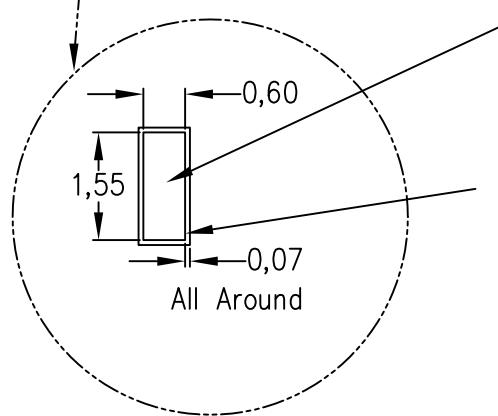
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

4211283-4/E 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



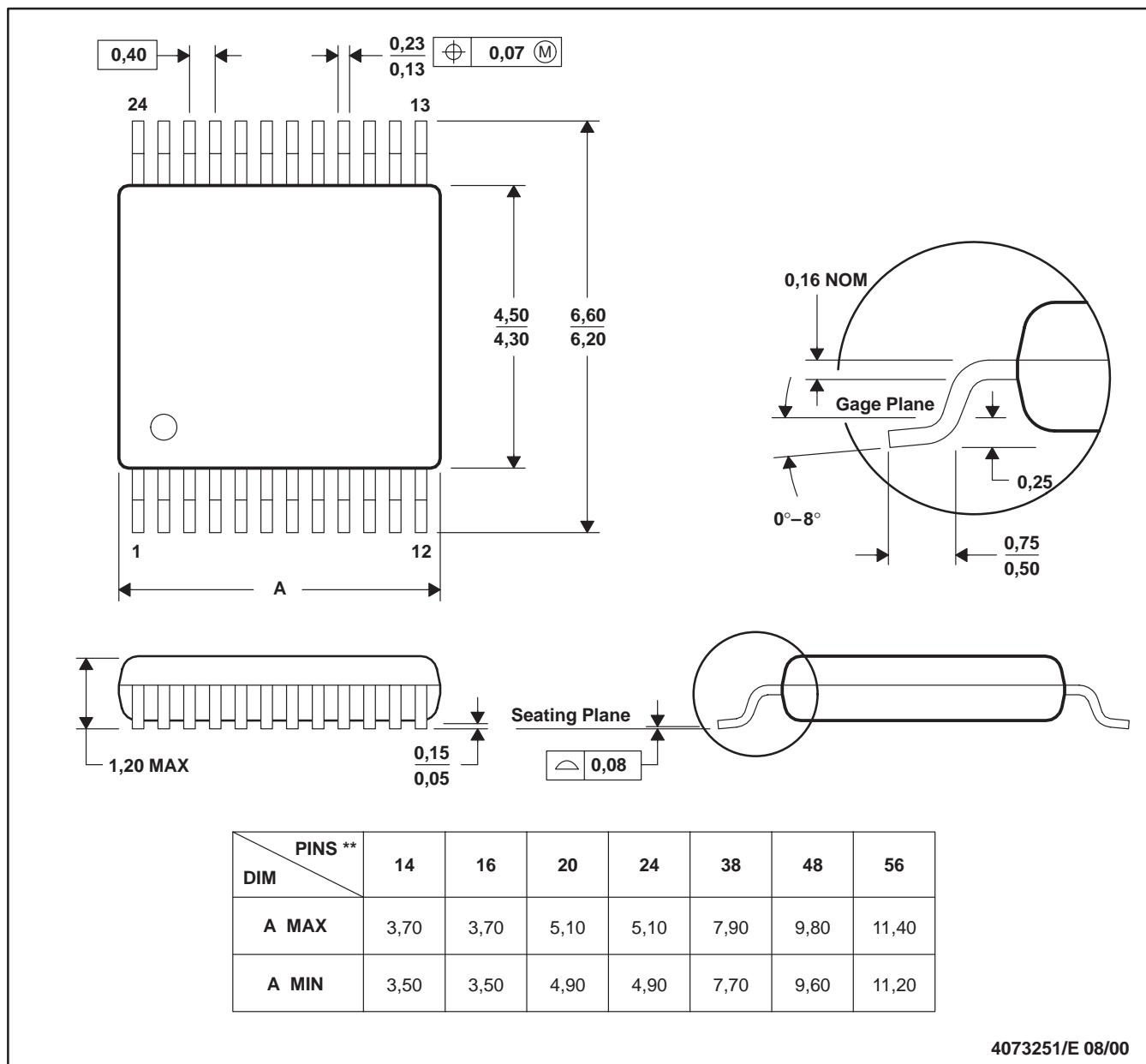
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

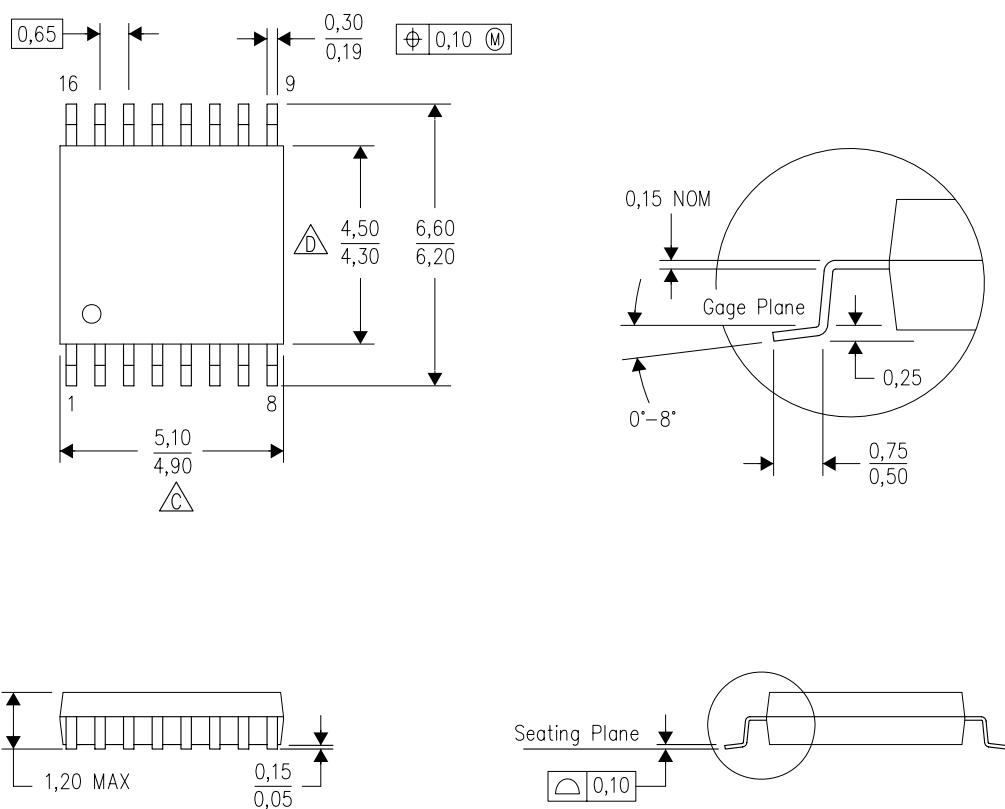
24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040064-4/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

 Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 each side.

 Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E Falls within JEDEC MO-153

E. TADS within SLEEC MU-155

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