High-Resolution Analog-to-Digital Converter

Check for Samples: ADS1281

FEATURES

- **High Resolution:**
  - **130dB SNR (250SPS)**
  - **127dB SNR (500SPS)**
- **High Accuracy:**
  - **THD: –122dB (typ), –115dB (max)**
  - **INL: 0.6ppm**
- **Inherently Stable Modulator with Fast Responding Over-Range Detection**
- **Flexible Digital Filter:**
  - **Sinc + FIR + IIR (Selectable)**
  - **Linear or Minimum Phase Response**
  - **Programmable High-Pass Filter**
  - **Selectable FIR Data Rates:**
    - **250SPS to 4kSPS**
- **Filter Bypass Option**
- **Low Power Consumption:**
  - **Operating: 12mW**
  - **Shutdown: 10μW**
- **Calibration Engine for Offset and Gain Correction**
- **SYNC Input**
- **Analog Supply:**
  - **Unipolar (+5V) or Bipolar (±2.5V)**
- **Digital Supply: 1.8V to 3.3V**

APPLICATIONS

- **Energy Exploration**
- **Seismic Monitoring**
- **High-Accuracy Instrumentation**

DESCRIPTION

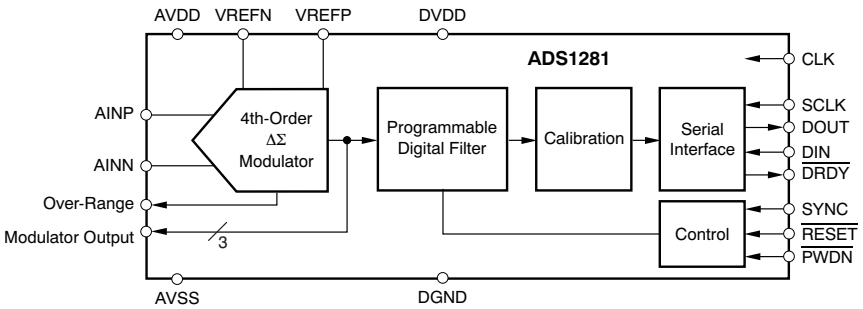
The ADS1281 is an extremely high-performance, single-chip analog-to-digital converter (ADC) designed for the demanding needs of energy exploration and seismic monitoring environments. The single-chip design promotes board area savings for improvements in high-density applications.

The converter uses a fourth-order, inherently stable, delta-sigma (ΔΣ) modulator that provides outstanding noise and linearity performance. The modulator is used either in conjunction with the on-chip digital filter, or can be bypassed for use with post-processing filters.

The digital filter consists of sinc and finite impulse response (FIR) low-pass stages followed by an infinite impulse response (IIR) high-pass filter (HPF) stage. Selectable decimation provides data rates from 250 to 4000 samples per second (SPS). The FIR low-pass stage provides both linear and minimum phase response. The HPF features an adjustable corner frequency. On-chip gain and offset scaling registers support system calibration.

The synchronization input (SYNC) can be used to synchronize the conversions of multiple ADS1281s. The SYNC input also accepts a clock input for continuous alignment of conversions from an external source.

Together, the modulator and filter dissipate only 12mW. The ADS1281 is available in a compact TSSOP-24 package and is fully specified from –40°C to +85°C, with a maximum operating range to +125°C.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

	ADS1281	UNIT
AVDD to AVSS	–0.3 to +5.5	V
AVSS to DGND	–2.8 to +0.3	V
DVDD to DGND	–0.3 to +3.9	V
Input current	100, momentary	mA
Input current	10, continuous	mA
Analog input voltage	AVSS – 0.3 to AVDD + 0.3	V
Digital input voltage to DGND	–0.3 to DVDD + 0.3	V
Maximum junction temperature	+150	°C
Operating temperature range	–40 to +125	°C
Storage temperature range	–60 to +150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

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ELECTRICAL CHARACTERISTICS

Limit specifications at –40°C to +85°C, typical specifications at +25°C, AVDD = +2.5V, AVSS = –2.5V, f_{CLK} (1) = 4.096MHz, VREFP = +2.5V, VREFN = –2.5V, DVDD = +3.3V, and f_{DATA} = 1000SPS, unless otherwise noted.

PARAMETER		CONDITIONS	ADS1281 MIN	ADS1281 TYP	ADS1281 MAX	UNIT
ANALOG INPUTS						
Full-scale input voltage		V_{IN} = AINP – AINN		$\pm V_{REF}/2$		V
Absolute input range	AINP or AINN		AVSS – 0.1		AVDD + 0.1	V
Differential input impedance				55		kΩ
AC PERFORMANCE						
Signal-to-noise ratio(2)	SNR	f_{DATA} = 250SPS		130		dB
		f_{DATA} = 500SPS		127		
		f_{DATA} = 1000SPS	120	124		
		f_{DATA} = 2000SPS		121		
		f_{DATA} = 4000SPS		118		
Total harmonic distortion	THD	V_{IN} = 31.25Hz, –0.5dBFS		–122	–115	dB
Spurious-free dynamic range(3)	SFDR			123		dB
DC PERFORMANCE						
Resolution	No missing codes		31			Bits
Data rate	f_{DATA}	FIR filter mode	250		4000	SPS
		Sinc filter mode	8,000		128,000	SPS
Integral nonlinearity(4)	INL	Differential input		0.00006	0.0005	% FSR(5)
Offset error		Shorted input		10	200	μV
Offset error after calibration(6)				1		μV
Offset drift				0.06		μV/°C
Gain error				0.1	0.3	%
Gain error after calibration(6)				0.0002		%
Gain drift				0.4		ppm/°C
Common-mode rejection		f_{CM} = 60Hz	105	120		dB
Power-supply rejection	AVDD, AVSS	f_{PS} = 60Hz	85	95		dB
	DVDD		85	105		
FIR DIGITAL FILTER RESPONSE						
Passband ripple					±0.003	dB
Passband (–0.01dB)				0.375 × f_{DATA}		Hz
Stop band attenuation(7)			135			dB
Stop band				0.500 × f_{DATA}		Hz
Bandwidth (–3dB)				0.413 × f_{DATA}		Hz
Group delay		FIR filter, minimum phase(8)		$5/f_{DATA}$		s
		FIR filter, linear phase		$31/f_{DATA}$		
Settling time (latency)		FIR filter, minimum phase		$62/f_{DATA}$		s
		FIR filter, linear phase		$62/f_{DATA}$		
High-pass filter corner			0.1		10	Hz

(1) f_{CLK} = system clock.
(2) SNR = signal-to-noise ratio = 20 log (V_{RMS} Full-Scale/V_{RMS} Noise), V_{IN} = 20mV_{DC}.
(3) Highest spurious component including harmonics.
(4) Best-fit method.
(5) FSR: Full-scale range = $\pm V_{REF}/2$.
(6) Calibration accuracy is on the level of noise reduced by 4 (calibration averages 16 readings).
(7) Input frequencies in the range of $Nf_{CLK}/512 \pm f_{DATA}/2$ (N = 1, 2, 3...) can mix with the modulator chopping clock. In these frequency ranges intermodulation = 120dB, typ.
(8) At dc; see Figure 32.

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ELECTRICAL CHARACTERISTICS (continued)

Limit specifications at –40°C to +85°C, typical specifications at +25°C, AVDD = +2.5V, AVSS = –2.5V, f_{CLK} (1) = 4.096MHz, VREFP = +2.5V, VREFN = –2.5V, DVDD = +3.3V, and f_{DATA} = 1000SPS, unless otherwise noted.

PARAMETER		CONDITIONS	ADS1281 MIN	ADS1281 TYP	ADS1281 MAX	UNIT
VOLTAGE REFERENCE INPUTS						
Reference input voltage V_{REF} = VREFP – VREFN			0.5	5	(AVDD – AVSS) + 0.2	V
Negative reference input	VREFN		AVSS – 0.1		VREFP – 0.5	V
Positive reference input	VREFP		VREFN + 0.5		AVDD + 0.1	V
Reference input impedance				85		kΩ
DIGITAL INPUT/OUTPUT						
V_{IH}			0.8 × DVDD		DVDD	V
V_{IL}			DGND		0.2 × DVDD	V
V_{OH}		I_{OH} = 1mA	0.8 × DVDD			V
V_{OL}		I_{OL} = 1mA			0.2 × DVDD	V
Input leakage		0 < $V_{DIGITAL\ IN}$ < DVDD			±10	µA
Clock input	f_{CLK}		1		4.096	MHz
POWER SUPPLY						
AVSS			–2.6		0	V
AVDD			AVSS + 4.75		AVSS + 5.25	V
DVDD			1.65		3.6	V
AVDD, AVSS current		Operating mode		2	3	| mA |
		Standby mode		1	15	| µA |
		Power-Down mode		1	15	| µA |
DVDD current		Operating mode		0.6	0.8	mA
		Modulator mode		0.1		mA
		Standby mode		25	50	µA
		Power-Down mode (9)		1	15	µA
Power dissipation		Operating mode		12	18	mW
		Standby mode		90	250	µW
		Power-Down mode		10	150	µW

(9) CLK input stopped.

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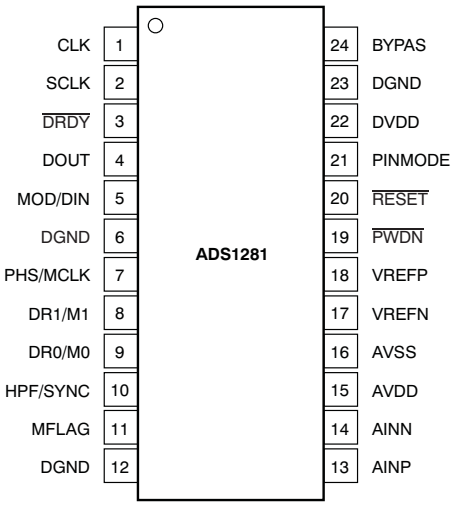
DEVICE INFORMATION

TSSOP-24
Top View



TERMINAL FUNCTIONS

NAME	NO.	FUNCTION	DESCRIPTION	
			PIN MODE (PINMODE = 1)	REGISTER MODE (PINMODE = 0)
CLK	1	Digital input	Master clock input	Master clock input
SCLK	2	Digital input	SPI serial clock input	SPI serial clock input
$\overline{\text{DRDY}}$	3	Digital output	Data ready output: read data on falling edge	Data ready output: read data on falling edge
DOUT	4	Digital output	SPI serial data output	SPI serial data output
MOD/DIN	5	Digital input	MOD: 0 = Digital filter mode 1 = Filter bypass (modulator output)	DIN: SPI serial data input
PHS/MCLK	7	Digital I/O	(MOD = 0) PHS: 0 = Linear phase filter, 1 = Minimum phase filter (MOD = 1) MCLK: Modulator clock output	If in modulator mode: MCLK: Modulator clock output Otherwise, the pin is an unused input (must be tied).
DR1/M1	8	Digital I/O	(MOD = 0) DR1 = Data rate select input 1 (MOD = 1) M1 = Modulator data output 1	If in modulator mode: M1: Modulator data output 1 Otherwise, the pin is an unused input (must be tied).
DR0/M0	9	Digital I/O	(MOD = 0) DR0 = Data rate select input 0 (MOD = 1) M0 = Modulator data output 0	If in modulator mode: M0: Modulator data output 0 Otherwise, the pin is an unused input (must be tied).
HPF/SYNC	10	Digital input	(MOD = 0) HPF: 0 = High-pass filter off, 1 = HPF on (MOD = 1) SYNC = Synchronize Input	SYNC: Synchronize input
MFLAG	11	Digital output	Modulator over-range flag: 0 = Normal, 1 = Modulator over-range	Modulator over-range flag: 0 = Normal, 1 = Modulator over-range
DGND	6, 12, 23	Digital ground	Digital ground, pin 12 is the key ground point	Digital ground, pin 12 is the key ground point
AINP	13	Analog input	Positive analog input	Positive analog input
AINN	14	Analog input	Negative analog input	Negative analog input
AVDD	15	Analog supply	Positive analog power supply	Positive analog power supply
AVSS	16	Analog supply	Negative analog power supply	Negative analog power supply
VREFN	17	Analog input	Negative reference input	Negative reference input
VREFP	18	Analog input	Positive reference input	Positive reference input
$\overline{\text{PWDN}}$	19	Digital input	Power-down input, active low	Power-down input, active low
$\overline{\text{RESET}}$	20	Digital input	Synchronize input	Reset input
PINMODE	21	Digital input	1 = Pin mode	0 = Register mode
DVDD	22	Digital supply	Digital power supply: +1.8V to +3.3V	Digital power supply: +1.8V to +3.3V
BYPAS	24	Capacitor bypass	Digital core bypass; 1μF bypass capacitor to GND	Digital core bypass; 1μF bypass capacitor to GND

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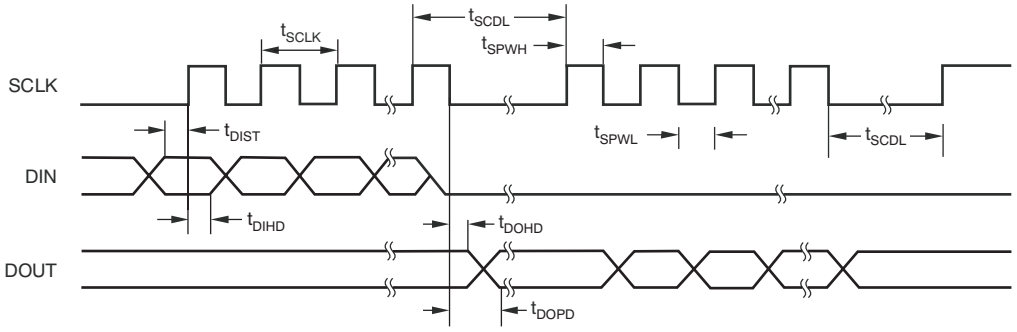
TIMING DIAGRAM



TIMING REQUIREMENTS

At T_A = –40°C to +85°C and DVDD = 1.65V to 3.6V, unless otherwise noted.

PARAMETER	DESCRIPTION	MIN	MAX	UNITS
t_{SCLK}	SCLK period	2	16	$1/f_{CLK}$
$t_{SPWH, L}$	SCLK pulse width, high and low(1)	0.8	10	$1/f_{CLK}$
t_{DIST}	DIN valid to SCLK rising edge: setup time	50		ns
t_{DIHD}	Valid DIN to SCLK rising edge: hold time	50		ns
t_{DOPD}	SCLK falling edge to valid new DOUT: propagation delay(2)		100	ns
t_{DOHD}	SCLK falling edge to DOUT invalid: hold time	0		ns
t_{SCDL}	Final SCLK rising edge of command to first SCLK rising edge for register read/write data. (Also between consecutive commands.)	24		$1/f_{CLK}$

(1) Holding SCLK low for 64 $\overline{DRDY}$ falling edges resets the SPI interface.
(2) Load on DOUT = 20pF || 100kΩ.

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TYPICAL CHARACTERISTICS

At T_A = +25°C, AVDD = +2.5V, AVSS = –2.5V, f_{CLK} = 4.096MHz, VREFP = +2.5V, VREFN = –2.5V, DVDD = +3.3V, and f_{DATA} = 1000SPS, unless otherwise noted.

OUTPUT SPECTRUM

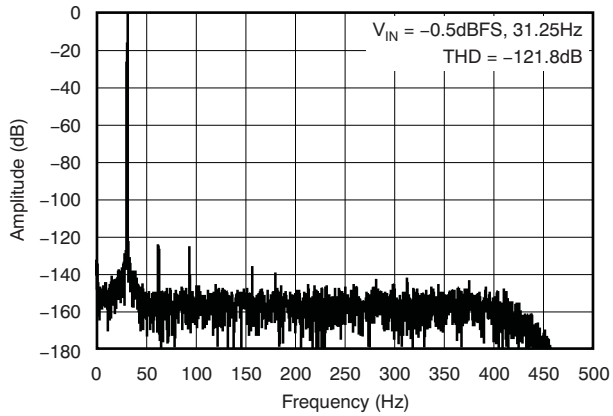

Figure 1.

OUTPUT SPECTRUM

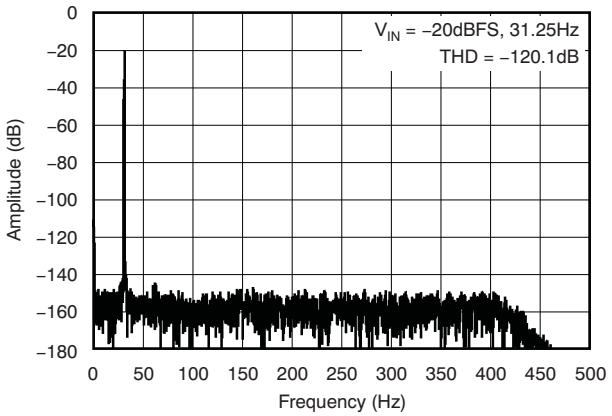

Figure 2.

OUTPUT SPECTRUM

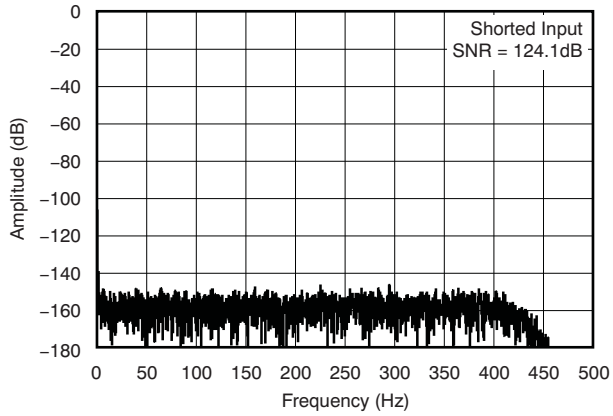

Figure 3.

OUTPUT SPECTRUM

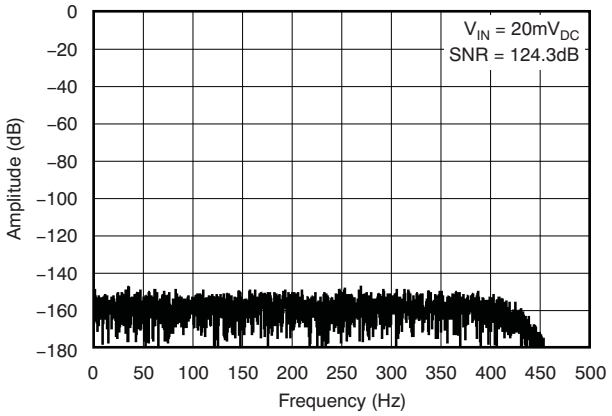

Figure 4.

THD vs INPUT FREQUENCY

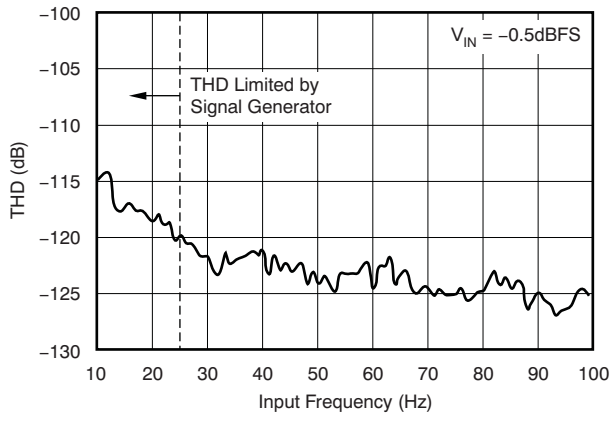

Figure 5.

SNR HISTOGRAM

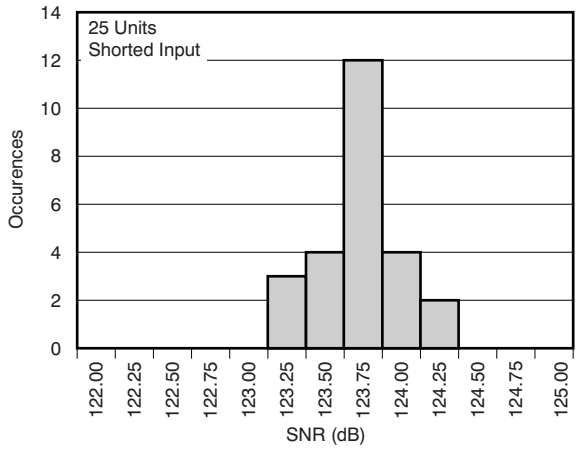

Figure 6.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AVDD = +2.5V, AVSS = –2.5V, f_{CLK} = 4.096MHz, VREFP = +2.5V, VREFN = –2.5V, DVDD = +3.3V, and f_{DATA} = 1000SPS, unless otherwise noted.

SNR AND THD vs TEMPERATURE

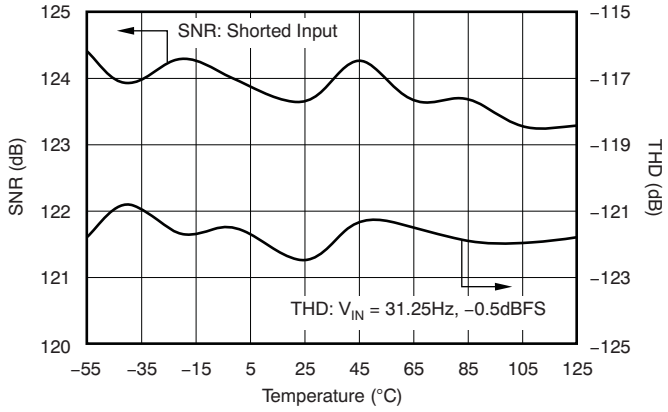

Figure 7.

NOISE AND THD vs V_{REF}

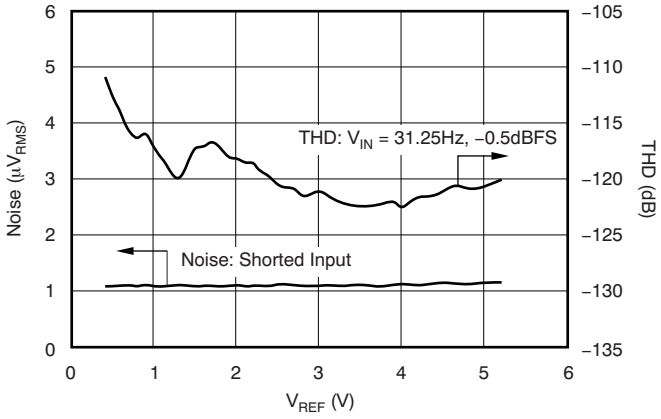

Figure 8.

SNR AND THD vs f_{CLK}

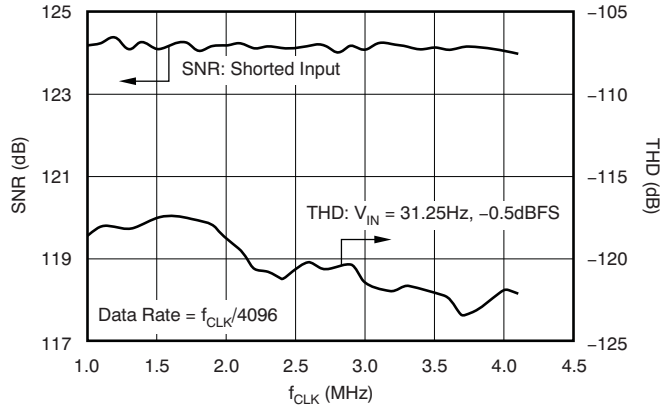

Figure 9.

POWER-SUPPLY AND COMMON-MODE REJECTION vs FREQUENCY

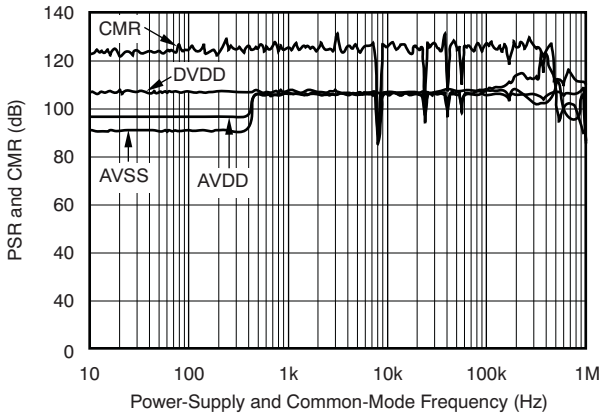

Figure 10.

LINEARITY ERROR vs INPUT LEVEL

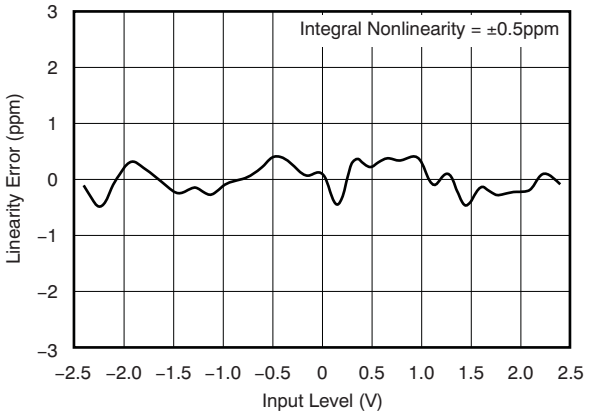

Figure 11.

INL AND POWER vs TEMPERATURE

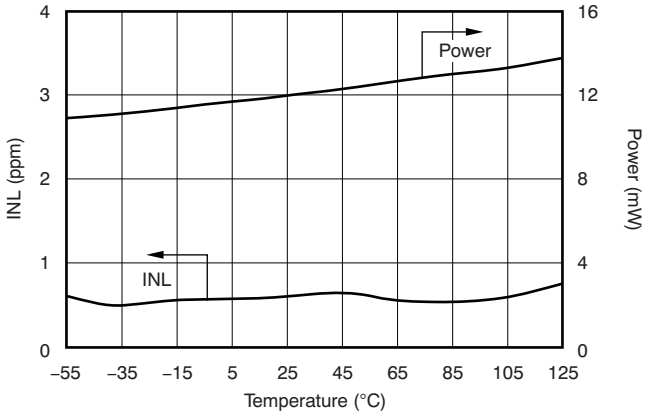

Figure 12.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AVDD = +2.5V, AVSS = –2.5V, f_{CLK} = 4.096MHz, VREFP = +2.5V, VREFN = –2.5V, DVDD = +3.3V, and f_{DATA} = 1000SPS, unless otherwise noted.

POWER vs f_{CLK}

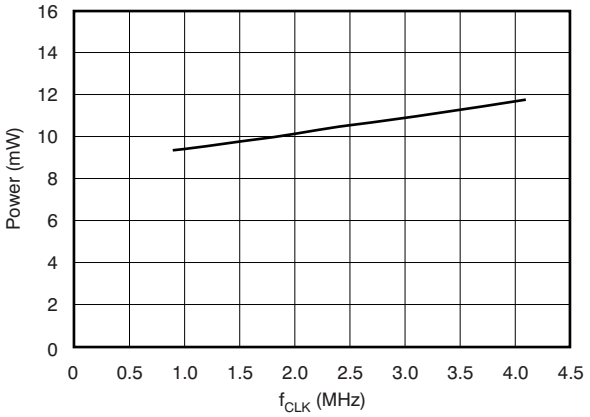

Figure 13.

GAIN AND OFFSET vs TEMPERATURE

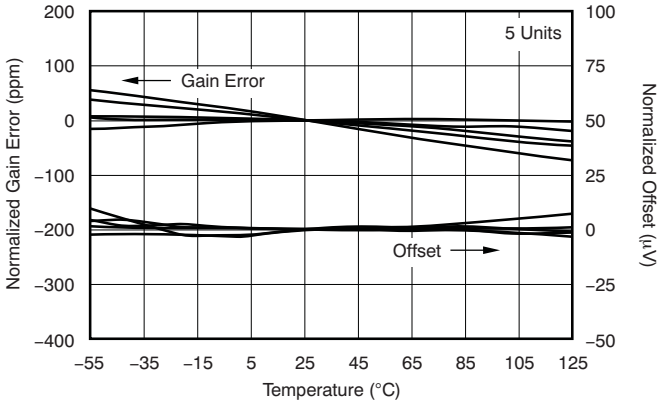

Figure 14.

OFFSET HISTOGRAM

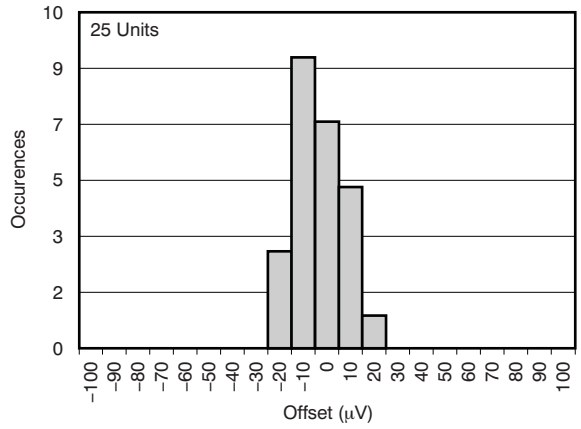

Figure 15.

GAIN ERROR HISTOGRAM

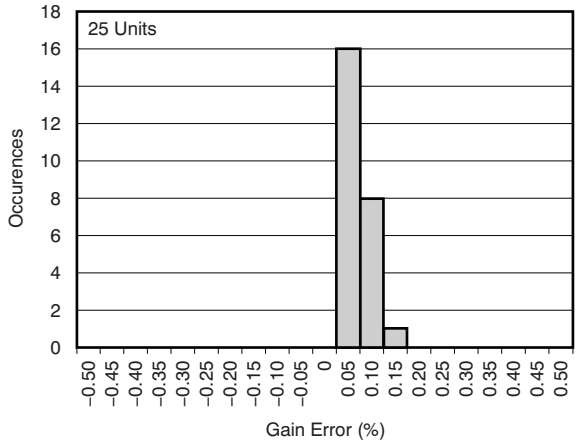

Figure 16.

OFFSET DRIFT HISTOGRAM

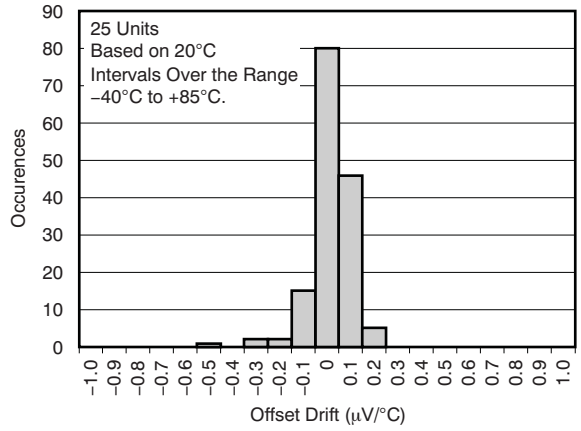

Figure 17.

GAIN DRIFT HISTOGRAM

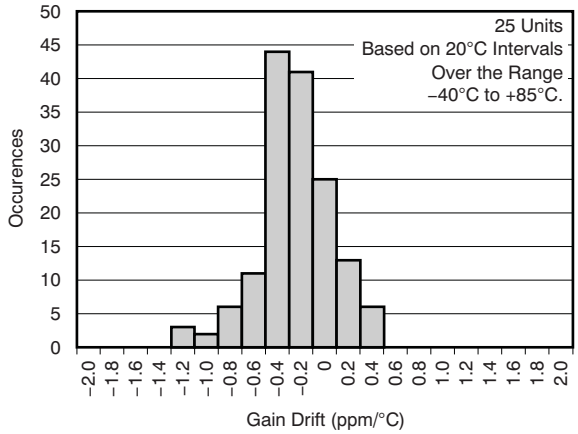

Figure 18.

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OVERVIEW

The ADS1281 is a high-performance analog-to-digital converter (ADC) intended for energy exploration, seismic monitoring, chromatography, and other exacting applications. The converter provides 24- or 32-bit output data in data rates from 4000SPS to 250SPS.

Figure 19 shows the block diagram of the ADS1281. The device features unipolar and bipolar analog power supplies (AVDD and AVSS, respectively) for input range flexibility and a digital supply accepting 1.8V to 3.3V. The analog supplies may be set to +5V to accept unipolar signals (with input offset) or set lower in the range of ±2.5V to accept true bipolar input signals (ground referenced).

An internal low-dropout (LDO) regulator is used to power the digital core from DVDD. The BYPAS pin is the LDO output and requires a 0.1μF capacitor for noise reduction (BYPAS should not be used to drive external circuitry).

The inherently-stable, fourth-order, ΔΣ modulator measures the differential input signal V_{IN} = (AINP – AINN) against the differential reference V_{REF} = (VREFP – VREFN). A digital output (MFLAG) indicates that the modulator is in over-range resulting from an input overdrive condition. The modulator output is available directly on the MCLK, M0, and M1 output pins. The modulator connects to an on-chip digital filter that provides the output code readings.

The digital filter is comprised of a variable decimation rate, fifth-order sinc filter followed by a decimate-by-32, FIR low-pass filter with programmable phase, and then by an adjustable high-pass filter for dc removal of the output reading. The output of the digital filter can be taken from the sinc, the FIR low-pass, or the IIR high-pass section.

Gain and offset registers scale the digital filter output to produce the final code value. The scaling feature can be used for calibration and sensor gain matching. The output data are provided with either a 24-bit word or a full 32-bit word, allowing full utilization of the inherently high resolution.

The PINMODE input pin determines the mode of the device: Pin control or Register control. In Pin control mode, the device is controlled by simple pin settings; there are no registers to program. In Register control mode, the device is controlled by register settings. The functionality of several device pins depends on the control mode selected (see the *Pin and Register Modes* section).

The SYNC input resets the operation of both the digital filter and the modulator, allowing synchronized conversions of multiple ADS1281 devices to an external event. The SYNC input supports a continuously-toggled input mode that accepts an external data frame clock locked to an integer of the conversion rate.

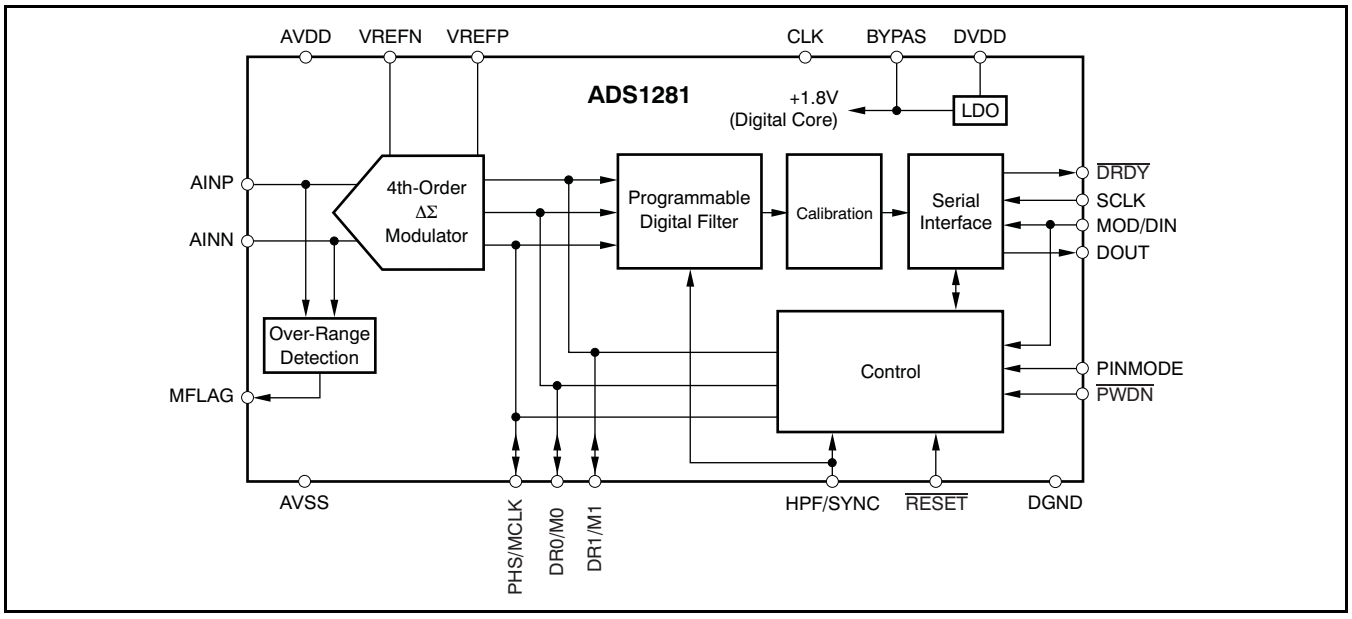

Figure 19. ADS1281 Block Diagram

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The $\overline{\text{RESET}}$ input resets the register settings (Register mode) and also restarts the conversion process.

The $\overline{\text{PWDN}}$ input sets the device into a micro-power state. Note that register settings are not retained in $\overline{\text{PWDN}}$ mode. Use the STANDBY command in its place if it is desired to retain register settings (the quiescent current in the Standby mode is slightly higher).

Noise-immune Schmitt-trigger and clock-qualified inputs ($\overline{\text{RESET}}$ and SYNC) provide increased reliability in high-noise environments.

The serial interface is used to read conversion data, in addition to reading from and writing to the configuration registers.

NOISE PERFORMANCE

The ADS1281 offers outstanding noise performance. Table 1 summarizes the SNR performance.

Table 1. Noise Performance (Typical)(1)

DATA RATE	FILTER	–3dB BW (Hz)	SNR (dB)
250	FIR	103	130
500	FIR	206	127
1000	FIR	413	124
2000	FIR	826	121
4000	FIR	1652	118

(1) $V_{IN} = 20mV_{DC}$.

IDLE TONES

The ADS1281 modulator incorporates an internal dither signal that randomizes the idle tone energy. Low-level idle tones may still be present, typically –137dB below full-scale. The low-level idle tones can be shifted out of the passband with the application of an external 20mV offset.

ADC

The ADC block of the ADS1281 is composed of two blocks: a high-accuracy modulator and a programmable digital filter.

MODULATOR

The high-performance modulator is an inherently-stable, fourth-order, ΔΣ, 2 + 2 pipelined structure, as shown in Figure 20. It shifts the quantization noise to a higher frequency (out of the passband) where digital filtering can easily remove it. The modulator can be filtered either by the on-chip digital filter or by use of post-processing filters.

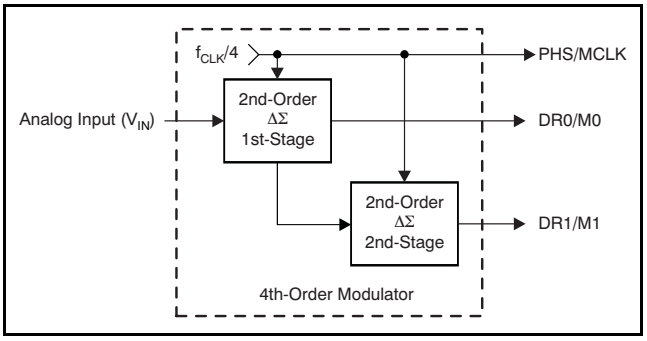

Figure 20. Fourth-Order Modulator

The modulator first stage converts the analog input voltage into a pulse-code modulated (PCM) stream. When the level of differential analog input (AINP – AINN) is near one-half the level of the reference voltage 1/2 × (VREFP – VREFN), the '1' density of the PCM data stream is at its highest. When the level of the differential analog input is near zero, the PCM '0' and '1' densities are nearly equal. At the two extremes of the analog input levels (+FS and –FS), the '1' density of the PCM streams are approximately +90% and +10%, respectively.

The modulator second stage produces a '1' density data stream designed to cancel the quantization noise of the first stage. The data streams of the two stages are then combined before input to the digital filter stage, as shown in Equation 1.

$$Y[n] = 3M0[n-2] - 6M0[n-3] + 4M0[n-4] + 9(M1[n] - 2M1[n-1] + M1[n-2]) \quad (1)$$

M0[n] represents the most recent first-stage output while M0[n – 1] is the previous first-stage output. When the modulator output is enabled, the digital filter shuts down to save power.

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The modulator is optimized for input signals within a 4kHz passband. As Figure 21 shows, the noise shaping of the modulator results in a sharp increase in noise above 6kHz. The modulator has a chopped input structure that further reduces noise within the passband. The noise is moved out of the passband and appears at the chopping frequency (f_{CLK}/512 = 8kHz). The component at 6.5kHz is the tone frequency, shifted out of band by a 20mV offset. The frequency of the tone is proportional to the applied dc input and is given by V_{IN}/0.003 (in kHz).

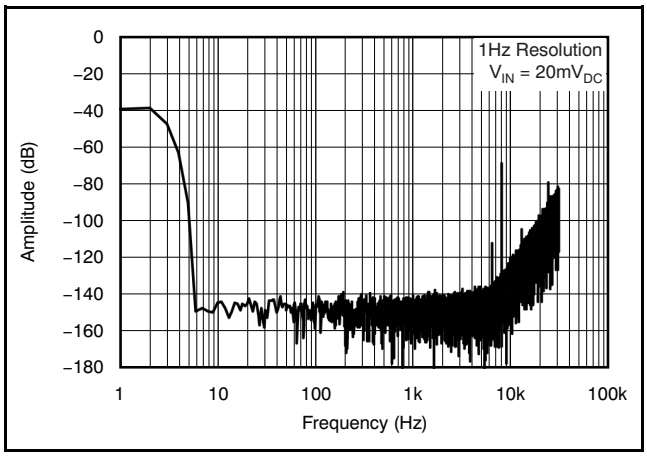

Figure 21. Modulator Output Spectrum

MODULATOR OVER-RANGE

The ADS1281 modulator is inherently stable and, therefore, has predictable recovery behavior that results from an input overdrive condition. The modulator does not exhibit self-resetting behavior, which often results in an unstable output data stream.

The ADS1281 modulator outputs a 1s density data stream at 90% duty cycle with the positive full-scale input signal applied (10% duty cycle with the negative full-scale signal). If the input is overdriven past 90% modulation, but below 100% modulation (10% and 0% for negative overdrive, respectively), the modulator remains stable and continues to output the 1s density data stream. The digital filter may or may not clip the output codes to +FS or –FS, depending on the duration of the overdrive. When the input is returned to the normal range from a long duration overdrive (worst case), the modulator returns immediately to the normal range, but the group delay of the digital filter delays the return of the conversion result to within the linear range (31 readings for linear phase FIR). 31 additional readings (62 total) are required for completely settled data.

If the inputs are sufficiently overdriven to drive the modulator to full duty cycle, all 1s or all 0s, the modulator enters a stable saturated state. The digital output code may clip to +FS or –FS, again depending on the duration. A small duration overdrive may not always clip the output code. When the input returns to the normal range, the modulator requires up to 12 modulator clock cycles (f_{MOD}) to exit saturation and return to the linear region. The digital filter requires an additional 62 conversion for fully settled data (linear phase FIR).

In the extreme case of over-range, either input is overdriven exceeding that either analog supply voltage plus an internal ESD diode drop. The internal ESD diodes begin to conduct and the signal on the input is clipped. If the differential input signal range is not exceeded, the modulator remains in linear operation. If the differential input signal range is exceeded, the modulator is saturated but stable, and outputs all 1s or 0s. When the input overdrive is removed, the diodes recovery quickly and the ADS1281 recovers as normal. Note that the linear input range is ±100mV beyond the analog supply voltages; with input levels above this, use care to limit the input current to 100mA peak transient and 10mA continuous.

MODULATOR OVER-RANGE DETECTION (MFLAG)

The ADS1281 has a fast-responding over-range detection, indicating when the differential input exceeds approximately +100% or –100% full-scale. The threshold tolerance is ±2.5%.The MFLAG output asserts high when in an over-range condition. As Figure 22 and Figure 23 illustrate, the absolute value of the input is compared to 100% of range. The output of the comparator is sampled at the rate of f_{MOD}/2, yielding the MFLAG output. The minimum MFLAG pulse width is f_{MOD}/2.

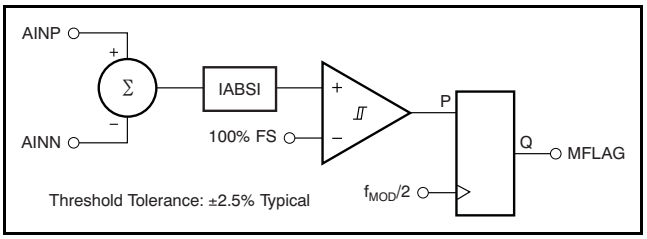

Figure 22. Modulator Over-Range Block Diagram

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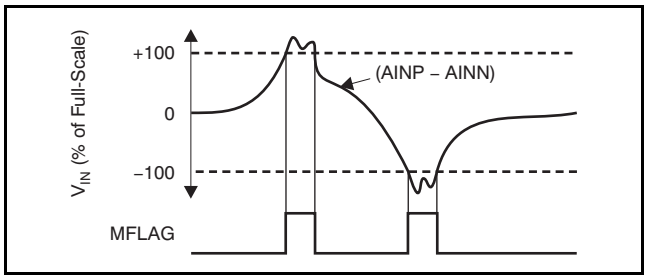

Figure 23. Modulator Over-Range Flag Operation

MODULATOR OUTPUT MODE

The modulator digital stream output is available directly, bypassing and disabling the internal digital filter. The modulator output mode is activated in the Pin mode by setting MOD/DIN = 1, and in Register mode by setting the CONFIG0 register bits FILTR[1:0] = 00. Pins DR0/M0 and DR1/M1 then become the modulator data outputs and the PHS/MCLK becomes the modulator clock output. When not in the modulator mode, these pins are inputs and must not float.

The modulator output is composed of three signals: one output for the modulator clock (PHS/MCLK) and two outputs for the modulator data (DR0/M0 and DR1/M1). The modulator clock output rate is f_{MOD} (f_{CLK}/4). Synchronization resets the MODCLK phase, as shown in Figure 24. The SYNC input is latched on the rising edge of CLK. The MODCLK resets and the next rising edge of MODCLK occurs three CLK periods later, as shown in Figure 24.

The modulator output data are two bits wide, which must be merged together before being filtered. Use the time domain equation of Equation 1 to merge the data outputs.

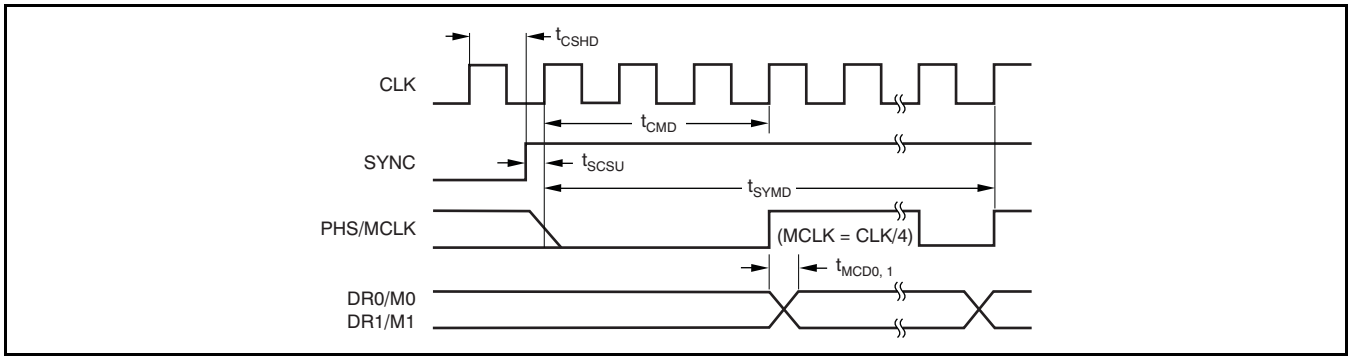

Figure 24. Modulator Mode Timing

Table 2. Modulator Output Timing for Figure 24

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
$t_{MCD0, 1}$	MODCLK rising edge to M0, M1 valid propagation delay(1)			100	ns
t_{CMD}	CLK rising edge to MODCLK rising edge reset time after synchronization		3		$1/f_{CLK}$
t_{CSHD}	CLK to SYNC hold time to not latch on CLK edge	10			ns
t_{SCSU}	SYNC to CLK setup time to latch on CLK edge	10			ns
t_{SYMD}	SYNC to stable bit stream			16	$1/f_{MOD}$

(1) Load on M0 and M1 = 20pF || 100kΩ.

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DIGITAL FILTER

The digital filter receives the modulator output and decimates the data stream. By adjusting the amount of filtering, tradeoffs can be made between resolution and data rate: filter more for higher resolution, filter less for higher data rate.

The digital filter is comprised of three cascaded filter stages: a variable-decimation, fifth-order sinc filter; a fixed-decimation FIR, low-pass filter (LPF) with selectable phase; and a programmable, first-order, high-pass filter (HPF), as shown in Figure 25.

The output can be taken from one of the three filter blocks, as shown in Figure 25. To implement the digital filter completely off-chip, select the filter bypass setting (modulator output). For partial filtering by the ADS1281, select the sinc filter output. For complete on-chip filtering, activate both the sinc and FIR stages. The HPF can then be included to remove dc and low frequencies from the data. Table 3 shows the filter options in Register mode. Table 4 shows the filter options in Pin mode.

Table 3. Digital Filter Selection, Register Mode

FILTR[1:0] BITS	DIGITAL FILTERS SELECTED
00	Bypass; modulator output mode
01	Sinc
10	Sinc + FIR
11	Sinc + FIR + HPF (low-pass and high-pass)

Table 4. Digital Filter Selection, Pin Mode

MOD/DIN PIN	HPF/SYNC PIN	DIGITAL FILTERS SELECTED
1	X	Bypass; modulator output mode
0	0	Sinc + FIR
0	1	Sinc + FIR + HPF (low-pass and high-pass)

Sinc Filter Stage (sinx/x)

The sinc filter is a variable decimation rate, fifth-order, low-pass filter. Data are supplied to this section of the filter from the modulator at the rate of f_{MOD} (f_{CLK}/4). The sinc filter attenuates the high-frequency noise of the modulator, then decimates the data stream into parallel data. The decimation rate affects the overall data rate of the converter; it is set by the DR[1:0] and MODE selections, as shown in Table 5.

Equation 2 shows the scaled Z-domain transfer function of the sinc filter.

$$H(Z) = \left[\frac{1 - Z^{-N}}{N(1 - Z^{-1})} \right]^5 \quad (2)$$

Where:

N = decimation ratio

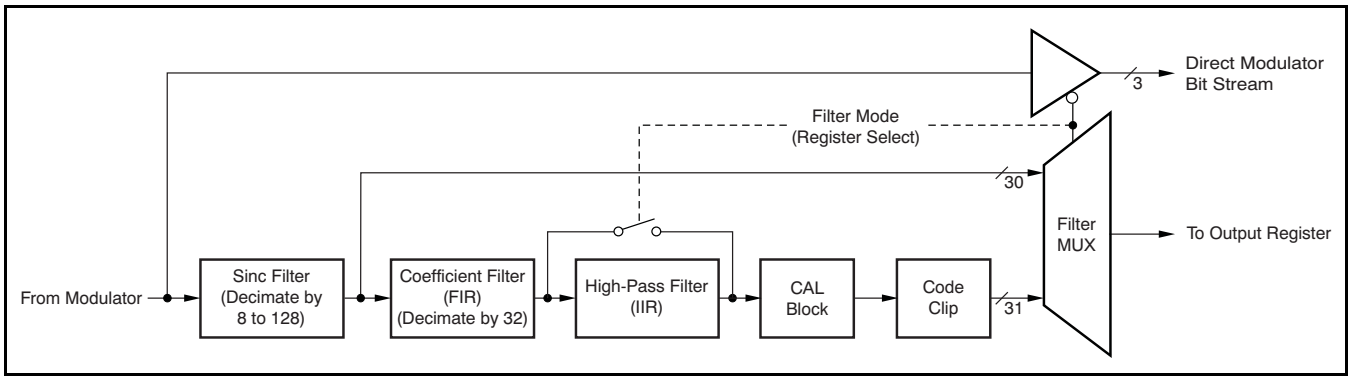

Figure 25. Digital Filter and Output Code Processing

Table 5. Sinc Filter Data Rates (CLK = 4.096MHz)

DR[1:0] PINS	DR[2:0] REGISTER	DECIMATION RATIO (N)	SINC DATA RATE (SPS)
00	000	128	8,000
01	001	64	16,000
10	010	32	32,000
11	011	16	64,000
—	100	8	128,000

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The frequency domain transfer function of the sinc filter is shown in Equation 3.

$$|H(f)| = \left| \frac{\sin\left(\frac{\pi N \times f}{f_{MOD}}\right)}{N \sin\left(\frac{\pi \times f}{f_{MOD}}\right)} \right|^5 \quad (3)$$

where:

N = decimation ratio (see Table 5)

The sinc filter has notches (or zeroes) that occur at the output data rate and multiples thereof. At these frequencies, the filter has zero gain. Figure 26 shows the frequency response of the sinc filter and Figure 27 shows the roll-off of the sinc filter.

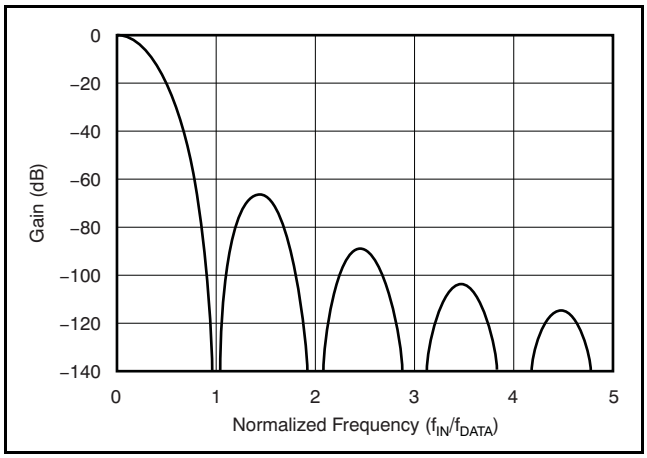

Figure 26. Sinc Filter Frequency Response

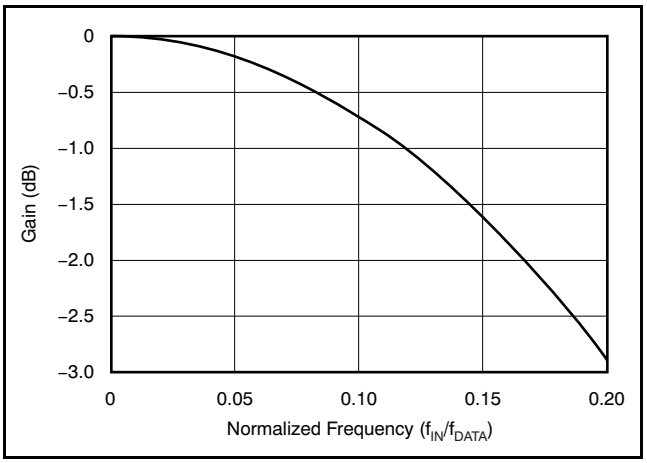

Figure 27. Sinc Filter Roll-Off

FIR Stage

The second stage of the ADS1281 digital filter is an FIR low-pass filter. Data are supplied to this stage from the sinc filter. The FIR stage is segmented into four sub-stages, as shown in Figure 28. The first two sub-stages are half-band filters with decimation ratios of 2. The third sub-stage decimates by 4 and the fourth sub-stage decimates by 2. The overall decimation of the FIR stage is 32. Note that two coefficient sets are used for the third and fourth sections, depending on the phase selection. Table 24 in the Appendix section at the end of this document lists the FIR stage coefficients. Table 6 lists the data rates and overall decimation ratio of the FIR stage.

Table 6. FIR Filter Data Rates

DR[1:0] PINS	DR[2:0] REGISTER	DECIMATION RATIO (N)	FIR DATA RATE (SPS)
00	000	4096	250
01	001	2048	500
10	010	1024	1000
11	011	512	2000
—	100	256	4000

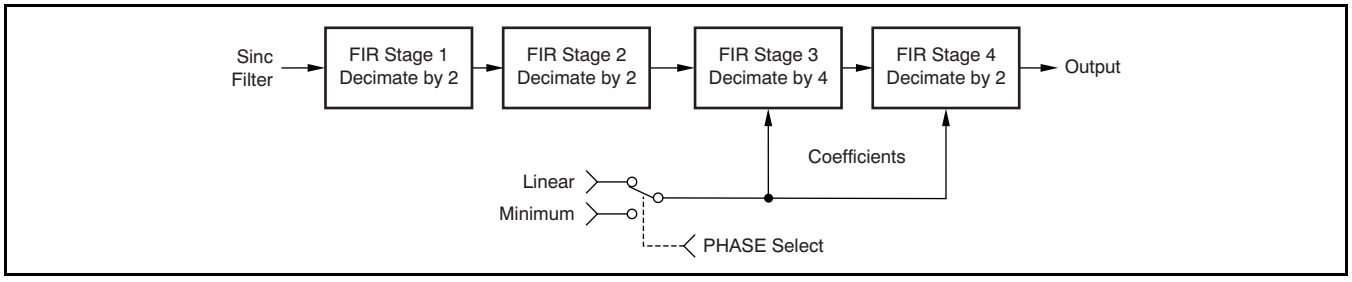

Figure 28. FIR Filter Sub-Stages

As shown in Figure 29, the FIR frequency response provides a flat passband to 0.375 of the data rate (±0.003dB passband ripple). Figure 30 shows the transition from passband to stop band.

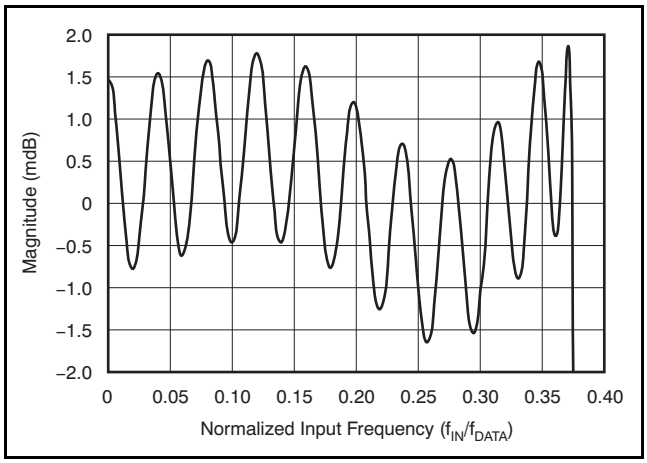

Figure 29. FIR Passband Response (f_{DATA} = 500Hz)

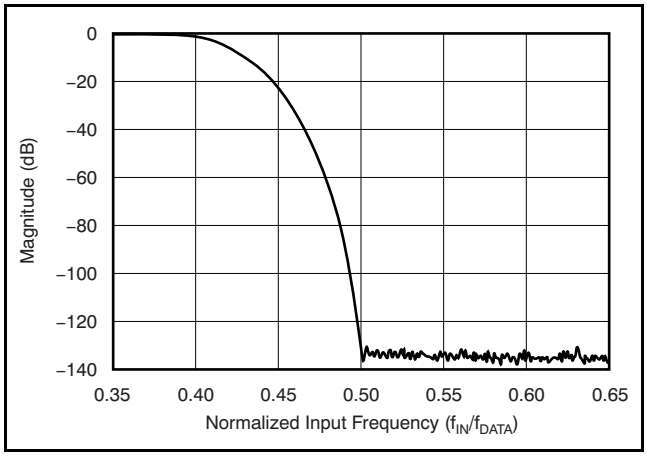

Figure 30. FIR Transition Band Response

Although not shown in Figure 30, the passband response repeats at multiples of the modulator frequency ($Nf_{MOD} – f_0$ and $Nf_{MOD} + f_0$, where N = 1, 2, etc. and f_0 = passband). These image frequencies, if present in the signal and not externally filtered, fold back (or alias) into the passband and cause errors. Placing an anti-alias, low-pass filter in front of the ADS1281 inputs is recommended to limit possible out-of-band input signals. Often, a single RC filter is sufficient.

GROUP DELAY AND STEP RESPONSE

The FIR block is implemented as a multi-stage FIR structure with selectable linear or minimum phase response. The passband, transition band, and stop band responses of the filters are nearly identical but differ in the respective phase responses.

Linear Phase Response

Linear phase filters exhibit constant delay time versus input frequency (that is, constant group delay). Linear phase filters have the property that the time delay from any instant of the input signal to the same instant of the output data is constant and is independent of the signal nature. This filter behavior results in essentially zero phase error when analyzing multi-tone signals. However, the group delay and settling time of the linear phase filter are somewhat larger than the minimum phase filter, as shown in Figure 31.

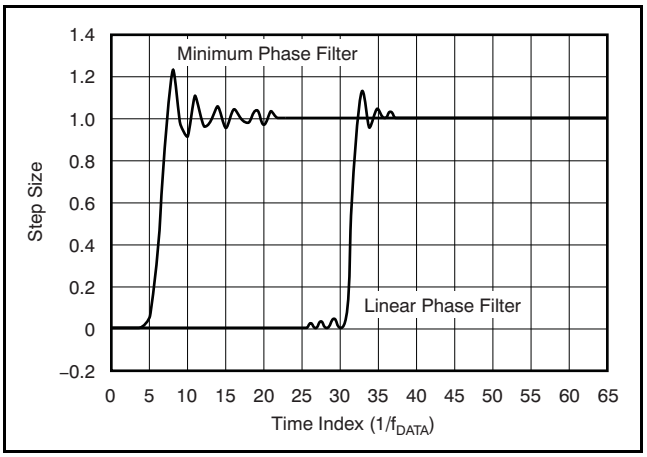

Figure 31. FIR Step Response

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Minimum Phase Response

The minimum phase filter provides a short delay from the arrival of an input signal to the output, but the relationship (phase) is not constant versus frequency, as shown in Figure 32. The filter phase is selected by the PHS bit (Register mode) or the PHS/MCLK pin (Pin mode); Table 7 shows additional information.

Table 7. FIR Phase Selection

PHS BIT or PHS/MCLK PIN	FILTER PHASE
0	Linear
1	Minimum

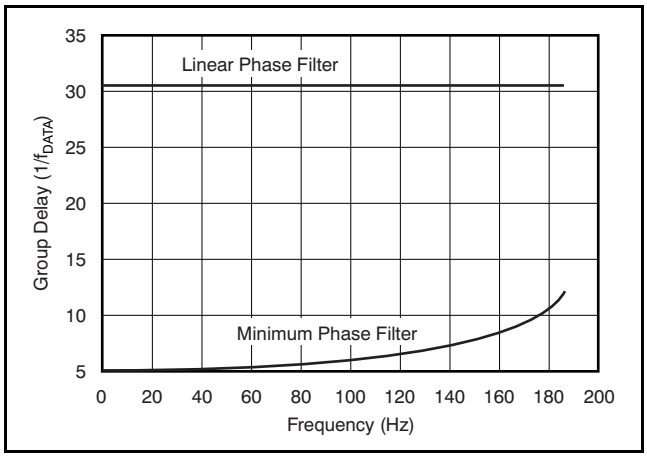

Figure 32. FIR Group Delay (f_{DATA} = 500Hz)

HPF Stage

The last stage of the ADS1281 filter block is a first-order HPF implemented as an IIR structure. This filter stage blocks dc signals and rolls off low-frequency components below the cut-off frequency. The transfer function for the filter is shown in Equation 12 of the *Appendix*.

The high-pass corner frequency is programmed by registers HPF[1:0], in hexadecimal. Equation 4 is used to set the high-pass corner frequency. Table 8 lists example values for the high-pass filter.

$$HPF[dec] = 65{,}536 \left[1 - \sqrt{1 - 2\,\frac{\cos \omega_N + \sin \omega_N - 1}{\cos \omega_N}} \right] \quad (4)$$

Where:

HPF = High-pass filter register value (converted to hexadecimal)

$\omega_N = 2\pi f_{HP}/f_{DATA}$ (normalized frequency, radians)

f_{HP} = High-pass corner frequency (Hz)

f_{DATA} = Data rate (Hz)

Table 8. High-Pass Filter Value Examples(1)

f_{HP} (Hz)	DATA RATE (SPS)	HPF[1:0]
0.5	250	0337h
1.0	500	0337h
1.0	1000	019Ah

(1) In Pin Control mode the HPF value is fixed at 0332h.

The HPF causes a small gain error, in which case the magnitude depends on the ratio of f_{HP}/f_{DATA}. For many common values of (f_{HP}/f_{DATA}), the gain error is negligible. Figure 33 shows the gain error of the HPF. The gain error factor is illustrated in Equation 11 (see the *Appendix* at the end of this document).

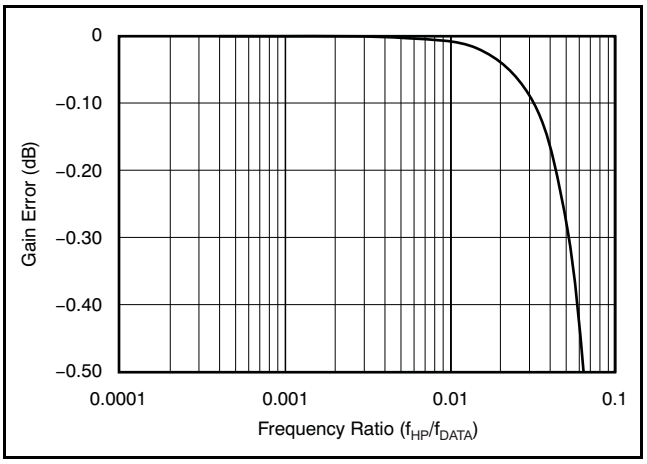

Figure 33. HPF Gain Error

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Figure 34 shows the first-order amplitude and phase response of the HPF. Note that in the case of applying step inputs or synchronizing, the settling time of the filter should be taken into account.

ANALOG INPUT CIRCUITRY (AINP, AINN)

The ADS1281 measures the differential input signal V_{IN} = (AINP – AINN) against the differential reference V_{REF} = (VREFP – VREFN) using internal capacitors that are continuously charged and discharged. Figure 36 shows the simplified schematic of the ADC input circuitry; the right side of the figure illustrates the input circuitry with the capacitors and switches replaced by an equivalent circuit. Figure 35 demonstrates the ON/OFF timings for the switches of Figure 36.

In Figure 36, S_1 switches close during the input sampling phase. With switch S_1 closed, C_{A1} charges to AINP, C_{A2} charges to AINN, and C_B charges to (AINP – AINN). For the discharge phase, S_1 opens first and then S_2 closes. C_{A1} and C_{A2} discharge to approximately to AVSS + 2.5V and C_B discharges to 0V. This two-phase sample/discharge cycle repeats with a period of $t_{SAMPLE} = 1/f_{MOD}$. f_{MOD} is the operating frequency of the modulator. See the *Master Clock Input (CLK)* section.

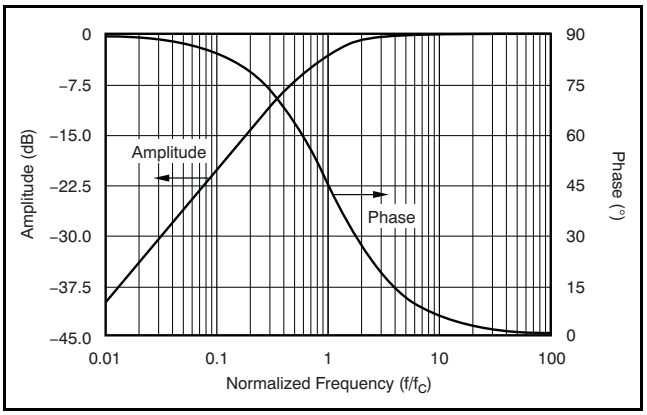

Figure 34. HPF Amplitude and Phase Response

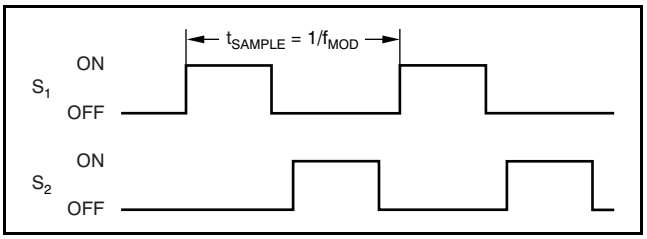

Figure 35. S_1 and S_2 Switch Timing for Figure 36

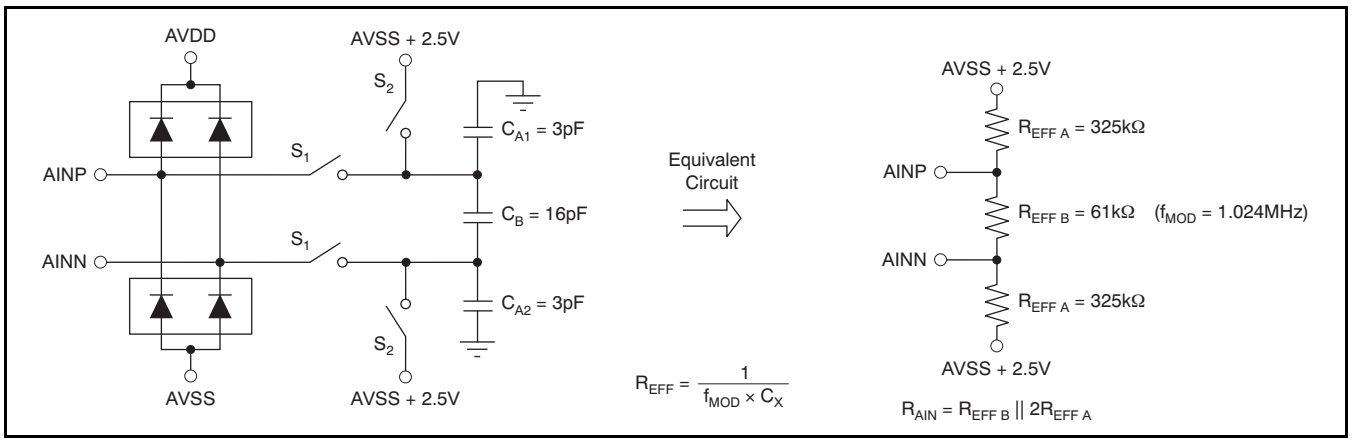

Figure 36. Simplified ADC Input Structure

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The charging of the input sampling capacitors draws a transient current from the source driving the ADS1281 ADC inputs. The average value of this current can be used to calculate an effective impedance (R_{EFF}) where $R_{EFF} = V_{IN}/I_{AVERAGE}$. These impedances scale inversely with f_{MOD}. For example, if f_{MOD} is reduced by a factor of two, the impedances double.

ESD diodes protect the analog inputs. To keep these diodes from turning on, make sure the voltages on the input pins do not go below AVSS by more than 300mV, and likewise do not exceed AVDD by more than 300mV, as shown in Equation 5.

$$AVSS - 300mV < (AINP \text{ or } AINN) < AVDD + 300mV \quad (5)$$

Some applications of the device may require external clamp diodes and/or series resistors to limit the input voltage to within this range.

The ADS1281 is a very high-performance ADC. For optimum performance, it is essential that the ADS1281 inputs be driven with a buffer with noise and distortion commensurate with the ADS1281 performance; see the *Applications* section. Most applications require an external capacitor (C0G/NPO dielectric) directly across the input pins. Depending on the input driver settling characteristics, some experimentation may be necessary to optimize the value to minimize THD (generally 10nF). Best performance is achieved with the common-mode signal centered at mid-supply.

Although optimized for differential signals, the ADS1281 inputs may be driven with a single-ended signal by fixing one input to mid-supply. To take advantage of the full dynamic range, the driven input should swing $5V_{PP}$ for $V_{REF} = 5V$.

VOLTAGE REFERENCE INPUTS (VREFP, VREFN)

The voltage reference for the ADS1281 ADC is the differential voltage between VREFP and VREFN: V_{REF} = VREFP – VREFN. The reference inputs use a structure similar to that of the analog inputs with the circuitry on the reference inputs shown in Figure 37. The average load presented by the switched capacitor reference input can be modeled with an effective differential impedance of $R_{EFF} = t_{SAMPLE}/C_{IN}$ ($t_{SAMPLE} = 1/f_{MOD}$). Note that the effective impedance of the reference inputs loads an external reference with non-zero source impedance.

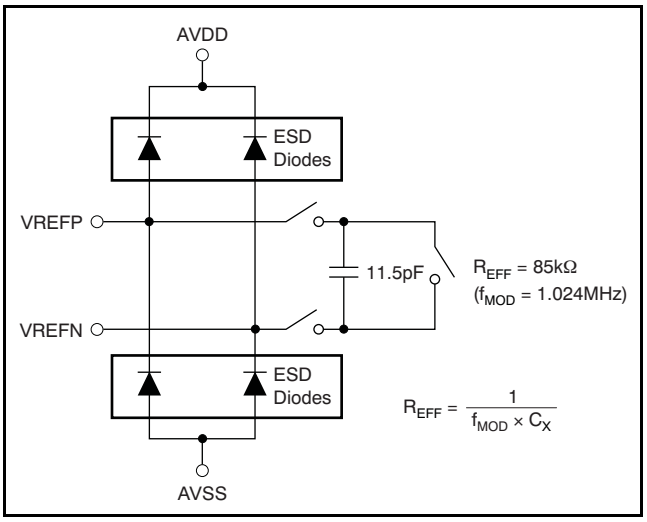

Figure 37. Simplified Reference Input Circuit

The ADS1281 reference inputs are protected by ESD diodes. In order to prevent these diodes from turning on, the voltage on either input must stay within the range shown in Equation 6:

$$AVSS - 300mV < (VREFP \text{ or } VREFN) < AVDD + 300mV \quad (6)$$

A high-quality reference voltage is necessary for achieving the best performance from the ADS1281. Noise and drift on the reference degrade overall system performance, and it is critical that special care be given to the circuitry generating the reference voltages in order to achieve full performance. For most applications, a 1μF ceramic capacitor applied directly to the reference inputs pins is suggested.

MASTER CLOCK INPUT (CLK)

The ADS1281 requires a clock input for operation. The clock is applied to the CLK pin. The data conversion rate scales directly with the CLK frequency. Power consumption versus CLK frequency is relatively constant (see the *Typical Characteristics*).

As with any high-speed data converter, a high-quality, low-jitter clock is essential for optimum performance. Crystal clock oscillators are the recommended clock source. Make sure to avoid excess ringing on the clock input; keep the clock trace as short as possible and use a 50Ω series resistor close to the source.

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PIN AND REGISTER MODES

The PINMODE input (pin 21) is used to set the control mode of the device: Pin mode or Register mode. In Pin mode (PINMODE = 1), control of the device is set by pins; there are no registers to program. In Register mode, control of the device is set by the configuration registers. As a result of the increased flexibility provided by the register space, Register mode has more control options. Table 9 describes the differences between the control modes.

Table 10 summarizes the functions of the dual-purpose pins, depending on the control mode selected.

SYNCHRONIZATION (SYNC PIN AND SYNC COMMAND)

The ADS1281 can be synchronized to an external event, as well as synchronized to other ADS1281 devices if the sync event is applied simultaneously to all devices.

The ADS1281 has two sources for synchronization: the SYNC input pin and the SYNC command. The ADS1281 also has two synchronizing modes: Pulse-sync and Continuous-sync. In Pulse-sync mode, the ADS1281 synchronizes to a single sync event. In Continuous-sync mode, either the device synchronizes to a single sync event or a continuous clock is applied to the pin with a period equal to integer multiples of the data rate. When the periods of the sync input and the $\overline{\text{DRDY}}$ output do not match, the ADS1281 re-synchronizes and conversions are restarted. Note that in Pin control mode, the $\overline{\text{RESET}}$ input serves as the sync control.

Table 9. Functions for Pin Mode and Register Mode

FUNCTION	PIN MODE (PINMODE = 1)	REGISTER MODE (PINMODE = 0)
Synchronization options	Pulse only	Continuous or Pulse
Digital filter options	Sinc + LPF or Sinc + LPF + HPF	Sinc, Sinc + LPF, or Sinc + LPF + HPF
Digital high-pass filter frequency	Fixed low-cut as ratio of f_{DATA}	Programmable
Calibration registers	No	Yes
Interface commands	No	Yes

Table 10. Mode-Dependent Pin Functions

PIN	PIN MODE (PINMODE = 1)	REGISTER MODE (PINMODE = 0)
MOD/DIN	MOD input (select Modulator mode)	SPI DIN input
HPF/SYNC	HPF input (select high-pass filter)	SYNC input
$\overline{\text{RESET}}$	Sync input	Reset input
PHS/MCLK	LPF phase input or MCLK output	MCLK output
DR0/M0	DR0 input or M0 output	M0 output
DR1/M1	DR1 input or M1 output	M1 output

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PULSE-SYNC MODE

In Pulse-sync mode, the ADS1281 stops and restarts the conversion process when a sync event occurs (by pin or command). When the sync event occurs, the device resets the internal memory; DRDY goes high, and after the digital filter has settled, new conversion data are available, as shown in Figure 38 and Table 11.

CONTINUOUS-SYNC MODE

In Continuous-sync mode, either a single sync pulse or a continuous clock may be applied. When a single sync pulse is applied (rising edge), the device behaves similar to the Pulse-sync mode. However, in this mode, DRDY continues to toggle unaffected but the DOUT output is held low until data are ready. When the conversion data are non-zero, new conversion data are ready (as shown in Figure 38).

When a continuous clock is applied to the SYNC pin, the period must be an integral multiple of the output data rate or the device re-synchronizes. Note that synchronization results in the restarting of the digital filter and an interruption of 63 readings.

When the sync input is first applied on the first rising edge of CLK, the device re-synchronizes (under the condition $t_{SYNC} \neq N/f_{DATA}$). DRDY continues to output but DOUT is held low until the new data are ready. Then, if the period of the applied sync clock matches an integral multiple of the output data rate, the device freely runs without re-synchronization. The phase of the applied clock and output data rate (DRDY) are not matched as a result of the initial delay of DRDY after SYNC is applied. Figure 39 shows the timing for Continuous-sync mode.

Synchronization occurs on the next rising CLK edge after the SYNC pin rising edge; or after the eighth rising SCLK edge (opcode SYNC). To be effective, the SYNC opcode should broadcast simultaneously to all ADS1281s.

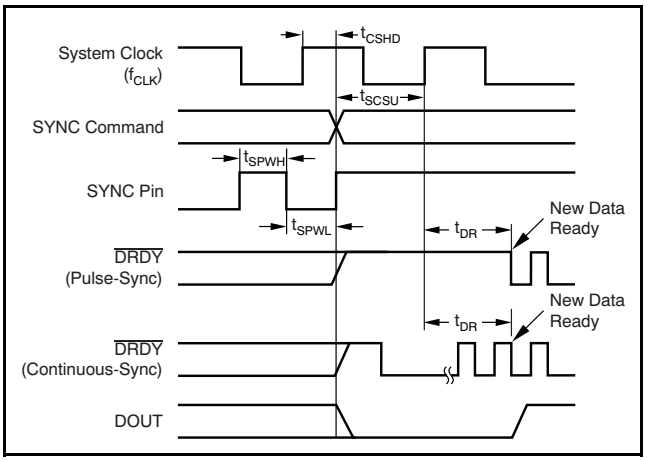

Figure 38. Pulse-Sync Timing, Continuous-Sync Timing with Single Sync

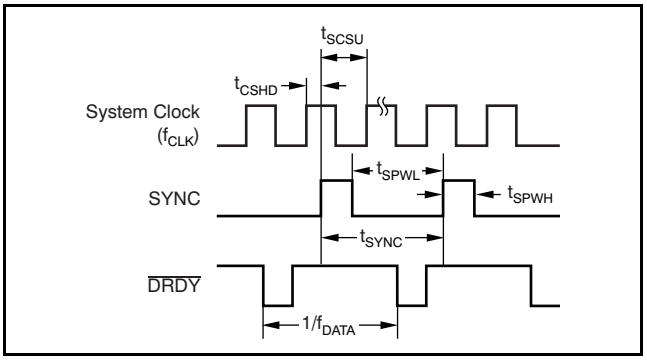

Figure 39. Continuous-Sync Timing with Sync Clock

Table 11. Pulse-Sync Timing for Figure 38 and Figure 39

PARAMETER	DESCRIPTION	MIN	MAX	UNITS
t_{SYNC}	SYNC period(1)	1	Infinite	n/f_{DATA}
t_{CSHD}	CLK to SYNC hold time to not latch on CLK edge	10		ns
t_{SCSU}	SYNC to CLK setup time to latch on CLK edge	10		ns
$t_{SPWH, L}$	SYNC pulse width, high or low	2		$1/f_{CLK}$
t_{DR}	Time for data ready (SINC filter)	See Appendix, Table 25		
	Time for data ready (FIR filter)	$62.98046875/f_{DATA} + 468/f_{CLK}$		

(1) Continuous-Sync mode; a free-running SYNC clock input without causing re-synchronization.

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RESET (RESET Pin and Reset Command)

The ADS1281 may be reset in two ways: toggle the RESET pin low or send a Reset command. When using the RESET pin, take it low and hold for at least $2/f_{CLK}$ to force a reset. The ADS1281 is held in reset until the pin is released. By command, RESET takes effect on the next rising edge of f_{CLK} after the eighth rising edge of SCLK of the command. Note: to ensure that the Reset command can function, the SPI interface may require a reset; see the *Serial Interface* section.

In reset, registers are set to default and the conversions are synchronized on the next rising edge of CLK. New conversion data are available, as shown in Figure 40 and Table 12.

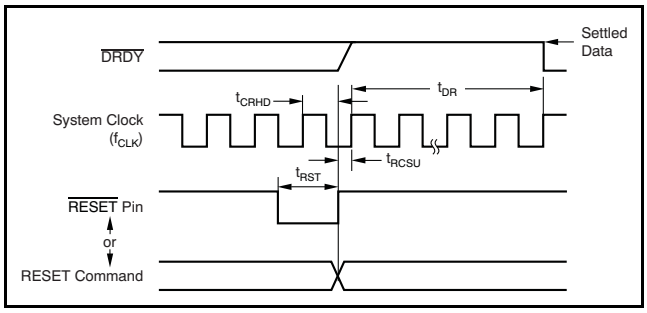

Figure 40. Reset Timing

Table 12. Reset Timing for Figure 40

PARAMETER	DESCRIPTION	MIN	UNITS
t_{CRHD}	CLK to RESET hold time	10	ns
t_{RCSU}	RESET to CLK setup time	10	ns
t_{RST}	RESET low	2	$1/f_{CLK}$
t_{DR}	Time for data ready	$62.98046875/f_{DATA} + 468/f_{CLK}$	

POWER-DOWN (PWDN Pin and Standby Command)

There are two ways to power-down the ADS1281: take the PWDN pin low or send a Standby command. When the PWDN pin is pulled low, the internal circuitry is disabled to minimize power and the contents of the register settings are reset.

In power-down, note that the device outputs remain active and the device inputs must not float. When the Standby command is sent, the SPI port and the configuration registers are kept active. Figure 41 and Table 13 show the timing.

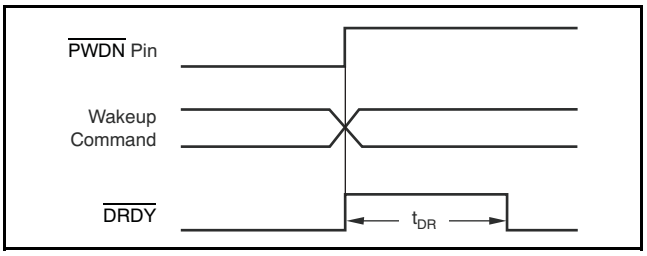

Figure 41. PWDN Pin and Wake-Up Command Timing (Table 13 shows t_{DR})

POWER-ON SEQUENCE

The ADS1281 has three power supplies: AVDD, AVSS, and DVDD. Figure 42 shows the power-on sequence of the ADS1281. The power supplies can be sequenced in any order. The supplies [the difference of (AVDD – AVSS) and DVDD] generate an internal reset whose outputs are summed to generate a global internal reset. After the supplies have crossed the minimum thresholds, 2^{16} f_{CLK} cycles are counted before releasing the internal reset. After the internal reset is released, new conversion data are available, as shown in Figure 42 and Table 13.

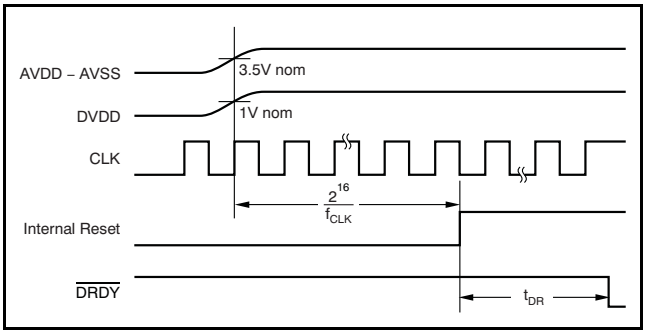

Figure 42. Power-On Sequence

Table 13. Power-On, PWDN Pin, and Wake-Up Command Timing for New Data

PARAMETER	DESCRIPTION		FILTER MODE
t_{DR}	Time for data ready 2^{16} CLK cycles after power-on; and new data ready after PWDN pin or Wake-Up command	See Appendix, Table 25	SINC (1)
		$62.98046875/f_{DATA} + 468/f_{CLK}$ (2)	FIR

(1) Supply power-on and PWDN pin default is 1000SPS FIR.
(2) Subtract 2 CLK cycles for the Wake-Up command. The Wake-Up command is timed from the next rising edge of CLK to after the eighth rising edge of SCLK during command to DRDY falling.

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DVDD POWER SUPPLY

The DVDD supply operates over the range of +1.65V to +3.6V. If DVDD is operated at less than 2.25V, connect the DVDD pin to the BYPAS pin. If DVDD is greater than or equal to 2.25V, do not connect DVDD to the BYPAS pin. Figure 43 shows this connection.

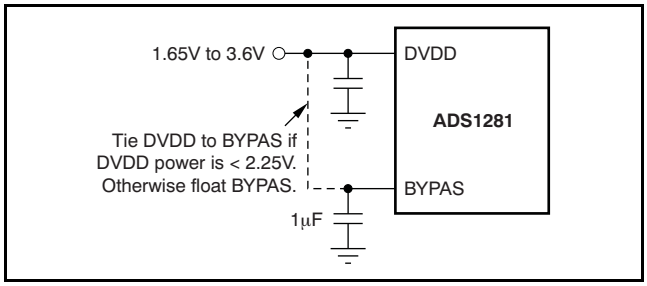

Figure 43. DVDD Power

SERIAL INTERFACE

A serial interface is used to read the conversion data and access the configuration registers. The interface consists of three basic signals: SCLK, DIN, and DOUT. An additional output, $\overline{\text{DRDY}}$, transitions low in Read Data Continuous mode when data are ready for retrieval. Figure 44 shows the connection when multiple converters are used.

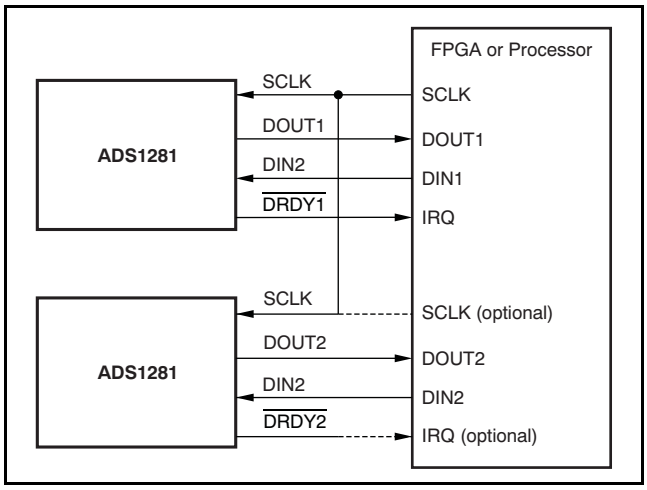

Figure 44. Pin Mode Interface for Multiple Devices

Serial Clock (SCLK)

The serial clock (SCLK) is an input that is used to clock data into (DIN) and out of (DOUT) the ADS1281. This input is a Schmitt-trigger input that has a high degree of noise immunity. However, it is recommended to keep SCLK as clean as possible to prevent possible glitches from inadvertently shifting the data.

Data are shifted into DIN on the rising edge of SCLK and data are shifted out of DOUT on the falling edge of SCLK. If SCLK is held low for 64 $\overline{\text{DRDY}}$ cycles, data transfer or commands in progress terminate and the SPI interface resets. The next SCLK pulse starts a new communication cycle. This timeout feature can be used to recover the interface when a transmission is interrupted or SCLK inadvertently glitches. SCLK should remain low when not active.

Data Input (DIN)

The data input pin (DIN) is used to input register data and commands to the ADS1281. Keep DIN low when reading conversion data in the Read Data Continuous mode (except when issuing a STOP Read Data Continuous command). Data on DIN are shifted into the converter on the rising edge of SCLK. In Pin mode, DIN is not used.

Data Output (DOUT)

The data output pin (DOUT) is used to output data from the ADS1281. Data are shifted out on DOUT on the falling edge of SCLK. In Pin mode, only conversion data are read from this pin.

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Data Ready (DRDY)

DRDY is an output; when it transitions low, this transition indicates new conversion data are ready, as shown in Figure 45. When reading data by the continuous mode, the data must be read within four CLK periods before DRDY goes low again or the data are overwritten with new conversion data. When reading data by the command mode, the read operation can overlap the occurrence of the next DRDY without data corruption.

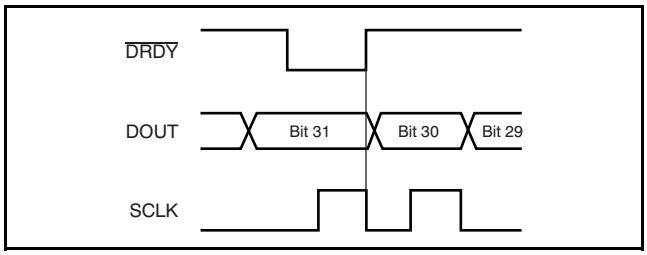

Figure 45. DRDY with Data Retrieval

DRDY resets high on the first falling edge of SCLK. Figure 45 and Figure 46 show the function of DRDY with and without data readback, respectively.

If data are not retrieved (no SCLK provided), DRDY pulses high for four f_{CLK} periods during the update time, as shown in Figure 46.

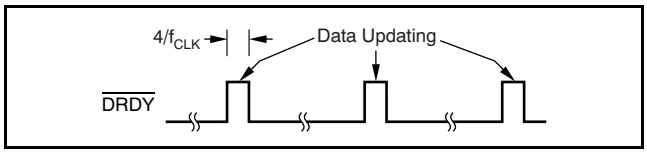

Figure 46. DRDY with No Data Retrieval

DATA FORMAT

The ADS1281 provides 32 bits of conversion data in binary twos complement format, as shown in Table 14. The LSB of the data is a redundant sign bit: '0' for positive numbers and '1' for negative numbers. However, when the output is clipped to +FS, the LSB = 1; when the output is clipped to –FS, the LSB = 0. If desired, the data readback may be stopped at 24 bits. Note that in sinc filter mode, the output data are scaled by 1/2.

Table 14. Ideal Output Code versus Input Signal

INPUT SIGNAL V_{IN} (AINP – AINN)	32-BIT IDEAL OUTPUT CODE(1)	
	FIR FILTER	SINC FILTER(2)
$> \frac{V_{REF}}{2}$	7FFFFFFFh	(3)
$\frac{V_{REF}}{2}$	7FFFFFFEh	3FFFFFFFh
$\frac{V_{REF}}{2 \times (2^{30} - 1)}$	00000002h	00000001h
0	00000000h	00000000h
$\frac{-V_{REF}}{2 \times (2^{30} - 1)}$	FFFFFFFFh	FFFFFFFFh
$\frac{-V_{REF}}{2} \times \frac{2^{30}}{2^{30} - 1}$	80000001h	C0000000h
$< \frac{-V_{REF}}{2} \times \frac{2^{30}}{2^{30} - 1}$	80000000h	(3)

(1) Excludes effects of noise, linearity, offset, and gain errors.

(2) As a result of the reduction in oversampling ratio (OSR) related to the sinc filter high data rates, the available resolution may be reduced.

(3) In sinc filter mode, the output does not clip when the full-scale range is exceeded.

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READING DATA

The ADS1281 has two ways to read conversion data: Read Data Continuous and Read Data By Command.

Read Data Continuous

In the Read Data Continuous mode, the conversion data are shifted out directly from the device without the need for sending a read command. This mode is the default mode at power-on. This mode is also enabled by the RDATAC command. When DRDY goes low, indicating that new data are available, the MSB of data appears on DOUT, as shown in Figure 47. The data are normally read on the rising edge of SCLK and at the occurrence of the first falling edge of SCLK, DRDY returns high. After 32 bits of data have been shifted out, further SCLK transitions cause DOUT to go low. If desired, the read operation may be stopped at 24 bits. The data shift operation must be completed within four CLK periods before DRDY falls again or the data may be corrupted.

The Read Data Continuous mode is the default data mode for Pin mode. When a Stop Read Data Continuous command is issued, the DRDY output is blocked but the ADS1281 continues conversions. In stop continuous mode, the data can only be read by command.

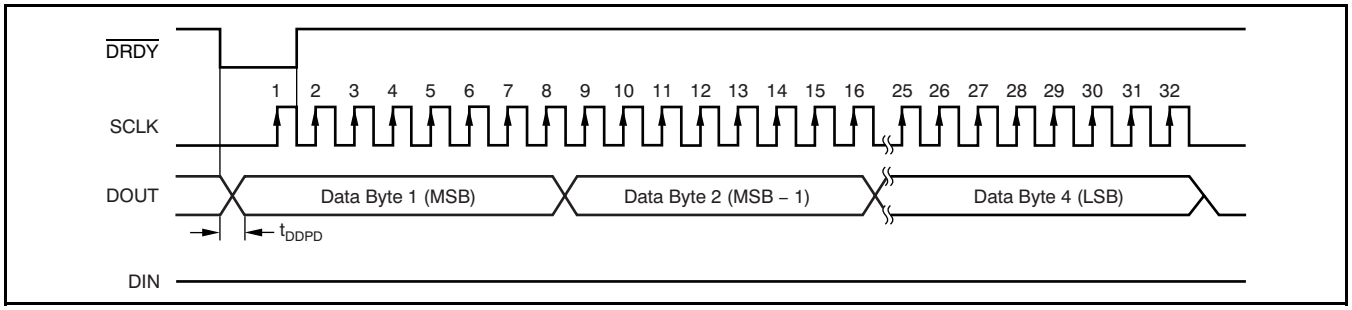

Figure 47. Read Data Continuous

Table 15. Timing Data for Figure 47

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{DDPD}	DRDY to valid MSB on DOUT propagation delay(1)			100	ns

(1) Load on DOUT = 20pF || 100kΩ.

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Read Data By Command

The Read Data Continuous mode is stopped by the SDATAC command. In this mode, conversion data are read by command. In the Read Data By Command mode, a read data command must be sent to the device for each data conversion (as shown in Figure 48). When the read data command is received (on the eighth SCLK rising edge), data are available to read only when $\overline{DRDY}$ goes low (t_{DR}). When $\overline{DRDY}$ goes low, conversion data appear on DOUT. The data may be read on the rising edge of SCLK.

ONE-SHOT OPERATION

The ADS1281 can perform very power-efficient, one-shot conversions using the STANDBY command while under software control. Figure 49 shows this sequence. First, issue the STANDBY command to set the Standby mode.

When ready to make a measurement, issue the WAKEUP command. Monitor $\overline{DRDY}$; when it goes low, the fully settled conversion data are ready and may be read directly in Read Data Continuous mode. Afterwards, issue another STANDBY command. When ready for the next measurement, repeat the cycle starting with another WAKEUP command.

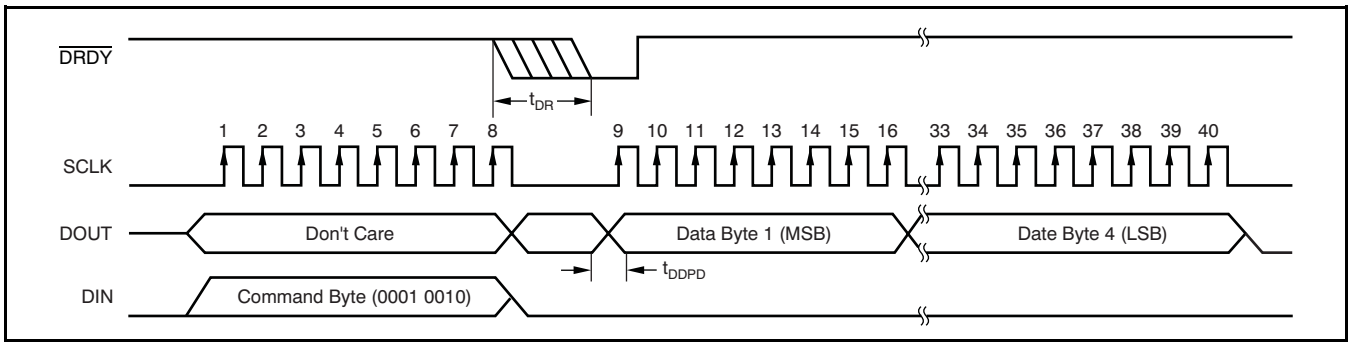
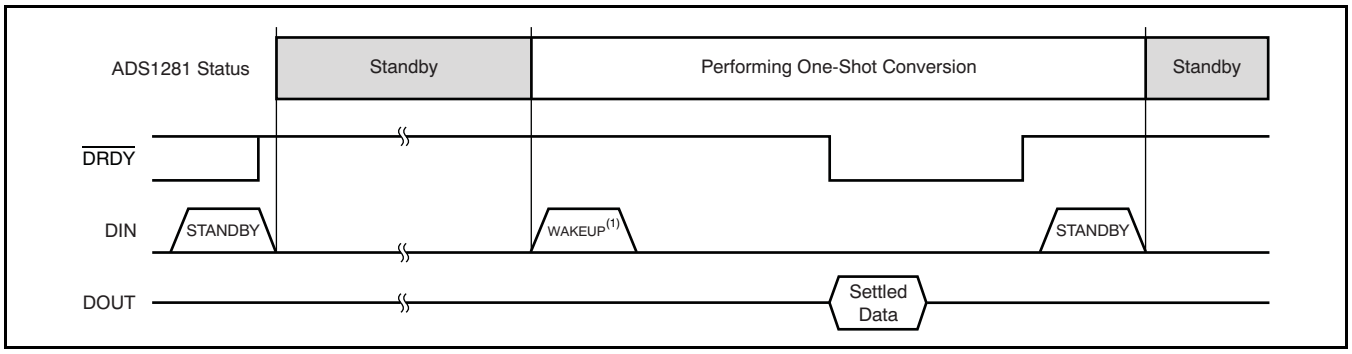


Figure 48. Read Data By Command, RDATA (t_{DDPD} timing is given in Table 15)

Table 16. Read Data Timing for Figure 48

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{DR}	Time for new data after data read command	0		1	f_{DATA}



(1) See Figure 41 and Table 13 for time to new data.

Figure 49. One-Shot Conversions Using the STANDBY Command

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OFFSET AND FULL-SCALE CALIBRATION REGISTERS

The conversion data can be scaled for offset and gain before yielding the final output code. As shown in Figure 50, the output of the digital filter is first subtracted by the offset register (OFC) and then multiplied by the full-scale register (FSC). Equation 7 shows the scaling:

$$\text{Final Output Data} = (\text{Input} - \text{OFC}[2:0]) \times \frac{\text{FSC}[2:0]}{400000\text{h}} \quad (7)$$

The values of the offset and full-scale registers are set by writing to them directly, or they are set automatically by calibration commands.

OFC[2:0] Registers

The offset calibration is a 24-bit word, composed of three 8-bit registers, as shown in Table 19. The offset register is left-justified to align with the 32-bits of conversion data. The offset is in twos complement format with a maximum positive value of 7FFFFFh and a maximum negative value of 800000h. This value is subtracted from the conversion data. A register value of 00000h has no offset correction (default value). Note that while the offset calibration register value can correct offsets ranging from –FS to +FS (as shown in Table 17), to avoid input overload, the analog inputs cannot exceed the full-scale range.

Table 17. Offset Calibration Values

OFC REGISTER	FINAL OUTPUT CODE(1)
7FFFFFh	80000000h
000001h	FFFFFF00h
000000h	00000000h
FFFFFFh	00000100h
800000h	7FFFFF00h

(1) Full 32-bit final output code with zero code input.

FSC[2:0] Registers

The full-scale calibration is a 24-bit word, composed of three 8-bit registers, as shown in Table 20. The full-scale calibration value is 24-bit, straight offset binary, normalized to 1.0 at code 400000h. Table 18 summarizes the scaling of the full-scale register. A register value of 400000h (default value) has no gain correction (gain = 1). Note that while the gain calibration register value corrects gain errors above 1 (gain correction < 1), the full-scale range of the analog inputs should not exceed 103% to avoid input overload.

Table 18. Full-Scale Calibration Register Values

FSC REGISTER	GAIN CORRECTION
800000h	2.0
400000h	1.0
200000h	0.5
000000h	0

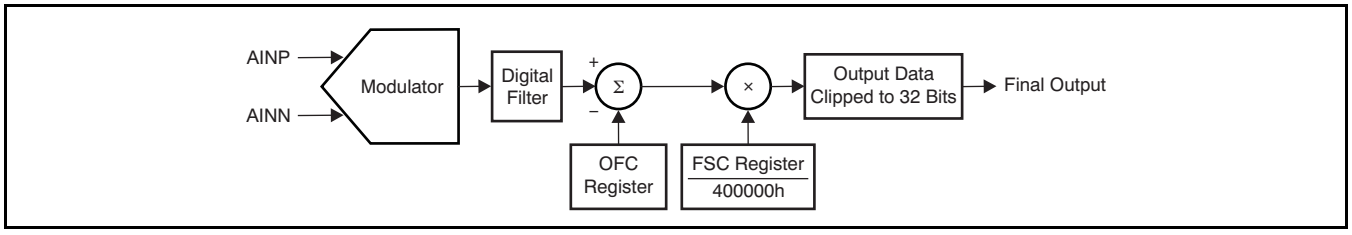

Figure 50. Calibration Block Diagram

Table 19. Offset Calibration Word

REGISTER	BYTE	BIT ORDER							
OFC0	LSB	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)
OFC1	MID	B15	B14	B13	B12	B11	B10	B9	B8
OFC2	MSB	B23 (MSB)	B22	B21	B20	B19	B18	B17	B16

Table 20. Full-Scale Calibration Word

REGISTER	BYTE	BIT ORDER							
FSC0	LSB	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)
FSC1	MID	B15	B14	B13	B12	B11	B10	B9	B8
FSC2	MSB	B23 (MSB)	B22	B21	B20	B19	B18	B17	B16

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CALIBRATION COMMANDS

Calibration commands may be sent to the ADS1281 to calibrate the conversion data. The values of the offset and gain calibration registers are internally written to perform calibration. The appropriate input signals must be applied to the ADS1281 inputs before sending the commands. Use slower data rates to achieve more consistent calibration results; this effect is a byproduct of the lower noise that these data rates provide. Also, if calibrating at power-on, be sure the reference voltage is fully settled.

Figure 51 shows the calibration command sequence. After the analog input voltage (and reference) have stabilized, send the Stop Data Continuous command followed by the SYNC and Read Data Continuous commands. 64 data periods later, $\overline{\text{DRDY}}$ goes low. After $\overline{\text{DRDY}}$ goes low, send the Stop Data Continuous, then the Calibrate command followed by the Read Data Continuous command. After 16 data periods, calibration is complete and conversion data may be read at this time. The SYNC input must remain high during the calibration sequence. Note that calibration is bypassed in sinc filter mode.

OFSCAL Command

The OFSCAL command performs an offset calibration. Before sending the offset calibration command, a *zero* input signal must be applied to the ADS1281 and the inputs allowed to stabilize. When the command is sent, the ADS1281 averages 16 readings and then writes this value to the OFC register. The contents of the OFC register may be subsequently read or written. During offset calibration, the full-scale correction is bypassed.

GANCAL Command

The GANCAL command performs a gain calibration. Before sending the GANCAL command sequence (Figure 51), a dc input must be applied (typically full-scale input, but not to exceed 103% full-scale). After the signal has stabilized, the command sequence can be sent. The ADS1281 averages 16 readings, then computes a gain value that makes the applied input the new full-scale. The gain value is written to the FSC register, whose contents may be subsequently read or written.

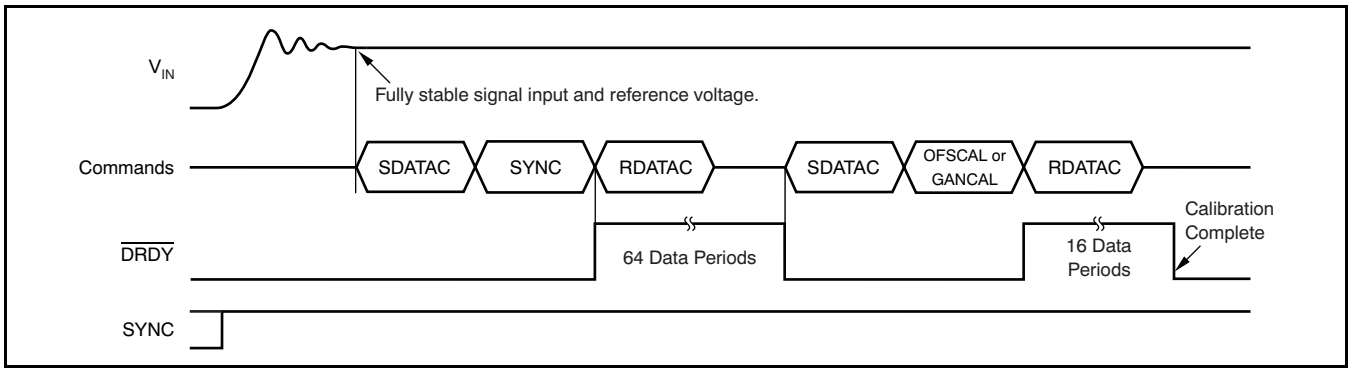

Figure 51. Offset/Gain Calibration Timing

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USER CALIBRATION

System calibration of the ADS1281 can be performed without using the calibration commands. This procedure requires the calibration values to be externally calculated and then written to the calibration registers. The steps for this procedure are:

1. Set the OFSCAL[2:0] register = 0h and GANCAL[2:0] = 400000h. These values set the offset and gain registers to 0 and 1, respectively.
2. Apply a *zero* differential input to the input of the system. Wait for the system to settle and then average *n* output readings. Higher numbers of averaged readings result in more consistent calibration. Write the averaged value to the OFC register.
3. Apply a differential dc signal, or an ac signal (typically full-scale, but not to exceed 103% full-scale). Wait for the system to settle and then average the *n* output readings.

The value written to the FSC registers is calculated by Equation 8 and Equation 9.

DC signal calibration is shown in Equation 8 and Equation 9. The expected output code is based on 31-bit output data.

$$\text{FSC[2:0]} = 400000\text{h} \times \left(\frac{\text{Expected Output Code}}{\text{Actual Output Code}} \right) \quad (8)$$

$$\text{Expected Output Code} = 2 \times V_{IN} \times \frac{2^{31}}{V_{REF}} \quad (9)$$

For ac signal calibration, use an RMS value of collected data (as shown in Equation 10).

$$\text{FSC[2:0]} = 400000\text{h} \times \frac{\text{Expected RMS Value}}{\text{Actual RMS Value}} \quad (10)$$

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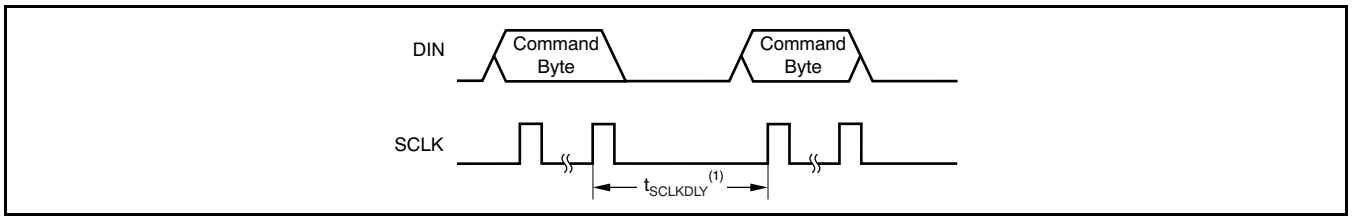
COMMANDS

The commands listed in Table 21 control the operation of the ADS1281. Command operations are only possible in Register mode. Most commands are stand-alone (that is, 1 byte in length); the register reads and writes require a second command byte in addition to the actual data bytes.

A delay of 24 f_{CLK} cycles between commands and between bytes within a command is required, starting from the last SCLK rising edge of one command to the first SCLK rising edge of the following command. This delay is shown in Figure 52.

In Read Data Continuous mode, the ADS1281 places conversion data on the DOUT pin as SCLK is applied. As a consequence of the potential conflict of conversion data on DOUT and data placed on DOUT resulting from a register or Read Data By Command operation, it is necessary to send a STOP Read Data Continuous command before Register or Data Read By Command. The STOP Read Data Continuous command disables the direct output of conversion data on the DOUT pin.



(1) $t_{SCLKDLY} = 24/f_{CLK}$ (min).

Figure 52. Consecutive Commands

Table 21. Command Descriptions

COMMAND	TYPE	DESCRIPTION	1st COMMAND BYTE(1) (2)	2nd COMMAND BYTE(3)
WAKEUP	Control	Wake-up from Standby mode	0000 000X (00h or 01h)	
STANDBY	Control	Enter Standby mode	0000 001X (02h or 03h)	
SYNC	Control	Synchronize the A/D conversion	0000 010X (04h or 5h)	
$\overline{\text{RESET}}$	Control	Reset registers to default values	0000 011X (06h or 07h)	
RDATAC	Control	Read data continuous	0001 0000 (10h)	
SDATAC	Control	Stop read data continuous	0001 0001 (11h)	
RDATA	Data	Read data by command(4)	0001 0010 (12h)	
RREG	Register	Read *nnnnn* register(s) at address *rrrrr* (4)	001*r rrrr* (20h + 000*r* rrrr)	000*n nnnn* (00h + *n nnnn*)
WREG	Register	Write *nnnnn* register(s) at address *rrrrr*	010*r rrrr* (40h + 000*r rrrr*)	000*n nnnn* (00h + *n nnnn*)
OFSCAL	Calibration	Offset calibration	0110 0000 (60h)	
GANCAL	Calibration	Gain calibration	0110 0001 (61h)	

(1) X = don't care.
(2) rrrrr = starting address for register read and write commands.
(3) nnnnn = number of registers to be read/written – 1. For example, to read/write three registers, set *nnnnn* = 2 (00010).
(4) Required to cancel Read Data Continuous mode before sending a command.

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WAKEUP: Wake-Up From Standby Mode

Description: This command is used to exit the standby mode. Upon sending the command, the time for the first data to be ready is illustrated in Figure 41 and Table 14. Sending this command during normal operation has no effect; for example, reading data by the Read Data Continuous method with DIN held low.

STANDBY: Standby Mode

Description: This command places the ADS1281 into Standby mode. In Standby, the device enters a reduced power state where a low quiescent current remains to keep the register settings and SPI interface active. For complete device shutdown, take the PWDN pin low (register settings are not saved). To exit Standby mode, issue the WAKEUP command. The operation of Standby mode is shown in Figure 53.

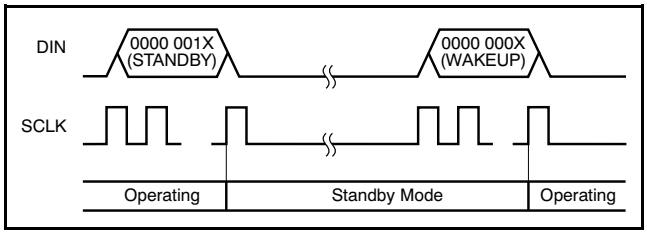

Figure 53. STANDBY Command Sequence

SYNC: Synchronize the A/D Conversion

Description: This command synchronizes the A/D conversion. Upon receipt of the command, the reading in progress is cancelled and the conversion process is re-started. In order to synchronize multiple ADS1281s, the command must be sent simultaneously to all devices. Note that the SYNC pin must be high for this command.

RESET: Reset the Device

Description: The RESET command resets the registers to default values, enables the Read Data Continuous mode, and restarts the conversion process; the RESET command is functionally the same as the RESET pin. See Figure 40 for the RESET command timing.

RDATAC: Read Data Continuous

Description: This command enables the Read Data Continuous mode (default mode). In this mode, conversion data can be read from the device directly without the need to supply a data read command. Each time DRDY falls low, new data are available to read. See the *Read Data Continuous* section for more details.

SDATAC: Stop Read Data Continuous

Description: This command stops the Read Data Continuous mode. Exiting the Read Data Continuous mode is required before sending Register and Data read commands. This command suppresses the DRDY output, but the ADS1281 continues conversions.

RDATA: Read Data By Command

Description: This command reads the conversion data. See the *Read Data By Command* section for more details.

RREG: Read Register Data

Description: This command is used to read single or multiple register data. The command consists of a two-byte op-code argument followed by the output of register data. The first byte of the op-code includes the starting address, and the second byte specifies the number of registers to read – 1.

First command byte: 001r rrrr, where *rrrrr* is the starting address of the first register.

Second command byte: 000n nnnn, where *nnnnn* is the number of registers – 1 to read.

Starting with the 16th falling edge of SCLK, the register data appear on DOUT.

The RREG command is illustrated in Figure 54. Note that a delay of 24 f_{CLK} cycles is required between each byte transaction.

WREG: Write to Register

Description: This command writes single or multiple register data. The command consists of a two-byte op-code argument followed by the input of register data. The first byte of the op-code contains the starting address and the second byte specifies the number of registers to write – 1.

First command byte: 001r rrrr, where *rrrrr* is the starting address of the first register.

Second command byte: 000n nnnn, where *nnnnn* is the number of registers – 1 to write.

Data byte(s): one or more register data bytes, depending on the number of registers specified.

Figure 55 illustrates the WREG command.

Note that a delay of 24 f_{CLK} cycles is required between each byte transaction.

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OFSCAL: Offset Calibration

Description: This command performs an offset calibration. The inputs to the converter (or the inputs to the external pre-amplifier) should be zeroed and allowed to stabilize before sending this command. The offset calibration register updates after this operation. See the *Calibration Commands* section for more details.

GANCAL: Gain Calibration

Description: This command performs a gain calibration. The inputs to the converter should have a stable dc input (typically full-scale, but not to exceed 103% full-scale). The full-scale calibration register updates after this operation. See the *Calibration Commands* section for more details.

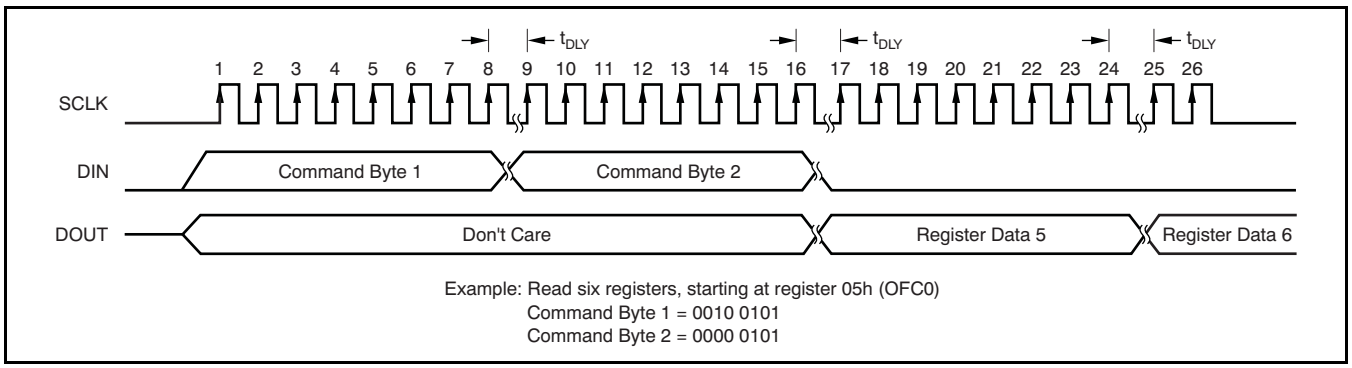

Figure 54. Read Register Data (Table 22 shows t_{DLY})

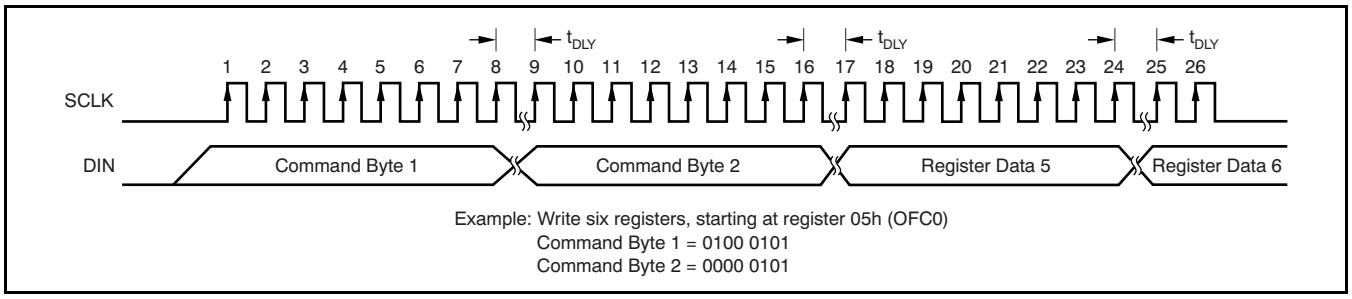

Figure 55. Write Register Data (Table 22 shows t_{DLY})

Table 22. t_{DRY} Value

PARAMETER	MIN
t_{DLY}	$24/f_{CLK}$

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REGISTER MAP

The Register mode (PINMODE = 0) allows read and write access to the device registers. Collectively, the registers contain all the information needed to configure the device, such as data rate, filter selection, calibration, etc. The registers are accessed by the RREG and WREG commands. The registers can be accessed individually or as a block of registers by sending or receiving consecutive bytes. Note that after a register write operation, the ADC resets, resulting in 63 reading interruption.

Table 23. Register Map

ADDRESS	REGISTER	RESET VALUE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	ID	X0h	ID3	ID2	ID1	ID0	0	0	0	0
01h	CONFIG0	52h	SYNC	1	DR2	DR1	DR0	PHS	FILTR1	FILTR0
02h	Reserved	08h	0	0	0	0	1	0	0	0
03h	HPF0	32h	HPF07	HPF06	HPF05	HPF04	HPF03	HPF02	HPF01	HPF00
04h	HPF1	03h	HPF15	HPF14	HPF13	HPF12	HPF11	HPF10	HPF09	HPF08
05h	OFC0	00h	OFC07	OFC06	OFC05	OFC04	OFC03	OFC02	OFC01	OFC00
06h	OFC1	00h	OFC15	OFC14	OFC13	OFC12	OFC11	OFC10	OFC09	OFC08
07h	OFC2	00h	OFC23	OFC22	OFC21	OFC20	OFC19	OFC18	OFC17	OFC16
08h	FSC0	00h	FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00
09h	FSC1	00h	FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08
0Ah	FSC2	40h	FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16

ID: ID REGISTER (ADDRESS 00h)

7	6	5	4	3	2	1	0
ID3	ID2	ID1	ID0	0	0	0	0

Reset value = X8h.

Bits[7:4] **ID[3:0]**

Factory-programmed identification bits (read-only)

Bits[3:0] **Reserved**

Always write '0'

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CONFIG0: CONFIGURATION REGISTER 0 (ADDRESS 01h)

7	6	5	4	3	2	1	0
SYNC	1	DR2	DR1	DR0	PHASE	FILTR1	FILTR0

Reset value = 52h.

Bit[7] **SYNC**

Synchronization mode
0: Pulse SYNC mode (default)
1: Continuous SYNC mode

Bit[6] **Reserved**

Always write '1' (default)

Bits[5:3] **Data Rate Select**

DR[2:0]

000: 250SPS
001: 500SPS
010: 1000SPS (default)
011: 2000SPS
100: 4000SPS

Bit[2] **FIR Phase Response**
PHASE

0: Linear phase (default)
1: Minimum phase

Bits[1:0] **Digital Filter Select**

FILTR[1:0]

Digital filter configuration
00: On-chip filter bypassed, modulator output mode
01: Sinc filter block only
10: Sinc + LPF filter blocks (default)
11: Sinc + LPF + HPF filter blocks

RESERVED: (ADDRESS 02h)

7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	0

Reset value = 08h.

Bits[7:0] **Reserved**

Always write '08h'

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HPF1 and HPF0

These two bytes (high-byte and low-byte, respectively) set the corner frequency of the HPF.

HPF0: High-Pass Filter Corner Frequency, Low Byte (Address 03h)

7	6	5	4	3	2	1	0
HP07	HP06	HP05	HP04	HP03	HP02	HP01	HP00

Reset value = 32h.

HPF1: High-Pass Filter Corner Frequency, High Byte (Address 04h)

7	6	5	4	3	2	1	0
HP15	HP14	HP13	HP12	HP11	HP10	HP09	HP08

Reset value = 03h.

OFC2, OFC1, OFC0

These three bytes set the OFC value.

OFC0: Offset Calibration, Low Byte (Address 05h)

7	6	5	4	3	2	1	0
OC07	OC06	OC05	OC04	OC03	OC02	OC01	OC00

Reset value = 00h.

OFC1: Offset Calibration, Mid Byte (Address 06h)

7	6	5	4	3	2	1	0
OC15	OC14	OC13	OC12	OC11	OC10	OC09	OC08

Reset value = 00h.

OFC2: Offset Calibration, High Byte (Address 07h)

7	6	5	4	3	2	1	0
OC23	OC22	OC21	OC20	OC19	OC18	OC17	OC16

Reset value = 00h.

FSC2, FSC1, FSC0

These three bytes set the FSC value.

FSC0: Full-Scale Calibration, Low Byte (Address 08h)

7	6	5	4	3	2	1	0
FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00

Reset value = 00h.

FSC1: Full-Scale Calibration, Mid Byte (Address 09h)

7	6	5	4	3	2	1	0
FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08

Reset value = 00h.

FSC2: Full-Scale Calibration, High Byte (Address 0Ah)

7	6	5	4	3	2	1	0
FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16

Reset value = 40h.

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CONFIGURATION GUIDE

The ADS1281 offers two modes of operation: Pin Control mode and Register Control mode. In Pin Control mode, the operation of the device is controlled by the pins; there are no registers to program. In Register Control mode, the registers are used to control device operation. After RESET or power-on, the registers can be configured using the following procedure:

1. **Reset the SPI interface.** Before using the SPI interface, it may be necessary to recover the SPI interface (undefined I/O power-up sequencing may cause false SCLK detection). To reset the SPI interface, toggle the RESET pin or, when in Read Data Continuous mode, hold SCLK low for 64 DRDY periods.
2. **Configure the registers.** The registers are configured by either writing to them individually or as a group. Software may be configured in either mode. The STOPC command must be sent before register read/write operations to cancel the Read Data Continuous mode.
3. **Verify register data.** The register may be read back for verification of device communications.
4. **Set the data mode.** After register configuration, the device may be configured for Read Data Continuous mode, either by the Read Data Continuous command or configured in Read Data By Register mode using STOPC command.
5. **Synchronize readings.** Whenever SYNC is high, the ADS1281 freely runs the data conversions. To stop and restart the conversions, take SYNC low and then high.
6. **Read data.** If the Read Data Continuous mode is active, the data are read directly after DRDY falls by applying SCLK pulses. If the Read Data Continuous mode is inactive, the data can only be read by Read Data By Command. The Read Data command must be sent in this mode to read each conversion result (note that DRDY only asserts after each read data command is sent).

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APPLICATION INFORMATION

The ADS1281 is a very high-resolution ADC. Optimal device performance requires giving special attention to the support circuitry and printed circuit board (PCB) design. Locate noisy digital components, such as microcontrollers and oscillators, in an area of the PCB away from the converter or front-end components. Place the digital components close to the power-entry point to keep the digital current path short and separate from sensitive analog components.

Figure 56 shows a typical geophone interface. This application circuit shows the ADS1281 and the OPA211 pre-amplifiers operating with ±2.5V supplies. The OPA211s are shown with gain = +4 [G = 1 + 2 (R_2/R_1)]. This pre-amplifier configuration has inherently good common-mode rejection. The 49.9Ω resistors isolate the driver outputs from the bypass capacitor.

The 20kΩ input resistors provide the common-mode bias for the amplifiers. The optional differential and common-mode input filters attenuate possible out-of-band interference (such as RFI). Recommended 75kΩ resistors provide a 20mV_{DC} input offset. The offset moves the low-level idle tones out of the passband.

The REF02 +5V reference provides the reference to the ADS1281. The reference output is filtered by the optional R_3 and C_1 filter network. The filter requires several seconds to settle after power-on. Capacitor C_2 provides high-frequency bypassing of the reference inputs and should be placed close to the ADS1281 pins. Note that R_3 (1kΩ) results in a systematic gain error (1.2%). The filter can be externally buffered to eliminate the gain error.

Alternatively, the REF5050 (5V) or REF5045 (4.5V) reference can be used. The REF5045 reference has the advantage of +5V power supply operation. The REF5050 requires +5.2V minimum power supply.

As with any precision circuit, use good supply bypassing techniques. Place the capacitors close to the device pins.

If switching dc/dc supplies are used to power the device, check for frequency components of the supply present within the ADS1281 passband. Voltage ripple should be kept as low as possible.

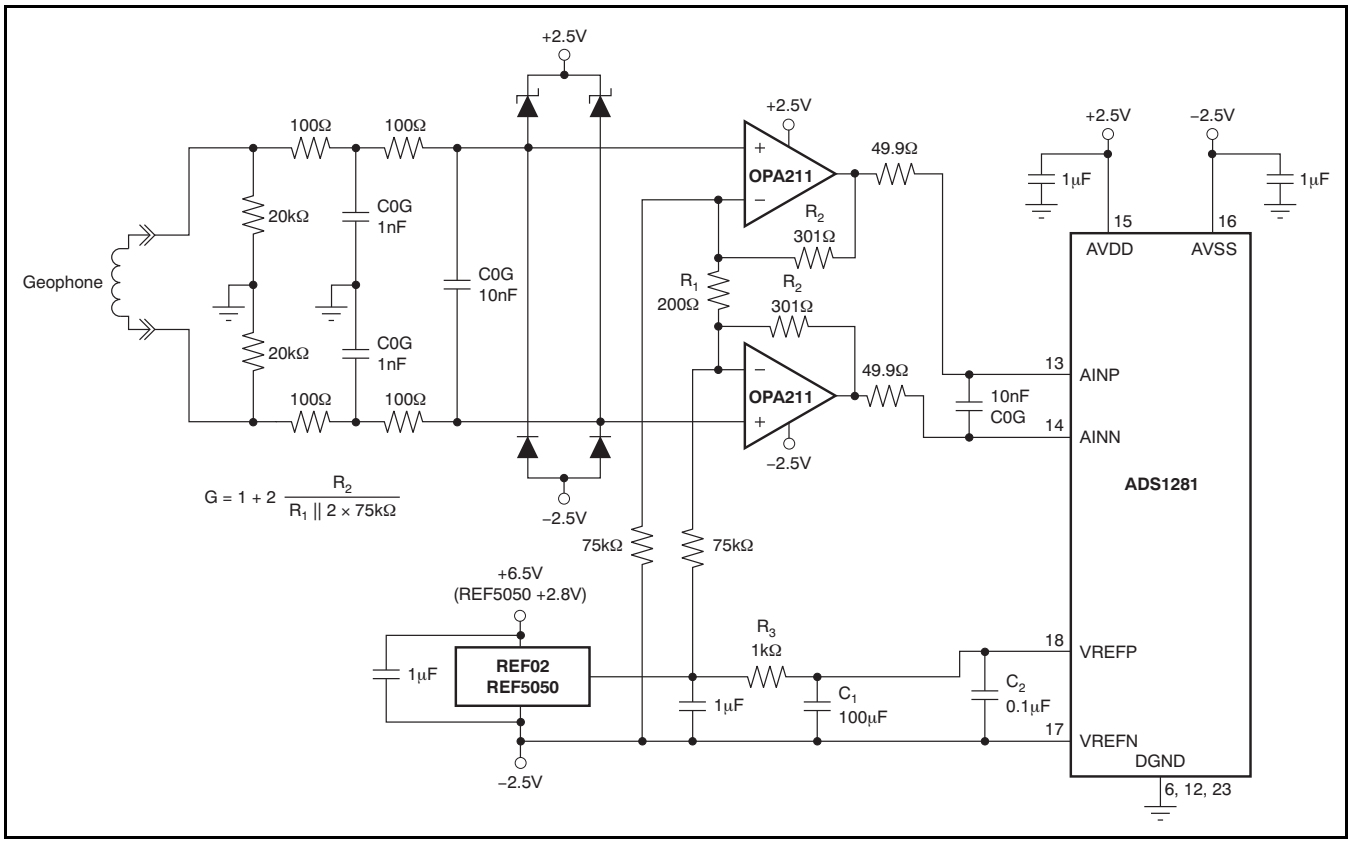
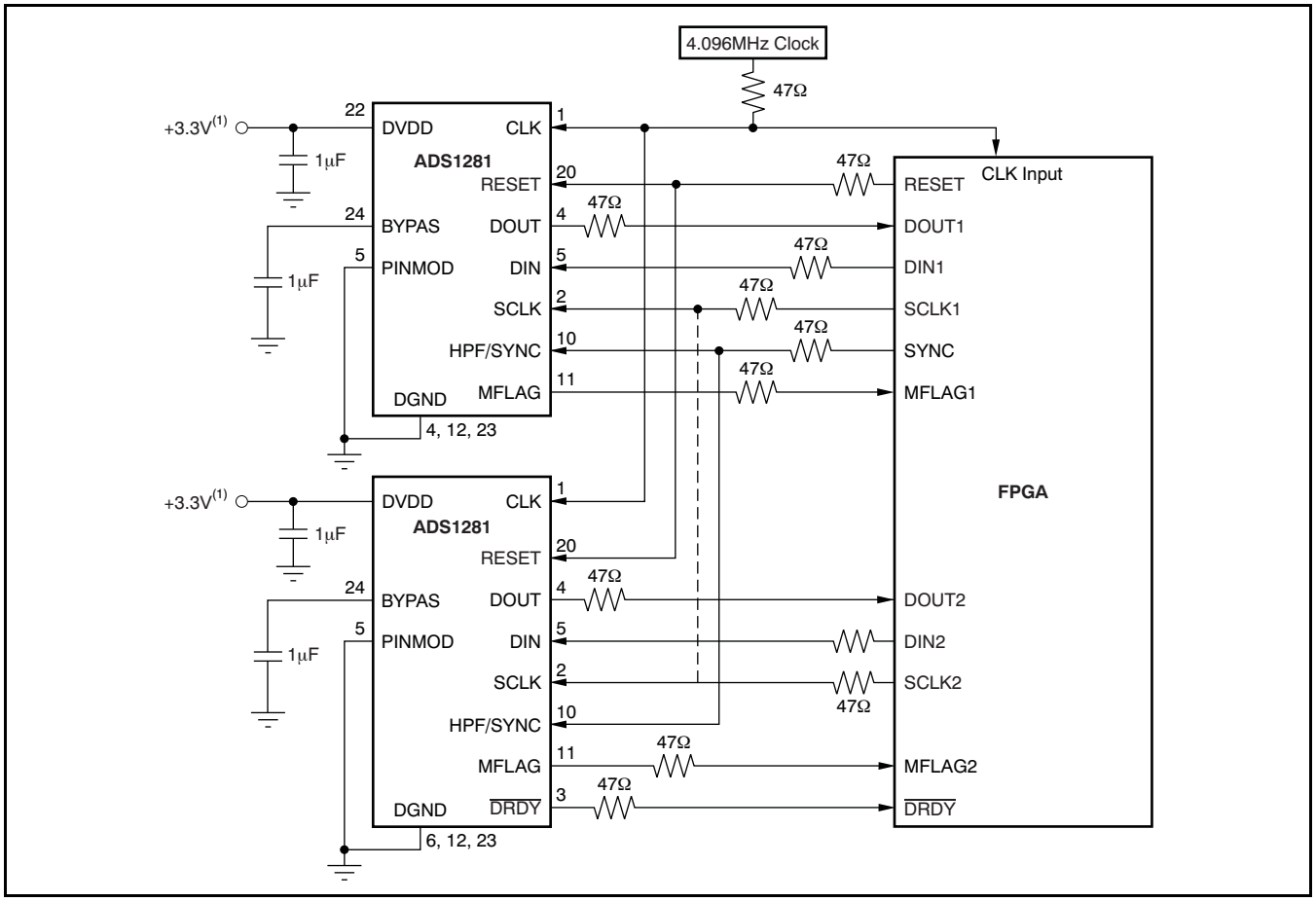


Figure 56. Geophone Interface, Dual Power-Supply Configuration

Figure 57 shows the digital connection to an FPGA (field programmable gate array) device. In this example, two ADS1281s are shown connected. The DRDY output from each ADS1281 can be used; however, when the devices are synchronized, the DRDY output from only one device is sufficient. A shared SCLK line between the devices is optional.

The modulator over-range flag (MFLAG) from each device ties to the FPGA. For synchronization, one SYNC control line connects all ADS1281 devices. The RESET line also connects to all ADS1281 devices.

For best performance, the FPGA and the ADS281s should operate from the same clock. Avoid ringing on the digital inputs. 47Ω resistors in series with the digital traces can help to reduce ringing by controlling impedances. Place the resistors at the source (driver) end of the trace. Unused digital inputs should not float; tie them directly to DVDD or GND.



NOTE: Dashed lines are optional.

(1) For DVDD < 2.25V, see the *DVDD Power Supply* section.

Figure 57. FPGA Device

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APPENDIX

Table 24. FIR Stage Coefficients

COEFFICIENT	SESSION 1	SESSION 2	SESSION 3		SESSION 4	
			Scaling = 134217728		Scaling = 134217728	
	LINEAR PHASE SCALING = 1/512	LINEAR PHASE SCALING = 1/8388608	LINEAR PHASE	MINIMUM PHASE	LINEAR PHASE	MINIMUM PHASE
b_0	3	–10944	0	819	–132	11767
b_1	0	0	0	8211	–432	133882
b_2	–25	103807	–73	44880	–75	769961
b_3	0	0	–874	174712	2481	2940447
b_4	150	–507903	–4648	536821	6692	8262605
b_5	256	0	–16147	1372637	7419	17902757
b_6	150	2512192	–41280	3012996	–266	30428735
b_7	0	4194304	–80934	5788605	–10663	40215494
b_8	–25	2512192	–120064	9852286	–8280	39260213
b_9	0	0	–118690	14957445	10620	23325925
b_{10}	3	–507903	–18203	20301435	22008	–1757787
b_{11}		0	224751	24569234	348	–21028126
b_{12}		103807	580196	26260385	–34123	–21293602
b_{13}		0	893263	24247577	–25549	–3886901
b_{14}		–10944	891396	18356231	33460	14396783
b_{15}			293598	9668991	61387	16314388
b_{16}			–987253	327749	–7546	1518875
b_{17}			–2635779	–7171917	–94192	–12979500
b_{18}			–3860322	–10926627	–50629	–11506007
b_{19}			–3572512	–10379094	101135	2769794
b_{20}			–822573	–6505618	134826	12195551
b_{21}			4669054	–1333678	–56626	6103823
b_{22}			12153698	2972773	–220104	–6709466
b_{23}			19911100	5006366	–56082	–9882714
b_{24}			25779390	4566808	263758	–353347
b_{25}			27966862	2505652	231231	8629331
b_{26}			25779390	126331	–215231	5597927
b_{27}			19911100	–1496514	–430178	–4389168
b_{28}			12153698	–1933830	34715	–7594158
b_{29}			4669054	–1410695	580424	–428064
b_{30}			–822573	–502731	283878	6566217
b_{31}			–3572512	245330	–588382	4024593
b_{32}			–3860322	565174	–693209	–3679749
b_{33}			–2635779	492084	366118	–5572954
b_{34}			–987253	231656	1084786	332589
b_{35}			293598	–9196	132893	5136333
b_{36}			891396	–125456	–1300087	2351253
b_{37}			893263	–122207	–878642	–3357202
b_{38}			580196	–61813	1162189	–3767666
b_{39}			224751	–4445	1741565	1087392
b_{40}			–18203	22484	–522533	3847821
b_{41}			–118690	22245	–2490395	919792
b_{42}			–120064	10775	–688945	–2918303

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Table 24. FIR Stage Coefficients (continued)

COEFFICIENT	SESSION 1	SESSION 2	SESSION 3		SESSION 4	
			Scaling = 134217728		Scaling = 134217728	
	LINEAR PHASE SCALING = 1/512	LINEAR PHASE SCALING = 1/8388608	LINEAR PHASE	MINIMUM PHASE	LINEAR PHASE	MINIMUM PHASE
b_{43}			–80934	940	2811738	–2193542
b_{44}			–41280	–2953	2425494	1493873
b_{45}			–16147	–2599	–2338095	2595051
b_{46}			–4648	–1052	–4511116	–79991
b_{47}			–874	–43	641555	–2260106
b_{48}			–73	214	6661730	–963855
b_{49}			0	132	2950811	1482337
b_{50}			0	33	–8538057	1480417
b_{51}			0	0	–10537298	–586408
b_{52}					9818477	–1497356
b_{53}					41426374	–168417
b_{54}					56835776	1166800
b_{55}					41426374	644405
b_{56}					9818477	–675082
b_{57}					–10537298	–806095
b_{58}					–8538057	211391
b_{59}					2950811	740896
b_{60}					6661730	141976
b_{61}					641555	–527673
b_{62}					–4511116	–327618
b_{63}					–2338095	278227
b_{64}					2425494	363809
b_{65}					2811738	–70646
b_{66}					–688945	–304819
b_{67}					–2490395	–63159
b_{68}					–522533	205798
b_{69}					1741565	124363
b_{70}					1162189	–107173
b_{71}					–878642	–131357
b_{72}					–1300087	31104
b_{73}					132893	107182
b_{74}					1084786	15644
b_{75}					366118	–71728
b_{76}					–693209	–36319
b_{77}					–588382	38331
b_{78}					283878	38783
b_{79}					580424	–13557
b_{80}					34715	–31453
b_{81}					–430178	–1230
b_{82}					–215231	20983
b_{83}					231231	7729
b_{84}					263758	–11463
b_{85}					–56082	–8791
b_{86}					–220104	4659

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Table 24. FIR Stage Coefficients (continued)

COEFFICIENT	SESSION 1	SESSION 2	SESSION 3		SESSION 4	
			Scaling = 134217728		Scaling = 134217728	
	LINEAR PHASE SCALING = 1/512	LINEAR PHASE SCALING = 1/8388608	LINEAR PHASE	MINIMUM PHASE	LINEAR PHASE	MINIMUM PHASE
b_{87}					–56626	7126
b_{88}					134826	–732
b_{89}					101135	–4687
b_{90}					–50629	–976
b_{91}					–94192	2551
b_{92}					–7546	1339
b_{93}					61387	–1103
b_{94}					33460	–1085
b_{95}					–25549	314
b_{96}					–34123	681
b_{97}					348	16
b_{98}					22008	–349
b_{99}					10620	–96
b_{100}					–8280	144
b_{101}					–10663	78
b_{102}					–266	–46
b_{103}					7419	–42
b_{104}					6692	9
b_{105}					2481	16
b_{106}					–75	0
b_{107}					–432	–4
b_{108}					–132	0
b_{109}					0	0

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$$\text{HPF Gain Error Factor} = \frac{1 + \sqrt{1 - 2\left(\frac{\cos \omega_N + \sin \omega_N - 1}{\cos \omega_N}\right)}}{2 - \left(\frac{\cos \omega_N + \sin \omega_N - 1}{\cos \omega_N}\right)} \quad (11)$$

See the *HPF Stage* section for an example of how to use this equation.

HPF Transfer Function

$$\text{HPF}(Z) = \frac{2 - a}{2} \times \frac{1 - Z^{-1}}{1 - bZ^{-1}} \quad (12)$$

where *b* is calculated as shown in Equation 13:

$$b = \frac{1 + (1 - a)^2}{2} \quad (13)$$

Table 25. t_{DR} Time for Data Ready (Sinc Filter)

f_{DATA}	f_{CLK} (1)
128k	440
64k	616
32k	968
16k	1672
8k	2824

(1) For SYNC and Wake-Up commands, f_{CLK} = number of CLK cycles from next rising CLK edge directly after eighth rising SCLK edge to $\overline{DRDY}$ falling edge. For Wake-Up command only, subtract two f_{CLK} cycles.

Table 25 is referenced by Table 11 and Table 13.

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (March 2009) to Revision D **Page**

- Added footnote 8 to Electrical Characteristics table 3
- Moved Equation 12 and Equation 13 to the *Appendix* from the *HPF Stage* section 17
- Added footnote 2 to Table 14, Ideal Output Code 24
- Corrected sign typo in Equation 11 42
- Updated Equation 13 42

Changes from Revision B (August 2008) to Revision C **Page**

- Changed t_{CMD} specification from 5 to 3 CLK cycles in Modulator Output Timing table 13
- Updated Equation 2 to include decimation ratio 14
- Corrected typo in Equation 3 15
- Updated Figure 29 16
- Minor graphical edits to Figure 38 21
- Minor graphical edits to Figure 39 21
- Changed $466/f_{CLK}$ to $468/f_{CLK}$ in t_{DR} row of Table 11 21
- Added 103% FS limit to gain calibration 28
- Changed Figure 56, showing alternate bias resistor location 37
- Corrected Table 24 (*Appendix, FIR Stage Coefficients*) 39

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1281IPW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ADS1281	Samples
ADS1281IPWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ADS1281	Samples
ADS1281IPWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ADS1281	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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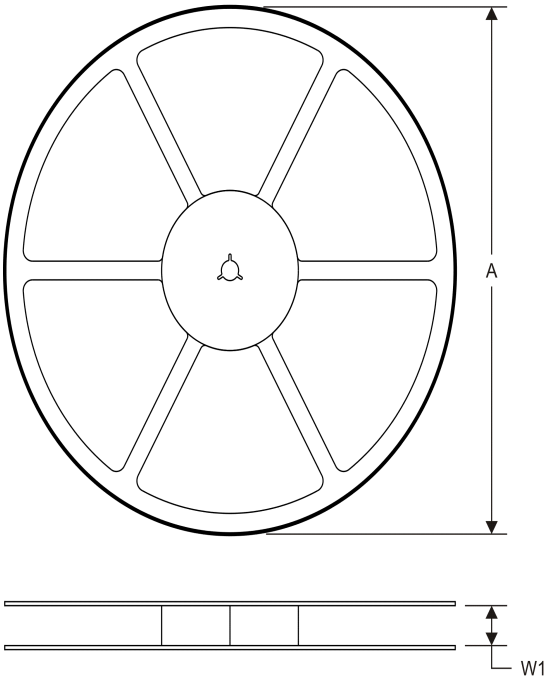
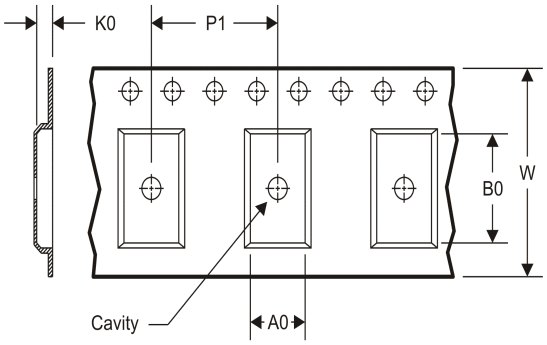
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



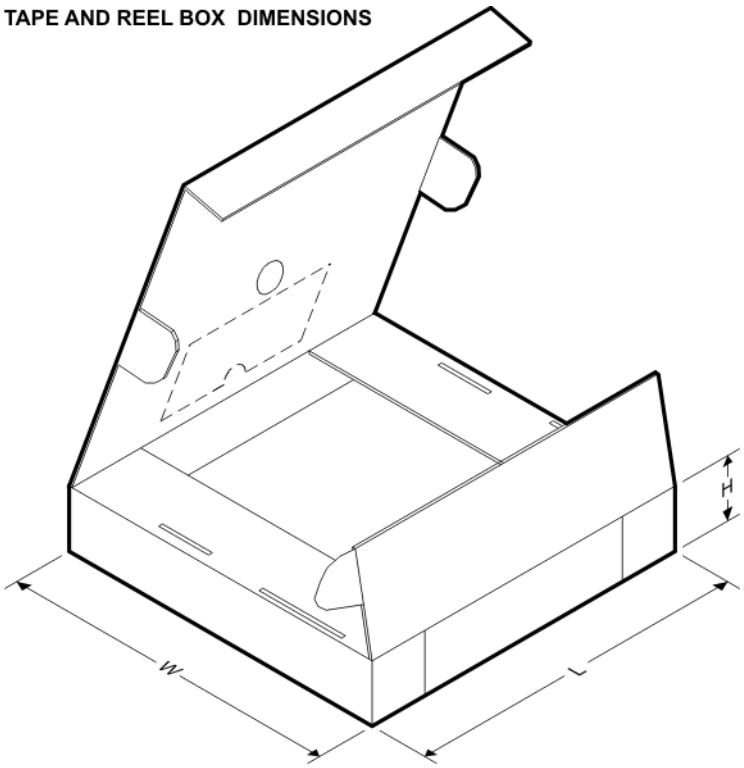
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1281IPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

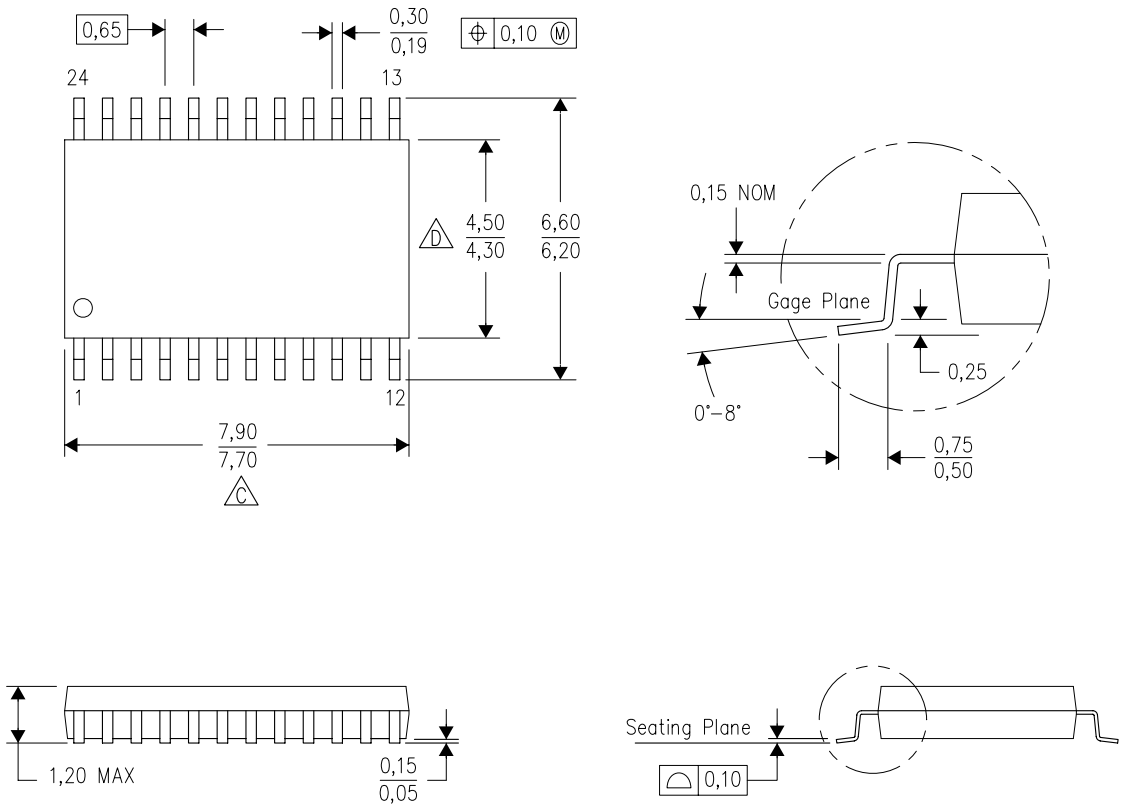
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1281IPWR	TSSOP	PW	24	2000	367.0	367.0	38.0

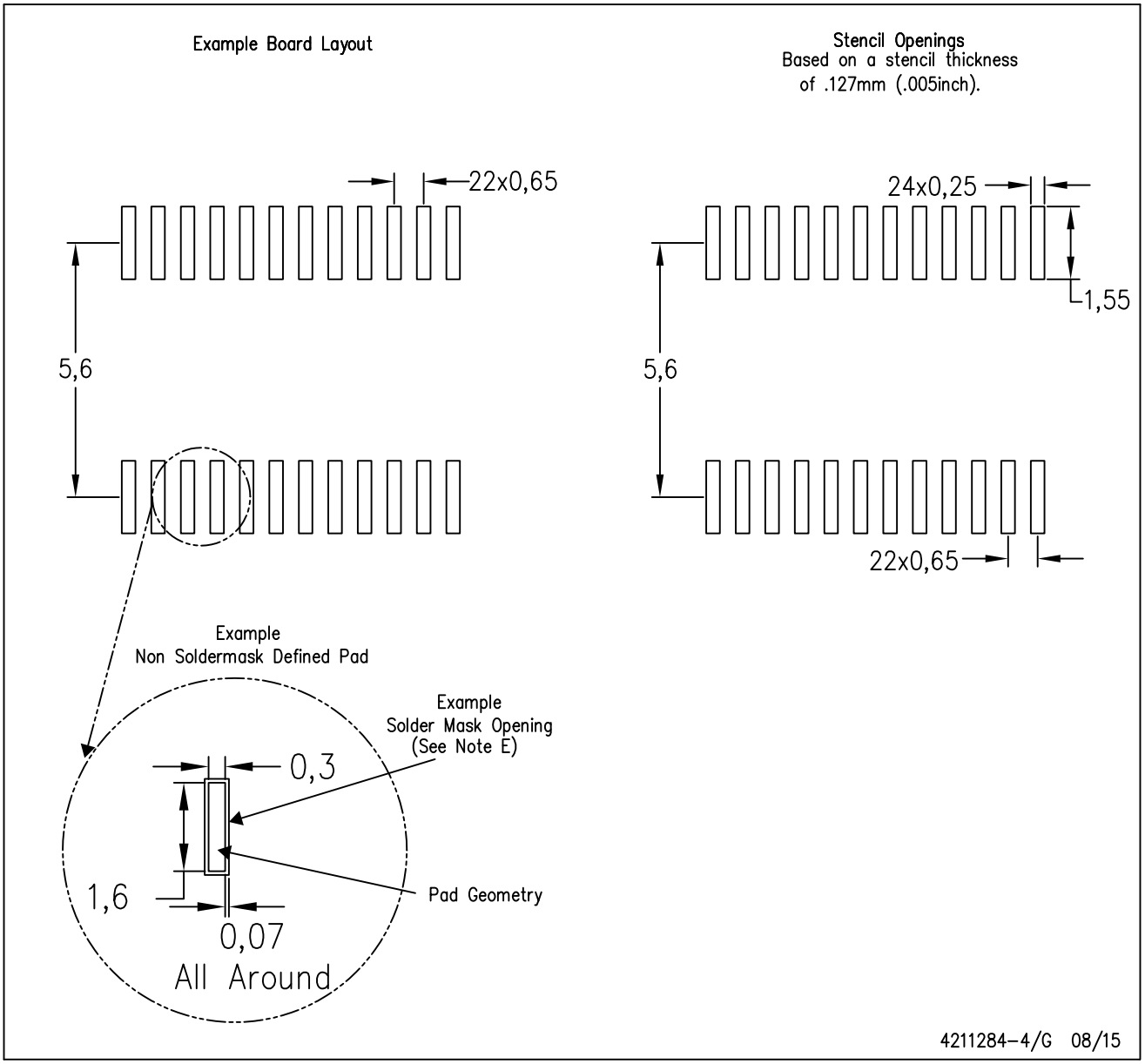
PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



4040064–6/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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