

NTK3043N

MOSFET – Power, N-Channel with ESD Protection, SOT-723 20 V, 285 mA

Features

- Enables High Density PCB Manufacturing
- 44% Smaller Footprint than SC-89 and 38% Thinner than SC-89
- Low Voltage Drive Makes this Device Ideal for Portable Equipment
- Low Threshold Levels, $V_{GS(TH)} < 1.3$ V
- Low Profile (< 0.5 mm) Allows It to Fit Easily into Extremely Thin Environments such as Portable Electronics
- Operated at Standard Logic Level Gate Drive, Facilitating Future Migration to Lower Levels Using the Same Basic Topology
- These are Pb-Free and Halogen-Free Devices

Applications

- Interfacing, Switching
- High Speed Switching
- Cellular Phones, PDAs

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	20	V
Gate-to-Source Voltage			V _{GS}	±10	V
Continuous Drain Current (Note 1)	Steady State	T _A = 25°C	I _D	255	mA
		T _A = 85°C		185	
	t ≤ 5 s	T _A = 25°C		285	
Power Dissipation (Note 1)	Steady State	T _A = 25°C	P _D	440	mW
	t ≤ 5 s			545	
Continuous Drain Current (Note 2)	Steady State	T _A = 25°C	I _D	210	mA
		T _A = 85°C		155	
Power Dissipation (Note 2)			T _A = 25°C	P _D	310
Pulsed Drain Current	t _p = 10 μs		I _{DM}	400	mA
Operating Junction and Storage Temperature			T _J , T _{STG}	–55 to 150	°C
Source Current (Body Diode) (Note 2)			I _S	286	mA
Lead Temperature for Soldering Purposes (1/8" from case for 10 seconds)			T _L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)
2. Surface-mounted on FR4 board using the minimum recommended pad size.

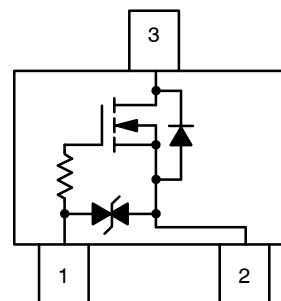


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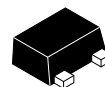
$V_{(BR)DS}$	$R_{DS(on)}$ TYP	I_D Max
20 V	1.5 Ω @ 4.5 V	285 mA
	2.4 Ω @ 2.5 V	
	5.1 Ω @ 1.8 V	
	6.8 Ω @ 1.65 V	

Top View

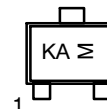


1 – Gate
2 – Source
3 – Drain

MARKING DIAGRAM



SOT-723
CASE 631AA
STYLE 5



KA = Device Code
M = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
NTK3043NT1G	SOT-723*	4000 / Tape & Reel
NTK3043NT5G	SOT-723*	8000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

*These packages are inherently Pb-Free.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	280	°C/W
Junction-to-Ambient – $t = 5$ s (Note 3)	$R_{\theta JA}$	228	
Junction-to-Ambient – Steady State Minimum Pad (Note 4)	$R_{\theta JA}$	400	

3. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)
4. Surface-mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = 100$ μ A	$V_{(BR)DSS}$	20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$I_D = 100$ μ A, Reference to 25°C	$V_{(BR)DSS}/T_J$		27		mV/°C
Zero Gate Voltage Drain Current	$V_{GS} = 0$ V, $V_{DS} = 16$ V	I_{DSS}			1	μ A
					10	
Gate-to-Source Leakage Current	$V_{DS} = 0$ V, $V_{GS} = \pm 5$ V	I_{GSS}			1	μ A

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250$ μ A	$V_{GS(TH)}$	0.4		1.3	V
Gate Threshold Temperature Coefficient		$V_{GS(TH)}/T_J$		-2.4		mV/°C
Drain-to-Source On Resistance	$V_{GS} = 4.5$ V, $I_D = 10$ mA	$R_{DS(ON)}$		1.5	3.4	Ω
	$V_{GS} = 4.5$ V, $I_D = 255$ mA			1.6	3.8	
	$V_{GS} = 2.5$ V, $I_D = 1$ mA			2.4	4.5	
	$V_{GS} = 1.8$ V, $I_D = 1$ mA			5.1	10	
	$V_{GS} = 1.65$ V, $I_D = 1$ mA			6.8	15	
Forward Transconductance	$V_{DS} = 5$ V, $I_D = 100$ mA	g_{FS}		0.275		S
Gate Resistance	$T_A = 25^\circ\text{C}$	R_G		2.2		k Ω

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	$V_{GS} = 0$ V, $f = 1$ MHz, $V_{DS} = 10$ V	C_{ISS}		11		pF
Output Capacitance		C_{OSS}		8.3		
Reverse Transfer Capacitance		C_{RSS}		2.7		

SWITCHING CHARACTERISTICS, $V_{GS} = 4.5$ V (Note 4)

Turn-On Delay Time	$V_{GS} = 4.5$ V, $V_{DD} = 5$ V, $I_D = 10$ mA, $R_G = 6$ Ω	$t_{d(ON)}$		13		ns
Rise Time		t_r		15		
Turn-Off Delay Time		$t_{d(OFF)}$		94		
Fall Time		t_f		55		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{GS} = 0\text{ V}, I_S = 286\text{ mA}$	$T_J = 25^{\circ}\text{C}$	V_{SD}		0.83	1.2	V
		$T_J = 125^{\circ}\text{C}$			0.69		
Reverse Recovery Time	$V_{GS} = 0\text{ V}, V_{DD} = 20\text{ V}, dI_{SD}/dt = 100\text{ A}/\mu\text{s}, I_S = 286\text{ mA}$		t_{RR}		9.1		ns
t_a				7.1			
Charge Time			t_b		2.0		
Discharge Time					Q_{RR}		3.7
Reverse Recovery Charge							

5. Pulse Test: pulse width ≤ 300 μ s, duty cycle $\leq 2\%$
6. Switching characteristics are independent of operating junction temperatures

TYPICAL PERFORMANCE CURVES

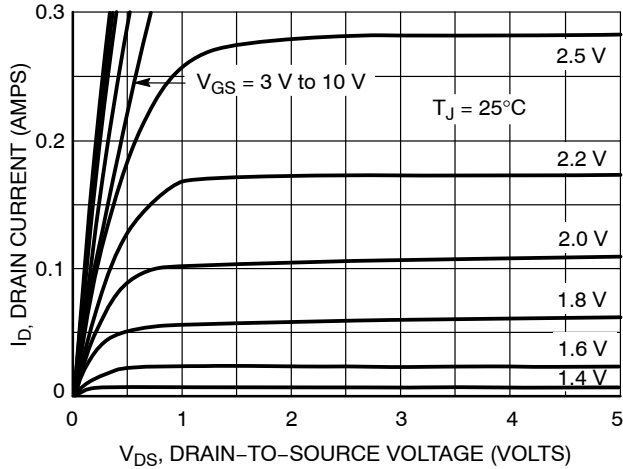


Figure 1. On-Region Characteristics

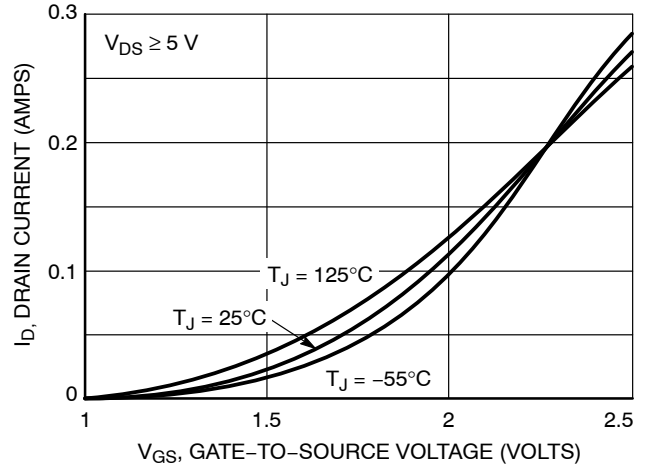


Figure 2. Transfer Characteristics

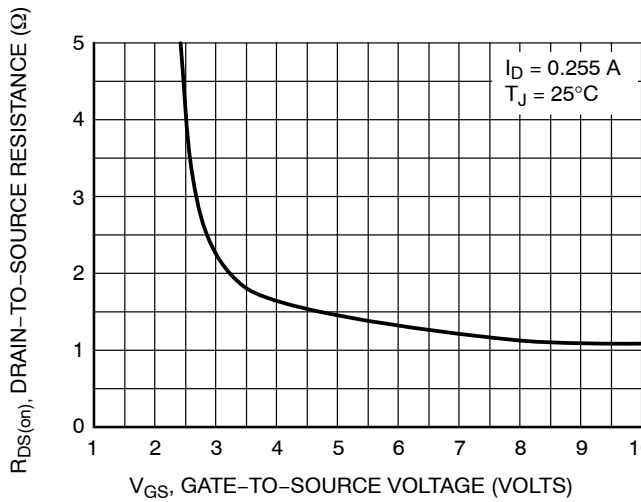


Figure 3. On-Resistance vs. Gate-to-Source Voltage

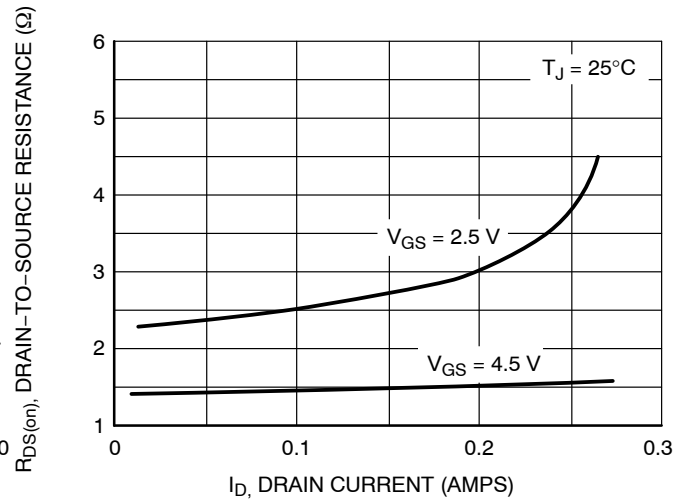


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

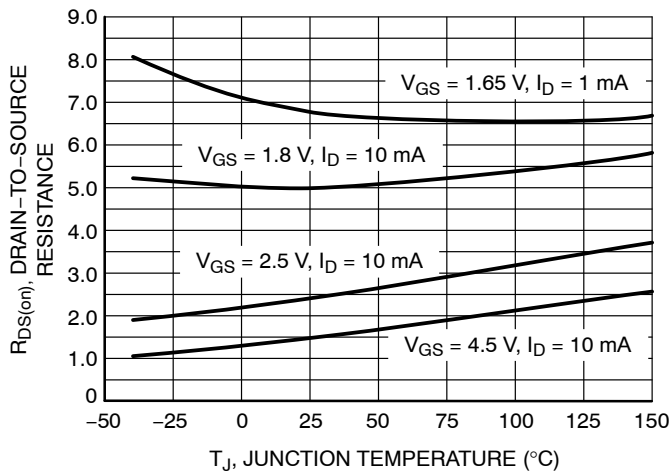


Figure 5. On-Resistance Variation with Temperature

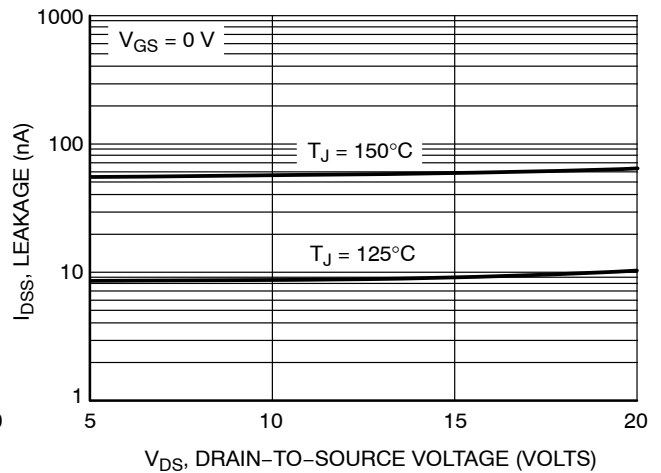


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

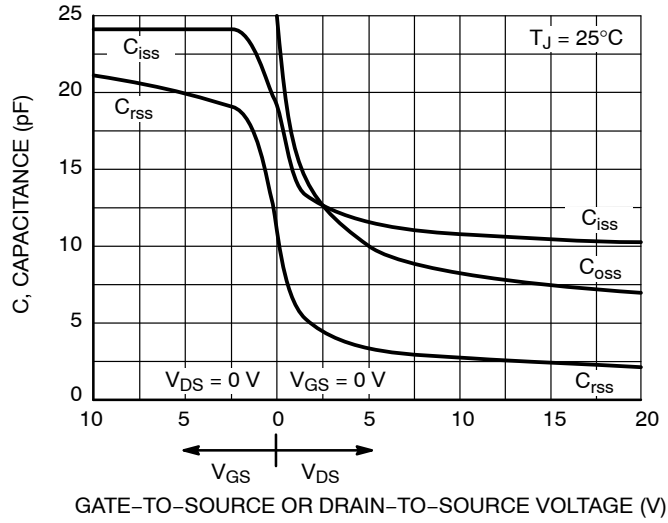


Figure 7. Capacitance Variation

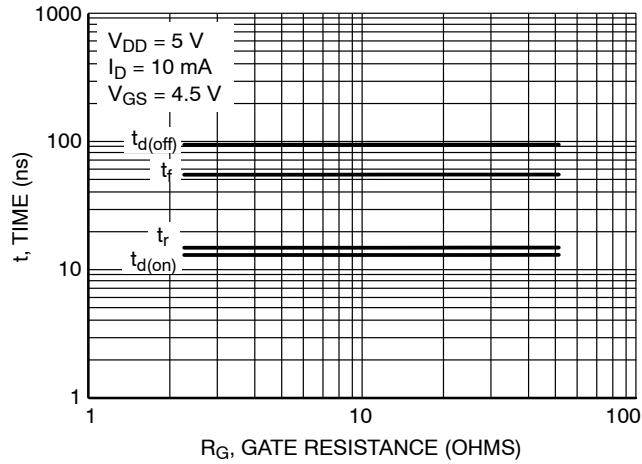


Figure 8. Resistive Switching Time Variation vs. Gate Resistance

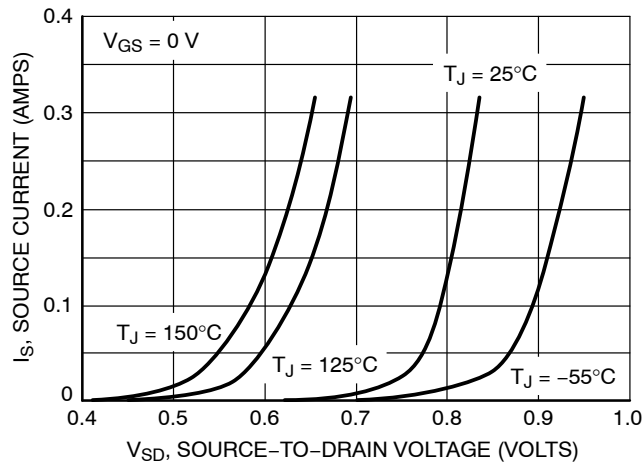


Figure 9. Diode Forward Voltage vs. Current

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

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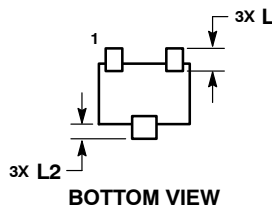
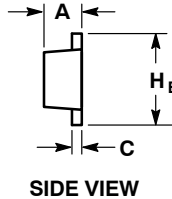
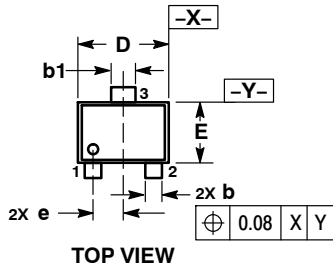
ON



SCALE 4:1

SOT-723 CASE 631AA-01 ISSUE D

DATE 10 AUG 2009



STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

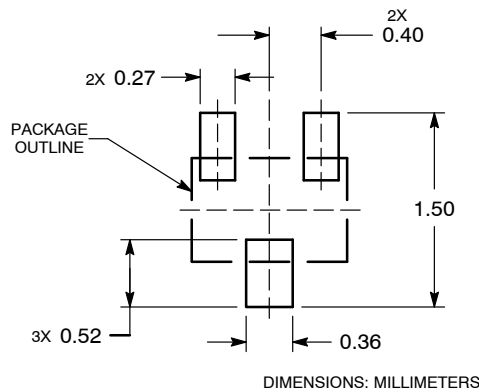
STYLE 2:
PIN 1. ANODE
2. N/C
3. CATHODE

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. GATE
2. SOURCE
3. DRAIN

RECOMMENDED SOLDERING FOOTPRINT*



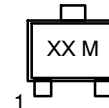
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.45	0.50	0.55
b	0.15	0.21	0.27
b1	0.25	0.31	0.37
C	0.07	0.12	0.17
D	1.15	1.20	1.25
E	0.75	0.80	0.85
e	0.40 BSC		
H E	1.15	1.20	1.25
L	0.29 REF		
L2	0.15	0.20	0.25

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present.

DOCUMENT NUMBER: 98AON12989D

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DESCRIPTION: SOT-723

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